Digital storage oscilloscope
PM3310

Instruction manual/Gerätehandbuch/Notice d'emploi et d'entretien

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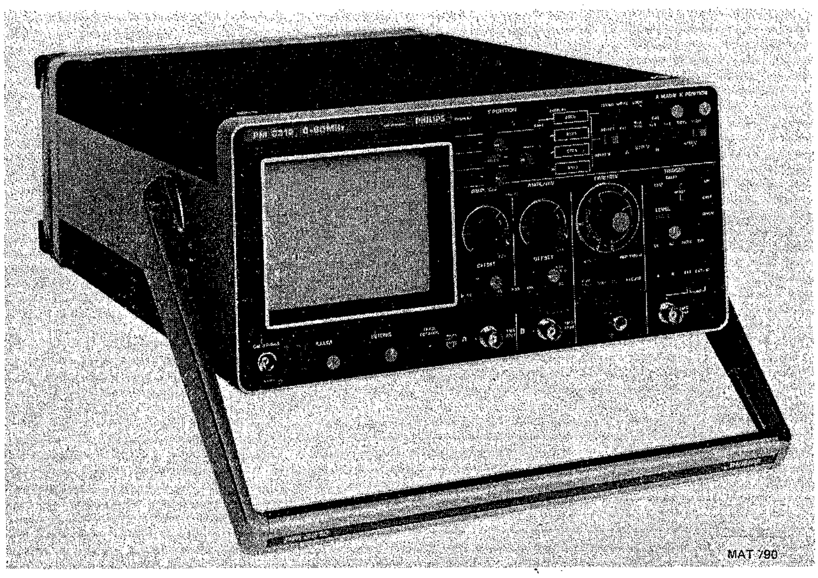


PHILIPS

IMPORTANT

In correspondence concerning this instrument, please quote the type number and serial number as given on the type plate.

NOTE: *The design of this instrument is subject to continuous development and improvement. Consequently, this instrument may incorporate minor changes in detail from the information contained in this manual.*

WICHTIG

Bei Schriftwechsel über dieses Gerät wird gebeten, die genaue Typenbezeichnung und die Gerätenummer anzugeben. Diese befinden sich auf dem Leistungsschild.

BEMERKUNG: *Die Konstruktion und Schaltung dieses Geräts wird ständig weiterentwickelt und verbessert. Deswegen kann dieses Gerät von den in dieser Anleitung stehenden Angaben abweichen.*

IMPORTANT

Dans votre correspondance et dans vos réclamations se rapportant à cet appareil, veuillez TOUJOURS indiquer le numéro de type et le numéro de série qui sont marqués sur la plaquette de caractéristiques.

REMARQUES: *Cet appareil est l'objet de développements et améliorations continuels. En conséquence, certains détails mineurs peuvent différer des informations données dans la présente notice d'emploi et d'entretien.*

PRINTED IN THE NETHERLANDS

CONTENTS

1. GENERAL INFORMATION

1.1. INTRODUCTION

The PM 3310 Digital Storage Oscilloscope is a portable, two-channel 60 MHz measuring instrument featuring micro-processor controlled electronic circuits.

A compact ergonomic design facilitates the extensive measuring capabilities of the instrument.
The versatile circuit arrangement combined with the software of the micro-processor gives a wide range of facilities, including:

- Brilliant display.
- Pre-trigger view.
- Storage of two channels with four different "event" signals per channel.
- IEC-bus optional (with the aid of PM 3325).
- Plotter output.
- Trigger delay.
- Memory back-up (batteries not included).

Furthermore, a large 8 cm x 10 cm screen with illuminated graticule lines provides for easier viewing, a 10 kV accelerating potential giving a high-intensity trace with a well-defined spot.
The oscilloscope is provided with numerous integrated circuits, which ensure stable operation and reduce the number of adjusting points.

The supply voltage can be set to one of two ranges: 100 ... 120 V ± 10 % or 220 ... 240 V ± 10 %.
As a result of the features listed above, the oscilloscope is suitable for a wide range of applications, for example the measurement and observation of:

- Rise-time (gives brilliant display intensity).
- Fast signals with a very low repetition rate.
- Very low frequency signals (up to 1 hour per division).

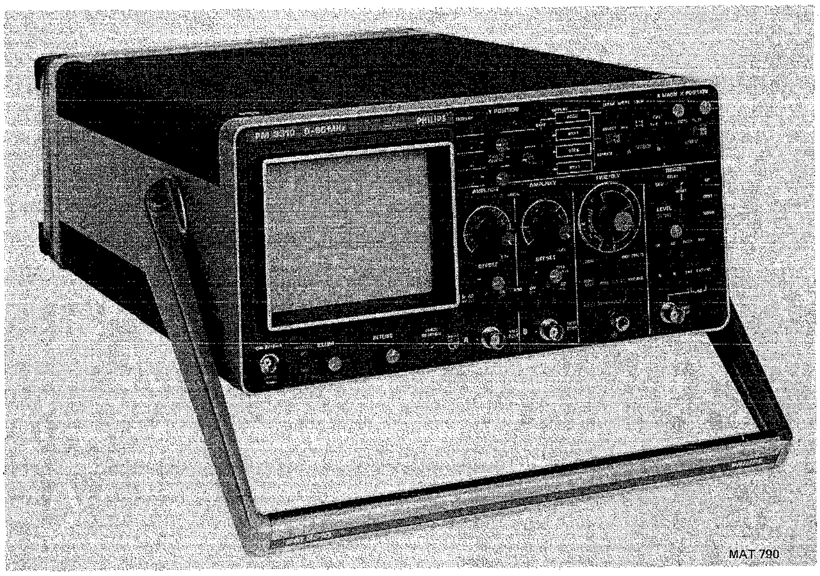


Fig. 1.1. 60 MHz Digital storage oscilloscope PM 3310

1.2. CHARACTERISTICS

This instrument has been designed and tested in accordance with IEC Publication 348 for Class 1 instruments and has been supplied in a safe condition. The present Instruction Manual contains information and warnings that shall be followed by the purchaser to ensure safe operation and to retain the instrument in a safe condition.

- This specification is valid after the instrument has warmed up for 30 minutes (reference temperature 23 °C).
- Properties expressed in numerical values with tolerance stated, are guaranteed by the manufacturer. Numerical values without tolerances are typical and represent the characteristics of an average instrument.
- Inaccuracies (absolute or in %) relate to the indicated reference value.

	Designation	*Specification*	*Additional information*
1.2.1.	**C.R.T.**		
	Cathode ray tube	D14 - 292 GH/39	
	Accelerating voltage	10 kV	
	Screen size	8 x 10 cm	Metal backed
	Phosphor type	P31 (GH)	
	Graticule	Internal	With centimeter divisions and 2 mm subdivisions along the central vertical axis shorter 2 mm divisions along the second, fourth, sixth and eight horizontal axis.
	Graticule illumination	Clearly visible under normal light conditions and continuously variable	
	Trace rotation	Front panel screwdriver adjustment	
	Focus	Adjusted automatically	
1.2.2.	**Input vertical**		
	Frequency range	d.c. 0 ... 60 MHz a.c. 10 Hz ... 60 MHz	
	Rise-time	< 6 ns	
	Pulse aberrations	± 3 %	Measured in Y-expand with a test pulse of 8 div; rise-time 1 ns; frequency 1 MHz (except first 0.2 cm measured from mid pulse)
	Vertical deflection		
	Defl. coeff.	10 mV/div ... 50 V/div	12 Calibrated positions in 1-2-5 sequence
	Error limit	± 3 %	±5 % in Y - expand
	Continuous control range	1 : > 2.5	
	Input impedance	1 MΩ // 25 pF	
	Coupling	a.c. - 0 - d.c.	
	Max. perm. input voltage	± 400 V	d.c. + a.c. peak
	Input selection	A only B only Add A and B	Channel B can be inverted

C.M.R.R.	100 : 1	At 2 MHz max. common mode signal 8 div.
Dynamic range	2x voltage range	
DC offset	± 4x voltage range	
Max. sample rate	50 MHz	
Visible signal delay	> 10 ns	See also "delay"

1.2.3. Time-base

Time coefficients		
Repetitive only	5 ns ... 0.2 μs/div	
Direct	0.5 μs ... 0.2 s/div	
Roll	0.5 s ... 60 min/div	
Coefficient error	< 2 %	4% combined with delay in "REPETITIVE ONLY"
Resolution	25 samples/div	

1.2.4. Triggering

Source	A B EXT EXT : 10 Line	
Sensitivity		
Internal	0.3 div 0.15 div	at 60 MHz at 40 MHz
External	0.3 V 0.15 V	at 60 MHz at 40 MHz
Ext : 10	3 V 1.5 V	at 60 MHz at 40 MHz
Slope	+/–	
Modes	Auto d.c. a.c. TV-frame (1/1 picture)	20 Hz ... 60 MHz dc ... 60 MHz 10 Hz ... 60 MHz Acc. to CCIR (625 lines)
Level		
Auto	Proportional to peak-to-peak value of trigger signal	
a.c./d.c.	± 3 div	
Delay		
Range	–9 ... +9999 div 0 ... 100 div	0.2 s ... 0.5 μs/div 0.2 μs ... 5 ns/div
Accuracy	±2 mm or 0.01 % ±2 div + visible delay	0.2 s ... 0.5 μs/div 0.2 μs ... 5 ns/div
Input impedance	1 MΩ // 25 pF	
Max. input voltage	± 400 V	dc + ac peak

1.2.5.	**Memory**		
	Number of memories	4	1 accumulator memory and 3 store memories
	Resolution horizontal	1 : 250	In single trace mode
	Resolution vertical	1 : 250	
1.2.6.	**Operation modes**		
	Single	Refreshment of accumulator mem. takes place, when trigger level is reached and time set with trigger delay has been passed. Signal is stored according to position of trigger delay. During waiting time accumulator, is displayed and LED "NOT TRIG'D" lights up.	0.5 μs ... 0.2 s/div
	Recurrent	Signal in accumulator memory is displayed on the screen. After the time set with the trigger delay the memory is overwritten by new information.	5 ns . . . 0.2 s/div
	Roll	Signal is built-up point by point at the right-hand side of the screen and moves to the left. When accumulator is completely filled, information is placed in register 3, next in 2, then in 1 and next in accumulator. After this, roll-mode stops, indicated by flashing "RUN" light.	0.5 s ... 60 min/div
	Multiple	4 times single with "SAVE" in memories	0.5 μs ... 0.2 s/div
1.2.7.	**Display modes**		
	Memory	Covers 2 div. screen height	
	Channel display combinations		
	Accumulator	Depends on input selection	
	Register	Information as stored in accumulator can be selected for storage in each of the three register memories and is displayed if display button is depressed.	Total information held in STORE 1, 2 or 3 can be inverted.
	Vertical position range	± 8 div	
	Vertical expand	5 x	Memory covers 10 cm screen height. Indicated via LED in display section.
	Horizontal expand	1 : > 2.5	Continuous
	X-Y selection	Deflection in X-direction can be derived from time base or from memory contents derived from A-input	

	Memory modes	Clear	Accumulator memory is cleared
		Save (3x)	Contents of accumulator memory are stored in selected register
		Write	Input signal can be written in accumulator memory
		Lock	Memory system is closed
	Dot join	Pushbutton	Changes normal display mode (dot-join) into display of only dots.
1.2.8.	**Plot output**		
	Horizontal	1 V / full scale	
	Vertical	1 V / full scale	
	Pen lift	TTL comp. "0" = unblanked (pen down) "1" = blanked (pen up)	open collector output max. load 0,5V at 500 mA cont.
	Plot time	approx. 100 s.	
	Plot sequence	B plot after A plot	
1.2.9.	**Interfaces**		
	IEC-Bus	Optional by means of a plug-in p.c. board	
	IEC-Bus	Settings and output controllable from bus-line controller	
	Local/Remote	With IEC connector.	
1.2.10.	**X-Y Display**		
	Y f(t)	From time-base	
	Y f(x)	From YA input	Dot join is not in operation
	Bandwidth	See YA	
	Accuracy	< 5 %	Tube included
	Phase difference	Distance between signal derived from A and signal derived from B is 1/25 div.	
	Position	0 of stored A signal will be at centre of screen	
1.2.11.	**Calibration output**		
	Frequency	2.5 kHz	
	Voltage	3 V	
	Current	6 mA	
1.2.12.	**Power supply**		
	Line voltage	100 ... 120 V ± 10 % 220 ... 240 V ± 10 %	
	Line frequency	50 ... 400 Hz ± 10 %	
	Power consumption	< 65 W	

Battery		
Function	For memory back-up only	
Type	2 pen light batteries of 1.5 V	For instance 2 x 1.5 V Lithium SAFT 2 x 1.5 V Duracell
Insulation	The insulation of the power supply fulfils the safety requirements of IEC 348 cl. I for metal-encased instruments	

1.2.13. Environmental characteristics

Note: The characteristics are valid only if the instrument is checked in accordance with the official checking procedure. Details on these procedures and failure criteria are supplied on request by the PHILIPS-organisation in your country, or by N.V. PHILIPS' GLOEILAMPENFABRIEKEN, TEST AND MEASURING DEPARTMENT, EINDHOVEN, THE NETHERLANDS.

Ambient temperature	+ 5 °C ... +40 °C	Rated range of use
	−10 °C ... +40 °C	Operating temperature range
	−55 °C ... +75 °C	Storage temperature in accordance with MIL 28800 and a maximum at 24 hours on high and low temperature
Altitude		
Operating	5000 m (15000 ft)	In accordance with IEC 68-2-13 test M
Non-operating	15000 m (50000 ft)	
Humidity	Acc. IEC 68 Db	Instrument withstands 95 % RH over a temperature cycle of 25 °C to 40 °C (non-operating)
Shock	30 m/s^2	Operating; half sine-wave shock of 11 ms duration; 3 shocks per direction for a total of 18 shocks.
Vibration	3 m/s^2	Operating; vibrations in three directions with a maximum of 20 min. per direction; 10 minutes with a frequency of 5 - 25 Hz and amplitude of 1.016 mm p-p; 10 min with a frequency of 25 - 55 Hz and an amplitude of 0.5 mm p-p. An extra 10 minutes of the resonant of frequency with the highest rise in amplitude. Unit mounted on vibration table without shock absorbing material.
Dimensions	Length 460 mm	Handle and controls excluded
	Width 316 mm	Handle excluded
	Height 154 mm	Feet excluded See also Fig. 1.2.
Weight	Approx. 12 kg	

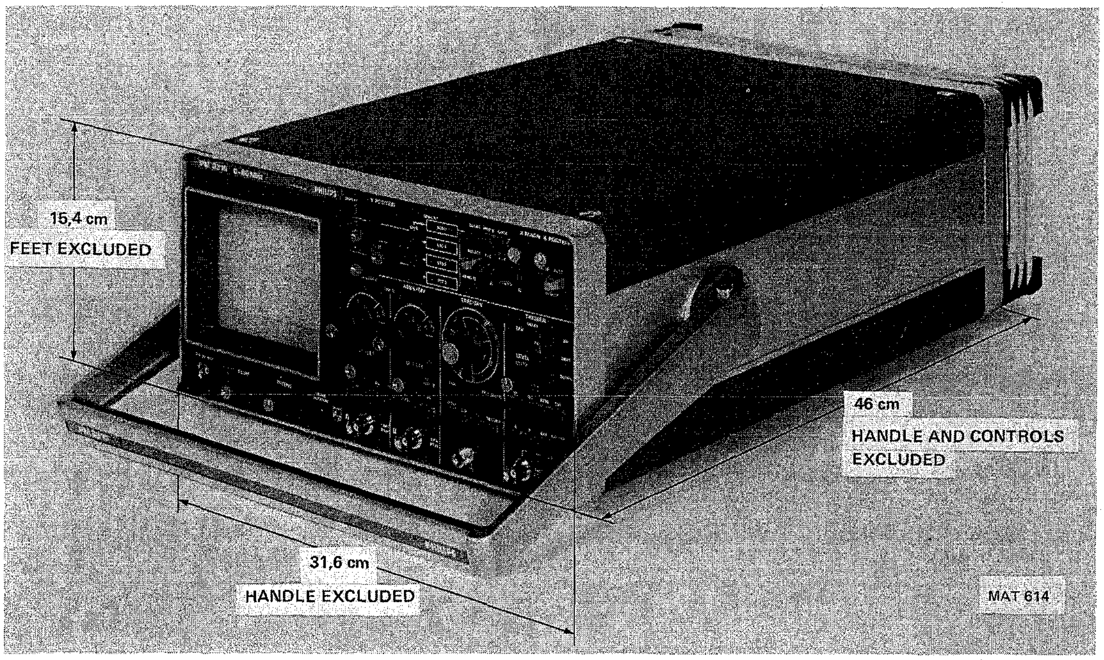


Fig. 1.2. Dimensions

1.3. ACCESSORIES

1.3.1. Accessories supplied with the instrument

- 2x 10 : 1 probe 1.5 m with range indication.
- 1x Cal terminal - BNC adaptor.
- 1x Blue contrast filter.
- 1x Collapsible viewing hood PM 9366.
- 1x Front cover with storage space for 3 probes.
- 1x Instruction manual.
- 2x BNC - 4 mm banana adaptor PM 9051.

1.3.2. Optional accessories

- Batteries for memory back-up.
- PM 3325 Printed-circuit board with connector and mounting materials for IEC bus operation (IEC-625).
- PM 8960 19-inch rack mount.

1.4. ACCESSORY INFORMATION

1.4.1. 10 : 1 probe (1.5 m) with range indication

The probe delivered with the oscilloscope PM 3310 is comparable to the standard probe PM 8927S. This is a 10x attenuator probe, designed for oscilloscopes up to 80 MHz, having a BNC input jack and 14 ... 40 pF input capacitance paralleled by 1 MΩ. At delivery the h.f. step response has been adjusted to the input capacitance of the PM 3310.
The probe is provided with a special BNC jack in order to obtain range indication. This means that the attenuator scale of the oscilloscope is adapted to the probe attenuation automatically.

Characteristics

Electrical

Attenuation	10x ±2 % (Oscilloscope input 1 MΩ)
Input resistance d.c.	10 MΩ ±2 % (Oscilloscope input 1 MΩ)
a.c.	See curve Fig. 1.3.
Input capacitance d.c. and l.f.	11 pF ± 1 pF (Oscilloscope input 1 MΩ ±5 % paralleled by 13 pF ±3 pF)
Input reactance h.f.	See curve Fig. 1.3.
Useful bandwidth	See curve Fig. 1.4a
Max. input voltage	500 V d.c. + a.c. peak, derating with frequency. See Fig. 1.4. Oscilloscope input 1 MΩ and voltage applied between probe tip and earthed part of probe body. Test voltage 1500 $V_{d.c.}$ during 1 s. at a temperature between 15 and 25 °C, a rel. hum. of 80 % at maximum and at sea level.
Check-zero button probe shell	Same function as 0 position of input coupling switch on oscilloscope.
Compensation range	14 ... 40 pF

Environmental

Probe operates within specifications over the following ranges:

Temperature	–25 °C to +70 °C
Altitude	Up to 5000 meters (15000 feet)
Other environmental data	Same as for any PHILIPS oscilloscope the probe is used with

Mechanical

Dimensions	Probe body 103 mm x 11 mm dia (max.) Cable length 1500 mm or 2500 mm Correction box 55 x 30 x 15 mm incl. BNC
Mass	Incl standard accessories 140 g

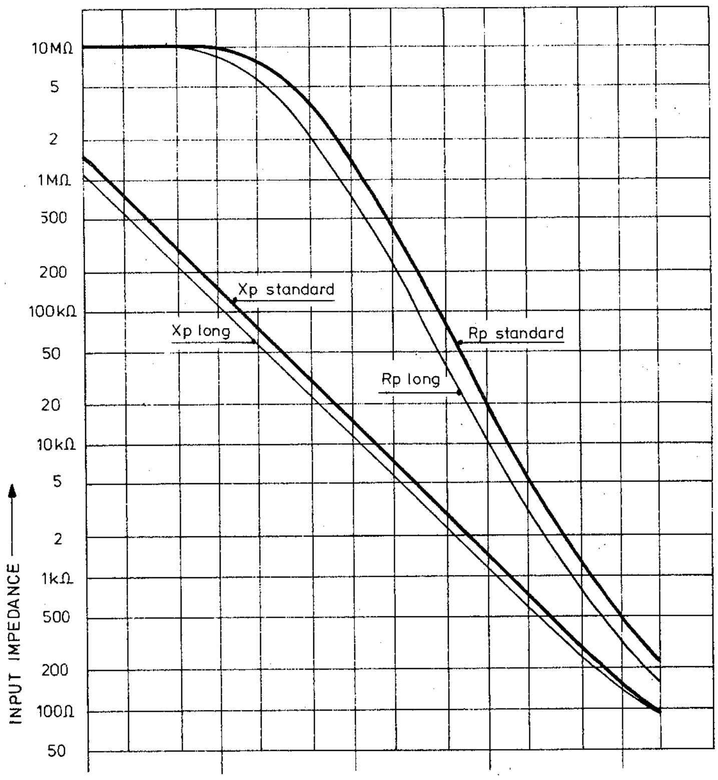


Fig. 1.3.

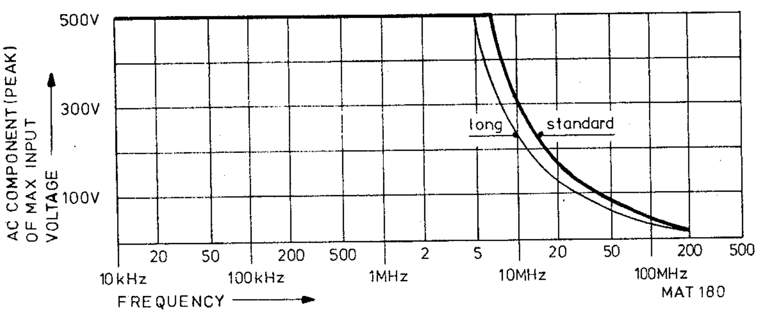


Fig. 1.4.

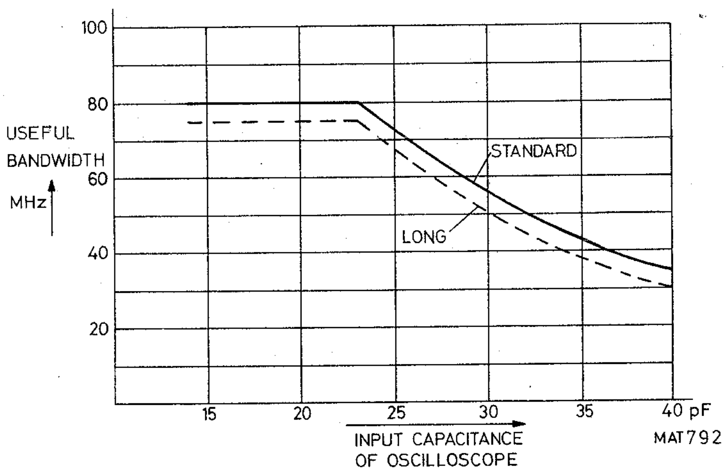


Fig. 1.4.a.

Adjustments

Matching the probe to your oscilloscope

The measuring probe has been adjusted and checked by the manufacturer. However, to match the probe to your oscilloscope, the following manipulation is necessary.
Connect the measuring pin to the CAL socket of the oscilloscope.
A trimmer C2 (Fig. 1.11.) can be adjusted through a hole in the compensation box to obtain optimum square-wave response. See Fig. 1.5., 1.6. and 1.7.

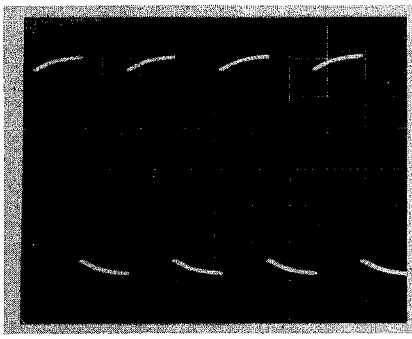


Fig. 1.5. Over-compensation (adjustment C2)

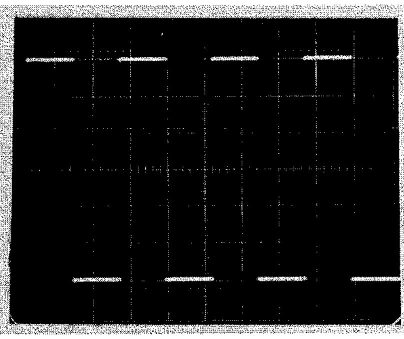


Fig. 1.6. Correct compensation (adjustment C2)

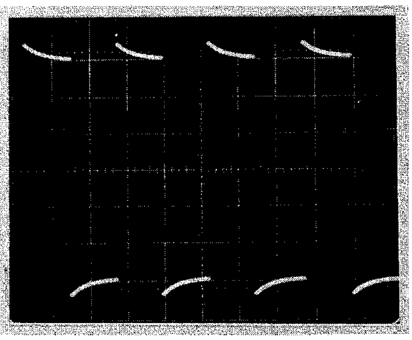


Fig. 1.7. Under-compensation (adjustment C2)

Adjusting the h.f. step response

The h.f. step response correction network has been adjusted by the manufacturer to match the oscilloscope input. For optimum pulse response, for separate delivered probes, the probe can be adjusted to match your particular oscilloscope. Later readjustment is only necessary if the probe is to be used with a different type of oscilloscope, or after replacement of an electrical component.
For the adjustment, proceed as follows:
Connect the probe to a fast pulse generator (rise-time not exceeding 1 ns) which is terminated by its characteristic impedance. Dismantle the compensation box. Set the generator to 100 kHz. Adjust R2 and R3 alternatively to obtain a display as shown in Fig. 1.8.
It is important that the leading edge is as steep, and the top is as flat, as possible. Incorrect settings of R2 and R3 give rise to pulse distortions as shown in Fig. 1.9. and 1.10.

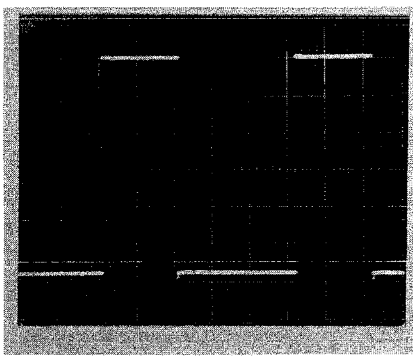


Fig. 1.8. Preset potentiometers correctly adjusted

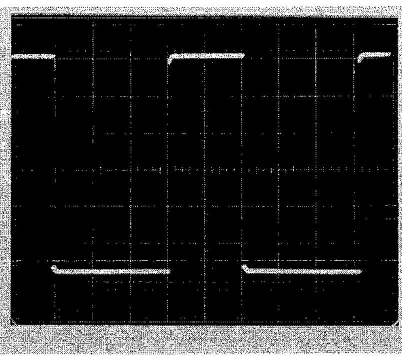


Fig. 1.9. Rounding due to incorrectly adjusted potentiometers

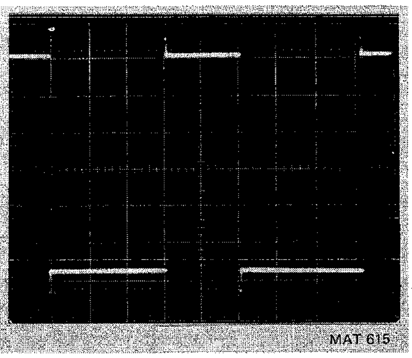


Fig. 1.10. Overshoot due to incorrectly adjusted potentiometers

Dismantling

Dismantling the probe (see Fig. 1.11.)

The front part 11 of the probe can be screwed from the rear part 13. Item 11 can then be slid from 12 and 13.
The RC combination 12 is soldered to 13. For replacement of 12 refer to the next section.

Dismantling the compensation box (see Fig. 1.11.)

Unscrew the ribbed collar of the compensation box to the cable. The case 14 can then be slide sideways off the compensation box. The electrical components on the printed-wiring board are then accessible.

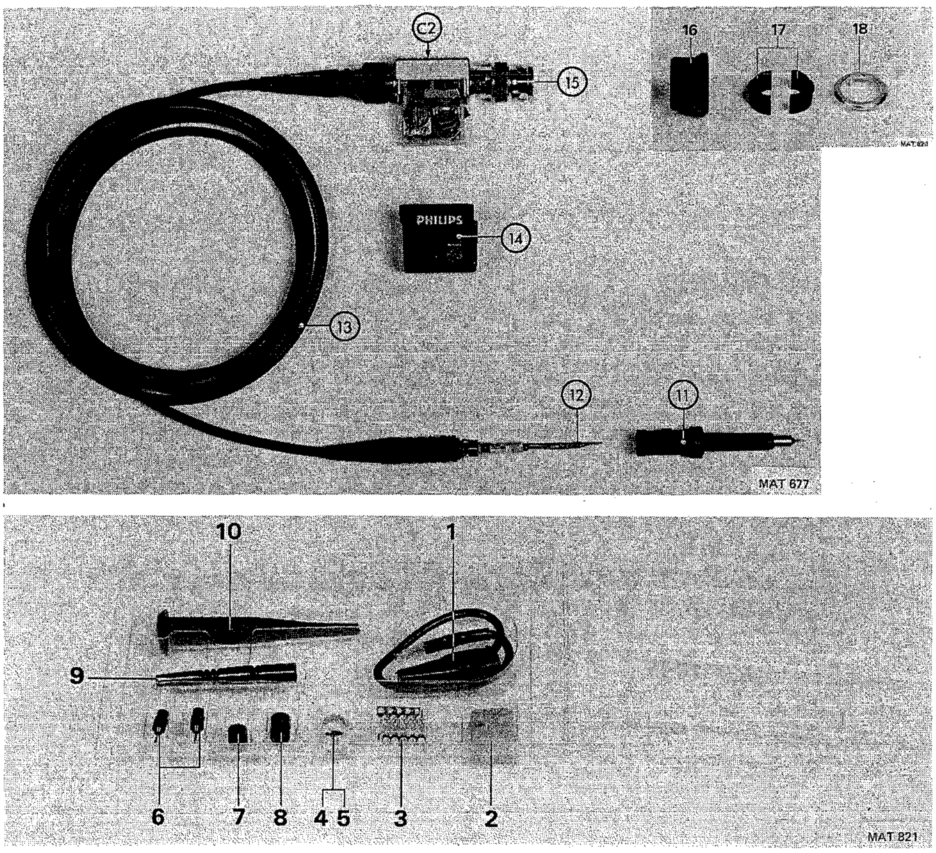


Fig. 1.11. Dismantling + accessories

Replacing parts

Assembling the probe

A new RC network is slid over the cable nipple, after which the cable core is soldered on to the resistor wire. When the measuring probe is assembled, the RC network must be at dead centre in the probe tip.

Replacing the cable assembly

Dismantle the compensation box.
Unsolder the connection between the inner conductor and the printed-wiring board. Keep the frame of the compensation box steady and loosen the cable nipple with a 5 mm spanner on the hexagonal part. Replace the cable and fit it, working in the reverse order.

Replacing the BNC

Dismantle the compensation box.
Unsolder the connection to the printed-wiring board. Hold the frame of the compensation box firmly and loosen the BNC with a 3/8 inch spanner. Replace the BNC and fit it, working in the reverse order.

Replacing the probe tip

The damaged tip can be pulled out by means of a pair of pliers. A new tip must be firmly pushed in.

Parts lists

Mechanical parts (see Fig. 1.11. and 1.12.)

Items 1 to 10 are standard accessories supplied with the probe.

Item	Order number	Qty	Description
1	5322 321 20223	1	Earth cable
2	5322 256 94136	1	Probe holder
3	5322 255 44026	10	Soldering terminals which may be incorporated in circuits as routine test points
4	5322 532 64223	2	Marking ring red
5	5322 532 64224	2	Marking ring white
	5322 532 64225	2	Marking ring blue (not shown)
6	5322 268 14017	2	Probe tip
7	5322 462 44319	1	Insulating cap to cover metal part of probe during measurements in densely wired circuits
8	5322 462 44318	2	Cap facilitating measurements on dual-in-line integrated circuits
9	5322 264 24018	1	Wrap pin adaptor
10	5322 264 24019	1	Spring-loaded test clip
11	5322 264 24021	1	Probe shell with check-zero button
12	5322 216 54152	1	RC network
13	5322 320 14063	1	Cable assembly
14	5322 447 64016	1	Cap
15	5322 268 44019	1	BNC connector
16	5322 532 64277	1	Holder
17	5322 532 64278	2	Ring
18	5322 532 14696	1	Contact ring
—	5322 492 64765	1	Contact spring
R	5322 116 55552	1	Resistor 2K32

Electrical parts

Item	Order number	Description
C1	–	Part of RC network (not supplied separately)
C2	5322 125 54003	Trimmer 60 pF, 300 V
R1	–	Part of RC network (not supplied separately)
R2	5322 101 14047	Potmeter 470 Ω, 20 %, 0.5 W
R3	5322 100 10112	Potmeter 1 kΩ, 20 %, 0.5 W

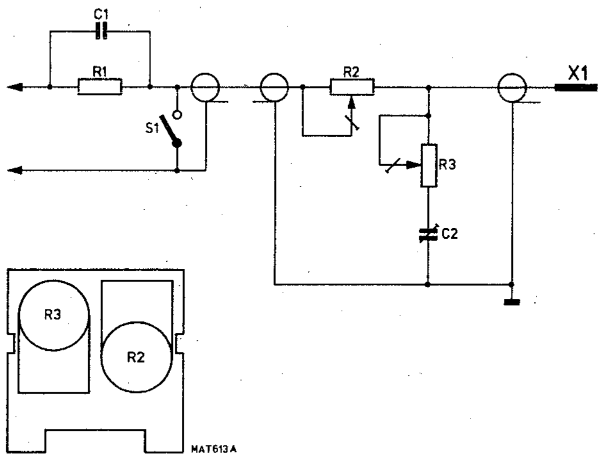


Fig. 1.12. Printed-wiring board showing adjusting elements, circuit diagram.

1.4.1.1. CAL TERMINAL–BNC adaptor

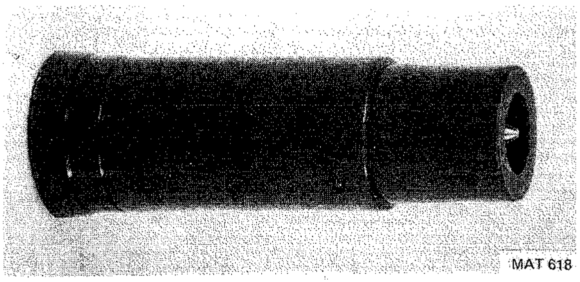


Fig. 1.13

1.4.1.2. BLUE CONTRAST FILTER

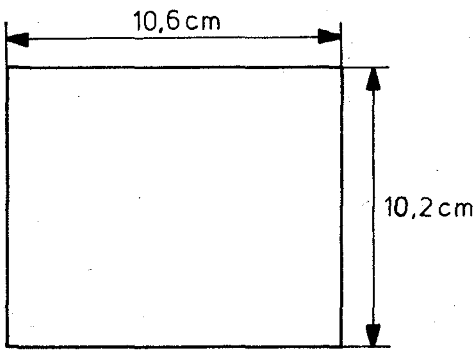


Fig. 1.14

1.4.1.3. PM9366 COLLAPSIBLE VIEWING HOOD

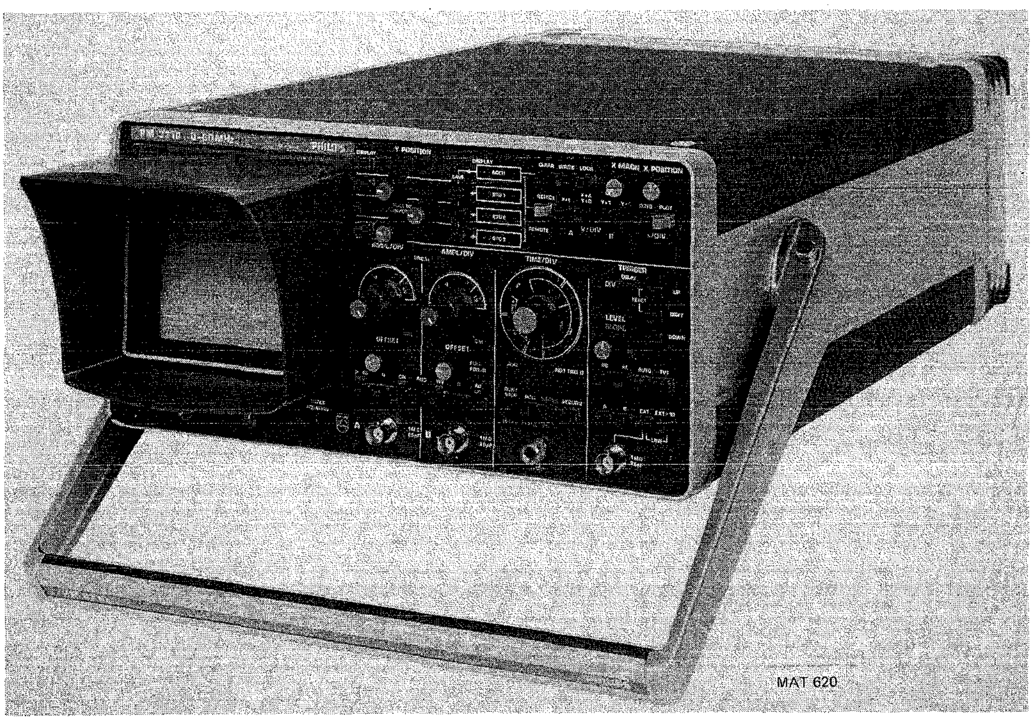


Fig. 1.15

1.4.1.4. FRONT COVER

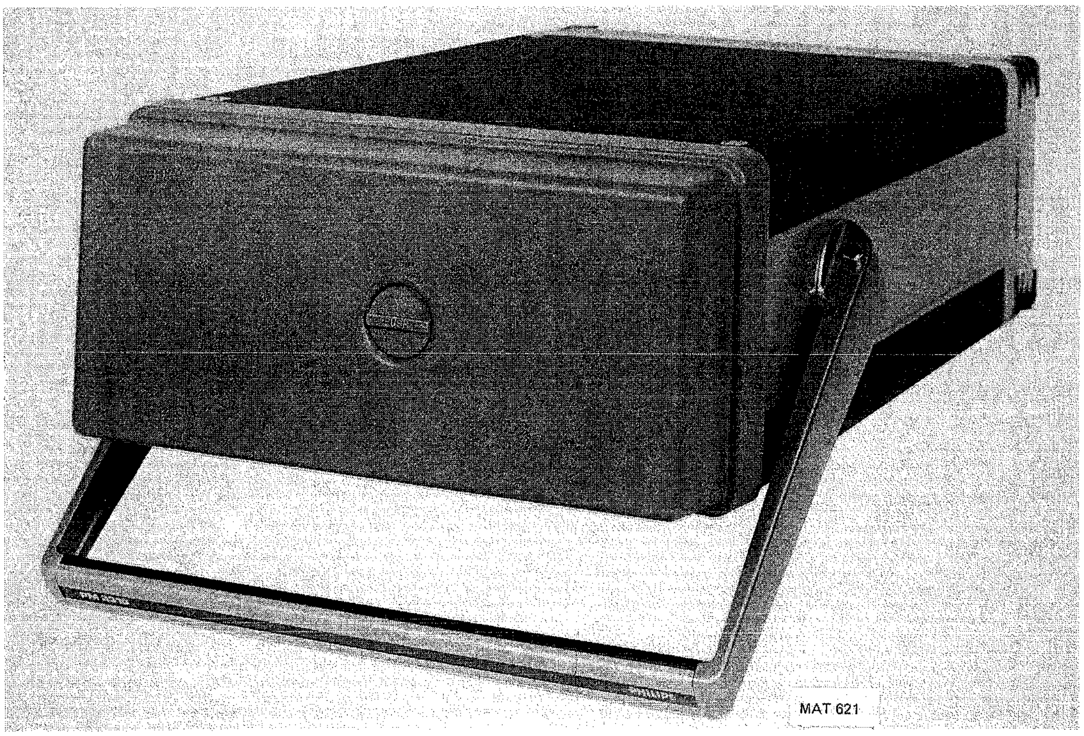


Fig. 1.16

1.4.1.5. BNC- 4mm BANANA ADAPTOR PM9051

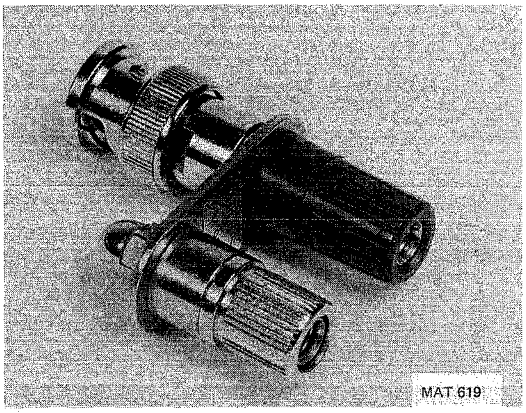


Fig. 1.17

1.4.2. Accessory information for optional items

1.4.2.1. BATTERIES FOR MEMORY BACK-UP

The instrument is equipped with a back-up facility to enable the memory contents and also the switch settings to be saved when the POWER switch is OFF.
When battery back-up is used, the information that was stored in the random access memories (RAMs) before the instrument was switched off is displayed again when the instrument is switched on after a period of time. Automatic display is given of the contents of the memory in which the last information was stored and also the associated switch settings.

Faulty or low battery functioning is not indicated by the oscilloscope. In that event, the instrument will function as if no memory back-up is present.
For technical reasons batteries are not included. If memory back-up is required install the batteries as described below.

Replacing the battery

WARNING: Always ensure that the mains supply is completely disconnected before removing any instrument cover plates.
The instrument is protected by four covers: a front panel protection cover, a rear plate and an upper and lower cabinet plate.

The batteries are accessible after the upper instrument cover is removed.
To remove instrument covers, proceed as follows:

- The upper cabinet plate can be removed after slackening the four quick-release fasteners at the corners of the plate. To prevent the fasteners coming apart, do not slacken more than two turns.

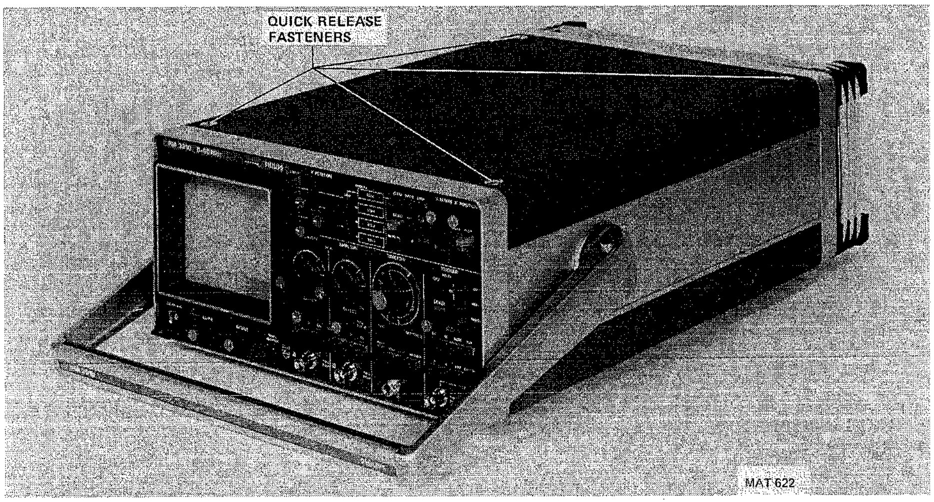


Fig. 1.18. Removing the instrument cover

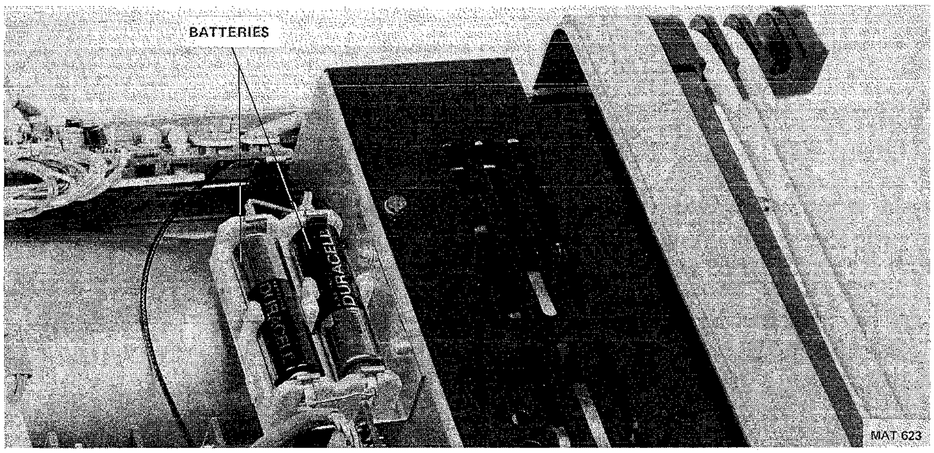


Fig. 1.19. Location of internal batteries.

Recommended battery types: 2x 1.5 V lithium saft or 2x 1.5 V duracell.

1.4.2.2. ASSEMBLING INSTRUCTIONS FOR RACK-MOUNT ADAPTOR KIT PM8960

Introduction

PM 8960 is an adaptor kit to enable the PM 3310 to be mounted in a 19" rack or cabinet. The instrument mounted with this kit can be slid out and inverted for easy inspection.

Contents of an adaptor kit PM 8960

Item in figure	Description	Number in kit
1	Handle	2
2	Front panel	1
3	Support, right-hand side	1
4	Cheese-head screw M4x12	4
5	Curved spring washer 4.1	10
6	Locking bracket	2
7	Support, left-hand side	1
8	Bracket	2
9	Telescopic rail	2
10	Countersunk screw M4x10	6
11	Hexagonal nut M4	6
12	Bracket	2
13	Cheese-head screw M5x10	8
14	Curved spring washer 5.1	8
15	Washer 5.3x10	8
16	Cupped washer 5.3x12	4
17	Countersunk M5x12	4

Mounting the telescopic rails

- Screw brackets, item 8, to the telescopic rails, item 9, by means of countersunk-head screws, item 10, curved spring washers, item 5, and hexagonal nuts, item 11. The fixing holes are accessible through an opening in the centre guide of the telescopic rails.
- Screw brackets item 12 to the rear end of the telescopic rails using equal numbers of items 5; 10 and 11.
- Screw the assembly between the mounting supports of the 19" cabinet or rack by means of cheese-head screws, item 13, washers, item 14, and curved spring washers, item 15.

Carrying handle

For removal:

- Remove the upper and lower instrument cover plates.
- Remove the plastic strip which is snapped on to the grip by slight leverage under one edge.
- Remove the four screws which secure the grip to the brackets.
- Depress the pushbuttons in the brackets and turn the carrying handle horizontally above the upper side of the oscilloscope.
- Keep the pushbutton of the right-hand bracket depressed and pull the bracket from its bearing.
- Remove the grip from the remaining bracket.
- Depress the pushbutton of the left-hand bracket and turn the latter horizontally below the base of the instrument.
- Keep the pushbutton depressed and pull the bracket from its bearing.

Fitting handles and supports to the front panel

Screw the supports, items 3 and 7, via the holes in front panel, item 2, to the handles with the aid of cheese-head screws, item 4, and curved spring washer, item 5.

Fitting the front panel to the oscilloscope

Pull the supports (items 3 and 7) slightly outwards and slip the front panel over the oscilloscope facia. Ensure that the narrower parts of the key holes in the supports point to the top of the oscilloscope. If they point downwards, turn the front panel-support combination 180° and fit it again round the oscilloscope. Slip the key holes in the supports over the handle bearings of the oscilloscope. Lock the supports to the oscilloscope by inserting locking brackets item 6 into the slots in the handle bearings.

Fitting the oscilloscope to the telescopic rails

Pull the telescopic rails all the way out. Slip the key holes in the supports (item 3 and 7) over the mushroom nuts in the front part of the rails and see that the oscilloscope slides down until the narrower part of the key holes rest on the mushroom nuts.

Slide the whole into the rack or the cabinet and secure the panel by means of countersunk-head screws, item 17, and cupped washers, item 16.

Turning the oscilloscope over for easy inspection

Pull the oscilloscope all the way out of the rack or cabinet.
Disengage the front key holes from their mushroom nuts and turn the oscilloscope over until its front rests against the rack or cabinet. For fitting the oscilloscope again in its normal position, proceed in reverse order

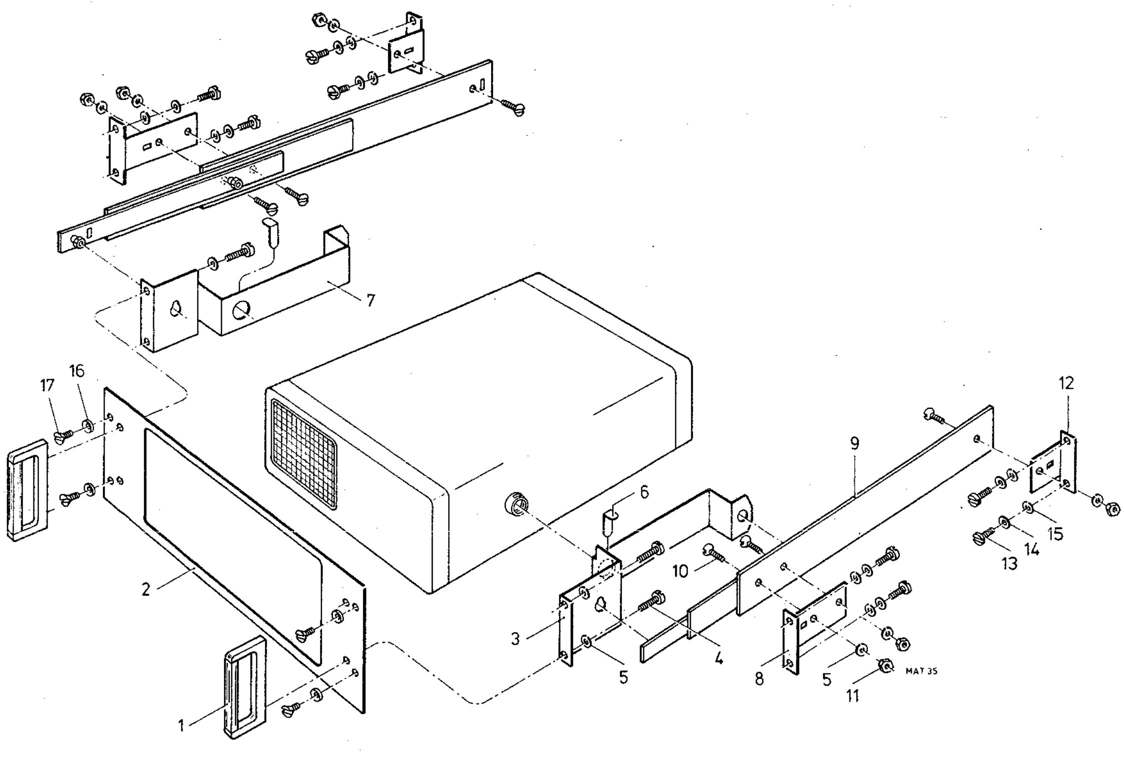


Fig. 1.20.

1.4.2.3. IEC bus interface PM 3325

General

The PM 3325 is a General Purpose Bus Interface according the IEC - TC 66 document, including a self-test facility.
Address selection is done by 5 switches (5 least significant bits of the ASCII characters).
A card function identification is also implemented.

Interface function repertoire for PM 3310

Interface function	*Symbol.*	*Identification*	*Remark*
Source handshake	SH	SH1	
Acceptor handshake	AH	AH1	
Talkerfunction	T	T6	
Listener function	L	L4	
Service request	SR	SR1	The PM 3310 is capable of sending a Service request.
Remote local	RL	RL2	No local lock out.
Device clear	DC	DC1	
Parallel poll	PP	PPØ	No capability
Device trigger	DT	DT1	
Controller function	C	CØ	No capability

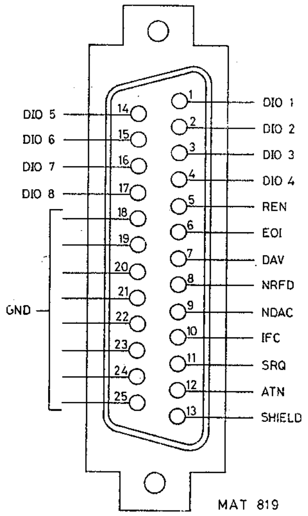
Service Request (SRQ)

The PM 3310 is capable to send a SRQ to indicate a special condition of the instrument.
A service request is given:
- If measurements are finished.
- After power on or reset, if the initialisation process is finished.
- If an incorrect programming code has been received.

After a SRQ, the controller can address the PM 3310 as "serial poll talker", than the status word is set on the Bus (DI08 . . . DI01).

A status word is built up as follows:

bit 8		Not used
bit 7 . . .	"1"	A SRQ has been given by the PM 3310
	"0"	No SRQ is given
bit 6 . . .	"1"	If an error is indicated.
	"0"	Normal condition
bit 5 . . .	"1"	Busy
	"0"	Ready
bit 4, bit 3, bit 2, bit 1		Not used



Input – Output

Input/output system	Bit parallel – Character serial
Input/output code	ISO 7 bit code ISO 646 (similar to ASCII)
	Input/output levels:
	L = –0.5 V . . . +0.8V
	H = +2V . . . +5.5V
	Logic levels for the 8 DIO lines
	L = 1
	H = 0

Connector contact assignment.

Connector Philips type	F161 male

Mounting

For mounting instructions see information delivered with the PM 3325.

Function of signals

Mnemonic	*Signal name*	*Direction*	*Description*
DIO 1	Data in/out 1	E ⟺ O	Data input/output
DIO 2	Data in/out 2	E ⟺ O	Data input/output
DIO 3	Data in/out 3	E ⟺ O	Data input/output
DIO 4	Data in/out 4	E ⟺ O	Data input/output
REN	Remote enable	E → O	Remote enable
EOI	End or identify	E ⟺ O	End or identify
DAV	Data valid	E ⟺ O	Condition of information
NRFD	Not ready for data	E ⟺ O	Device is busy
NDAC	Not data accepted	E ⟺ O	Condition of data acceptance
IFC	Interface clear	E → O	Resetting of the interface
SRQ	Service request	E ← O	Oscilloscope asks for service
ATN	Attention	E → O	Attention
SHIELD		E – O	
DIO 5	Data in/out 5	E ⟺ O	Data input/output
DIO 6	Data in/out 6	E ⟺ O	Data input/output
DIO 7	Data in/out 7	E ⟺ O	Data input/output
DIO 8	Data in/out 8	E ⟺ O	Data input/output
GND	Ground	E – O	Common
GND	Ground	E – O	Common
GND	Ground	E – O	Common
GND	Ground	E – O	Common
GND	Ground	E – O	Common
GND	Ground	E – O	Common
GND	Ground	E – O	Common
GND	Ground	E – O	Common

E = External Controller
O = Digital storage oscilloscope

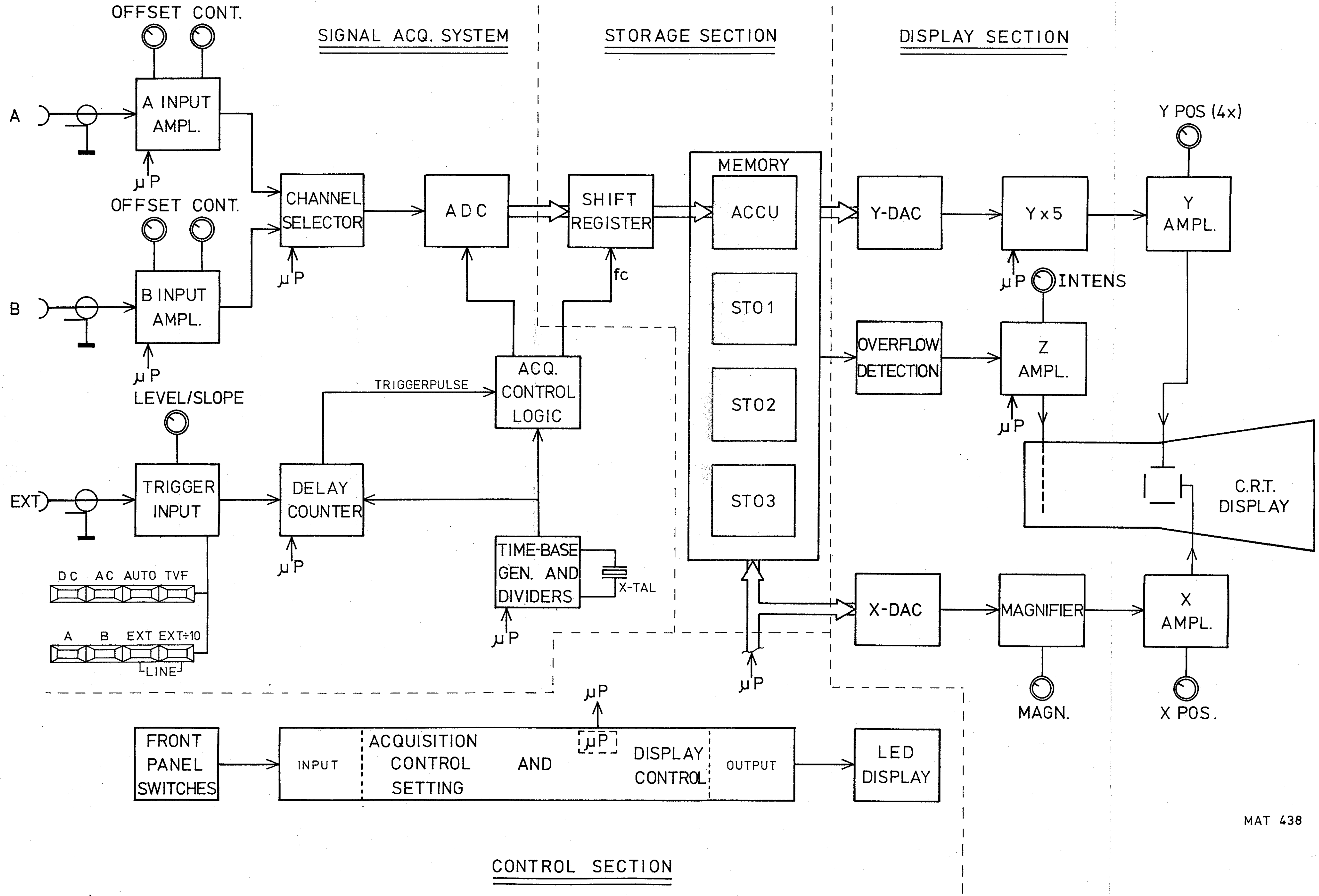
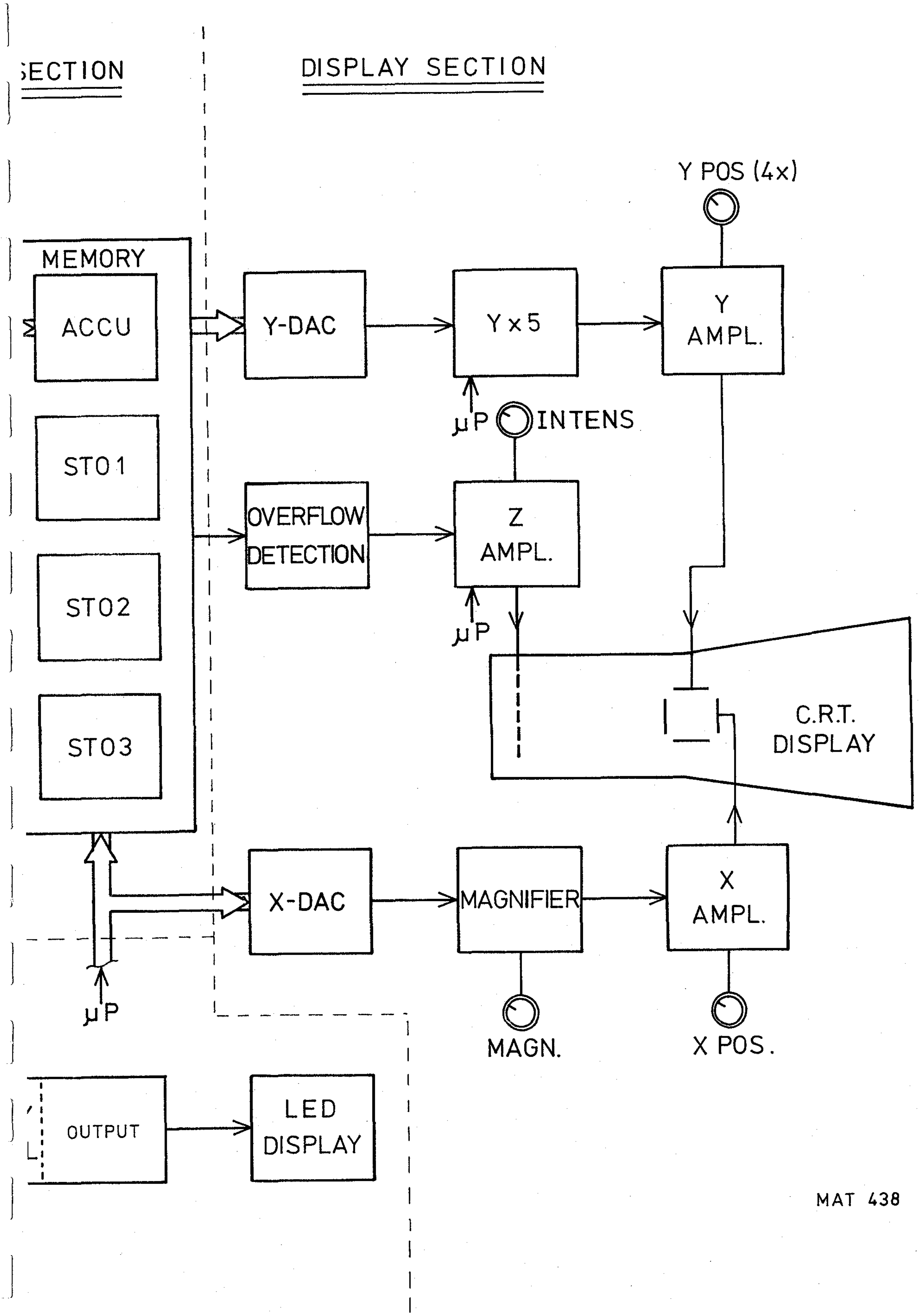


Fig. 1.2.1. Principle of operation



Address selection

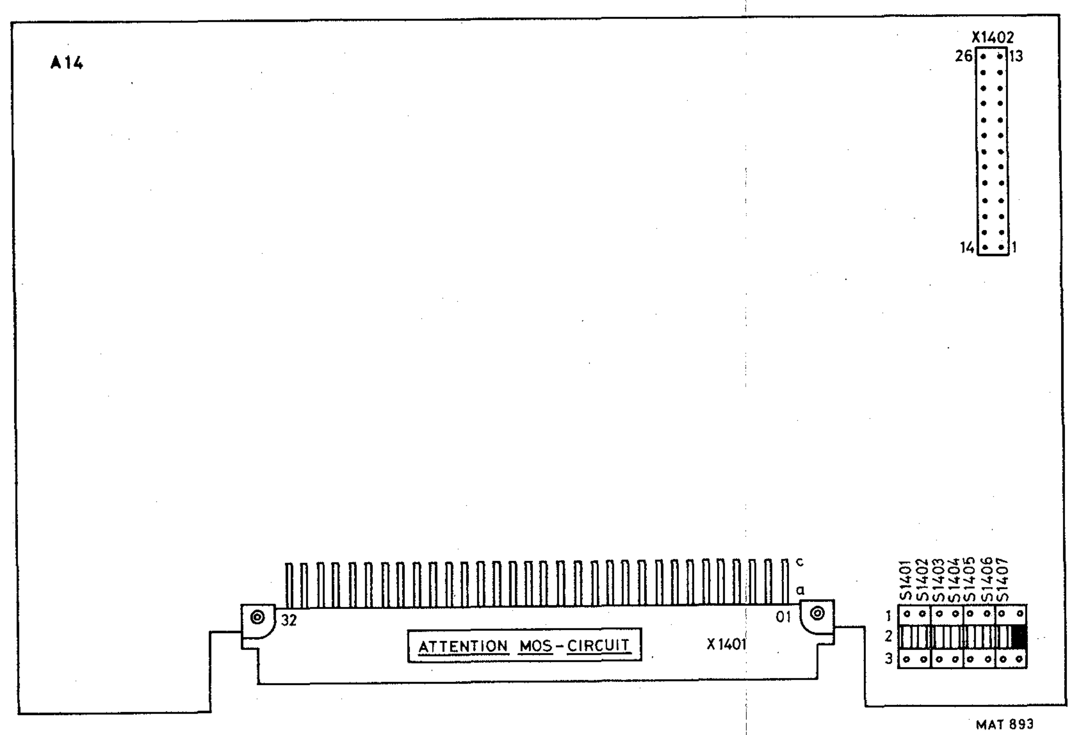
Select the address of the IEC bus interface (device address) by setting S1401 – S1405.
S1405 is the least significant bit, and S1401 is the most significant bit.

Example

	S1401	S1402	S1403	S1404	S1405	
	A5	A4	A3	A2	A1	SWITCH
01	0	0	1	0	0	Listen address 5
10	0	0	1	0	0	Talk address 5

Controlled by the system controller.

"Listen only" can be selected with switch S1407.
"Talk only", selectable with switch S1406.



For more detailed operating information refer to the separate booklet in this instruction manual.

1.5. PRINCIPLES OF OPERATION (See Fig. 1.21.)

In this section, the principles of operation of the PM 3310 are discussed at block diagram level, with special emphasis being applied to those parts of the circuit that differ from normal oscilloscope practice; i.e. the digital storage and control facilities.

1.5.1. General

The PM 3310 digital storage oscilloscope comprises four basic sections:

- a signal acquisition system
- a storage section
- a display section
- a control section.

These sections are now considered in some detail.

1.5.2. The signal acquisition system

The input signal to be displayed is applied to the channel selector via an attenuator and an amplifier. The front-panel control settings are scanned by the control section (the micro-processor system). After decoding, this information is applied to the attenuator, the amplifier and the channel selector to determine their correct characteristics.

The output of the channel selector is fed to the Analogue-to-Digital Converter (ADC) to convert it from an analogue signal into digital form. A conversion is started if the ADC receives a control pulse from the Acquisition Control Logic (ACL). On receipt of a control pulse, one instantaneous analogue value of the input signal is converted into a digital word by the ADC.

A trigger signal derived either from channel A, channel B, an external input, or from the mains frequency, is applied to the trigger delay counter. After a particular time, determined by the presetting of the delay counter, a trigger pulse is generated and applied to the acquisition control logic.

1.5.3. The storage section

After an analogue-to-digital conversion is completed, the Acquisition Control Logic (ACL) generates a clock pulse for the shift register. At every clock pulse one digital word of the ADC output is stored in the shift register and all existing stored information will shift one position.

The capacity of the shift register is 256 digital words, and therefore 256 converted instantaneous analogue values.
As soon as the trigger delay counter sends a trigger pulse to the ACL, and the ACL has supplied more than 256 pulses to the shift register, the latter is filled with information and the ACL stops generating clock pulses.

The contents of the shift register are now ready to be copied into the Random Access Memory referred to as ACCU. The transfer of information from the shift register to the ACCU is arranged via a "handshake" procedure in order to obtain a flicker-free display on the CRT. When the copying is completed, the shift register is "ready" and the action restarts.
The stored information in the ACCU can be copied into one of the other memories (STO 1, STO 2, STO 3). Each of these RAMs is able to contain 256 bytes of digital information. With both channels ON, the memory capability is equally divided into 128 bytes for each channel.

1.5.4. The display section

The information in the RAMs may now be displayed. The contents of each RAM are 256 words, each consisting of 8 bits. Each 8-bit word is capable of indicating 256 different amplitudes (i.e. $2^8 = 256$): Y parameters.
Each address of the memory corresponds to a specified vertical line of the display along the X-axis; i.e. the display of 10 divisions is divided into 256 lines.

With each 8-bit value per address being an instantaneous value in the Y direction, a display area of 2 vertical and 10 horizontal divisions is divided into 256 x 256 dots. When Y x 5 is selected, this area is expanded to 256 x 256 dots over 10 x 10 divisions.
An address counter sends 256 different addresses sequentially (starting with address 0 and ending with address 255) to the RAMs and to the Digital-to-Analogue Converter (DAC) of the X-system. To provide the discrete steps for the horizontal time-base display, the output of the X-DAC is a linear staircase voltage, which is applied to the X amplifier via the magnifier. The resulting output of the X amplifier is routed to the horizontal deflection plates of the CRT.
Similarly, the 8-bit instantaneous values for each address (i.e. the Y information) are converted into analogue signals by means of the Y-DAC. Via the Y x 5 magnifier, the converted signal is applied to the Y amplifier and then to the vertical deflection plates of the CRT.

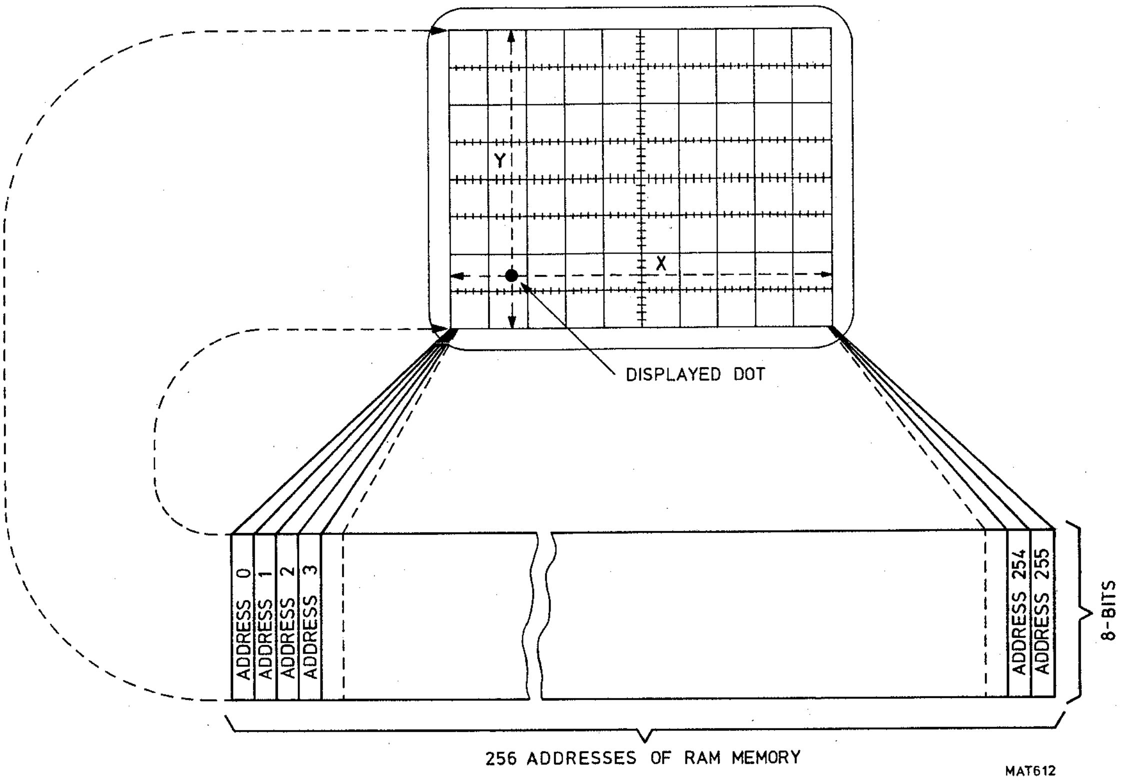


Fig. 1.22.

1.5.5. The control section

The control section consists of a micro-processor, memories, latches, input and output ports and relevant logic circuits.
The following functions are under its control:

- *Front panel switches*

  At a defined time interval the control section scans all switches (except the trigger source and trigger mode switches) on the front panel. The settings are decoded and the corresponding functions are set.
  To simplify operation, incorrect settings will be translated into meaningful settings (e.g. both channels OFF would be translated into channel A ON).

- *Recalculation*

  In the expand mode, the setting of AMPL/DIV are recalculated and displayed.

- *Display control*

  The control of the complete display is handled by the control section. The display section comprises the CRT, the pilot lamps, the alpha-numeric LEDs and associated circuits for the display elements.
  The CRT display is built-up dot by dot. In order to obtain a line display, the control section generates the control signals for the dot-joining system.

- *Handshake procedure*

  The input system (including the shift register) and the display system have different operating cycles. To obtain a flicker-free display, both systems are coupled via a handshake procedure, organised by the control section.

In addition to these standard oscilloscope functions, the control section also supervises the plot output and the handling of the IEC-bus option.

2. INSTALLATION INSTRUCTIONS

2.1. IMPORTANT SAFETY INSTRUCTIONS (IN ACCORDANCE WITH IEC 348)

Before connecting the instrument to the mains (line), visually check the cabinet, controls and connectors etc. to ascertain whether any damage has occurred in transit. If any defects are apparent, **do not** connect the instrument to the mains (line).

CLAIMS: In the event of obvious damage or shortages, or if the safety of the instrument is suspect, a claim should be filed with the carrier immediately. A Philips Sales or Service organisation should also be notified in order to facilitate the repair procedure.

Before any other connection is made, the protective earth terminal shall be connected to a protective conductor (see section 2.5. EARTHING).

WARNING: The opening of covers or removal of parts, except those to which access can be gained by hand, is likely to expose live parts and accessible terminals, which can be dangerous to life.

The instrument shall be disconnected from all voltage sources before any adjustment, replacement or maintenance and repair is effected with the instrument open. If afterwards any adjustment, maintenance or repair of the opened instrument under voltage is inevitable, it shall be carried out only by a skilled person who is aware of the hazards involved. Bear in mind that the capacitors inside the instrument may still be charged even if the instrument has been separated from all voltage sources.

2.2. REMOVING AND FITTING THE FRONT COVER

Removing:

- Push and rotate the knob in the centre of the cover a quarter-turn anti-clockwise to the UNLOCKED position.
- Remove the cover.

Fitting:

- Push and rotate the knob to the UNLOCKED position.
- Fit the cover over the front of the oscilloscope.
- Press and rotate the knob a quarter-turn clockwise to the LOCKED position.

Space is available in the front cover to accommodate accessories such as probes, collapsible viewing hood, etc. To open the front cover, press both tongues of the locking device and lift the inner plate.

2.3. POSITION OF THE INSTRUMENT

The instrument may be used in any desired position. With the handle folded down the instrument may be used in sloping position. The electrical characteristics in accordance with para. 1.2. are guaranteed for any position of the instrument. (Ensure that the ventilation holes in the top and bottom covers are free). Do not position the instrument on any surface which produces or radiates heat, or in direct sunlight.
The carrying handle can be rotated if the push-buttons on its bearings are depressed.

2.4. MAINS VOLTAGE SETTING AND FUSE

Before inserting the mains plug into the mains socket, make sure that the instrument is set to the local mains voltage.
This can be done by the MAINS ADAPTOR SWITCH on the rear panel.
The two-position switching enables the instrument to operate at any mains voltage between 100 V and 120 V ± 10 % (115 V visible in MAINS ADAPTOR SWITCH window) and between 220 V and 240 V ± 10 % (230 V visible in window).

The fuse-holder mounted on the rear panel carries a 2 A delayed-action fuse (4822 253 30025).

Make sure that only fuses with the required rated current and of the specified type are used for replacement. The use of mended fuses and the short-circuiting of fuse holders must be avoided. The instrument must be disconnected from all voltage sources when a fuse is to be replaced or when the instrument is to be adapted to a different mains voltage.

Note: The same 2 A delayed-action fuse is applicable for all settings of the mains adaptor switch.

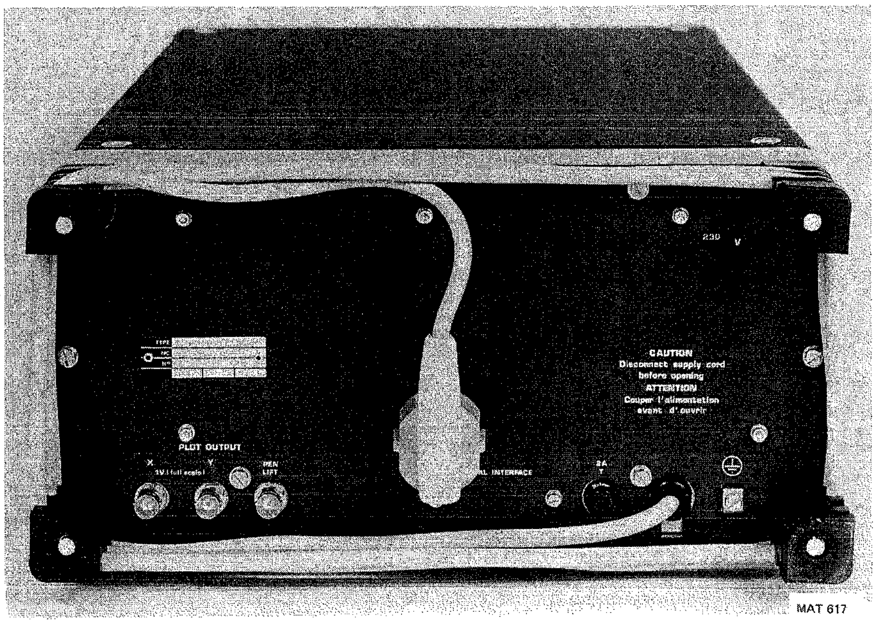


Fig. 2.1. Rear view of oscilloscope showing mains adaptor switch and fuse.

When not in use, the mains lead can be stored around the feet on the rear panel.

2.5. EARTHING

Before switching on, the instrument shall be connected to a protective earth conductor in one of the following ways:

- via the protective earth terminal;
- via the three-core mains cable. The mains plug shall only be inserted into a socket outlet provided with a protective earth contact. The protective action shall not be negated by the use of an extension cord without protective conductor.

WARNING: Any interruption of the protective conductor inside or outside the instrument, or disconnection of the protective earth terminal, is likely to make the instrument dangerous. Intentional interruption is prohibited.

When an instrument is brought from a cold into a warm environment, condensation may cause a hazardous condition. Therefore, make sure that the earthing requirements are strictly adhered to.

3. OPERATING INSTRUCTIONS

3.1. GENERAL INFORMATION

This section outlines the procedures and precautions necessary for operation.
It identifies and briefly describes the functions of the front and rear panel controls and indicators, and explains the practical aspects of operation to enable an operator to evaluate quickly the instrument's main functions.

3.2. SWITCHING-ON AND POWER-UP ROUTINE

3.2.1. Switching-on

After the oscilloscope has been connected to the mains (line) voltage in accordance with sections 2.4. and 2.5., it can be switched on with the **POWER** switch.
The POWER switch is incorporated in the graticule ILLUM control on the front panel, below the screen bezel. The associated POWER ON/OFF indicator lamp is adjacent to the ILLUM control/POWER switch.

When switching on the oscilloscope, it is immediately ready for use. With normal installation, according to Section 2, and after a warming-up time of 30 minutes, the characteristics according to Section 1.2. are valid.

WARNING: The oscilloscope must never be switched on whilst any circuit board is removed. (Except for IEC and SPARE circuit board).
Never remove a circuit board until the oscilloscope has been switched-off for at least one minute.

3.2.2. Power-up routine

When switching-on the instrument, note that the in-built micro-processor initiates an automatic test of a number of internal circuits including:

- Start test.
- PROM test.
- LED display test.
- RAM test.

The tests starts automatically after switching-on. At the end of the test cycle all pilot lamps,scale lamps and alpha-numerical display will light for about three seconds, and then the oscilloscope switches to normal operation.

If during the test a circuit is found to be faulty, the test stops. This will be visible by:

1. The instrument does not operate normally.
2. A number (but not all) pilot lamps and scale lamps will light.

If this occurs it is recommended to switch-off the instrument and switch-on again after a few seconds.
If after switching-on the same fault condition appears, contact your Philips service department or check in accordance with chapter 9 in the Service Manual.
If one or more of the pilot lamps and scale lamps do not light and the instrument reverts to the operative mode after the tests, that particular lamp might be defect.

If during operation the system blocks, which may be caused by extreme high static voltages, a switch-off and switch-on action will automatically reset the micro-processor controlled system and the oscilloscope will become operative again.

3.3. EXPLANATION OF CONTROLS AND SOCKETS

The controls and sockets are listed according to their sections and a brief description of each is given.

3.3.1. CRT section

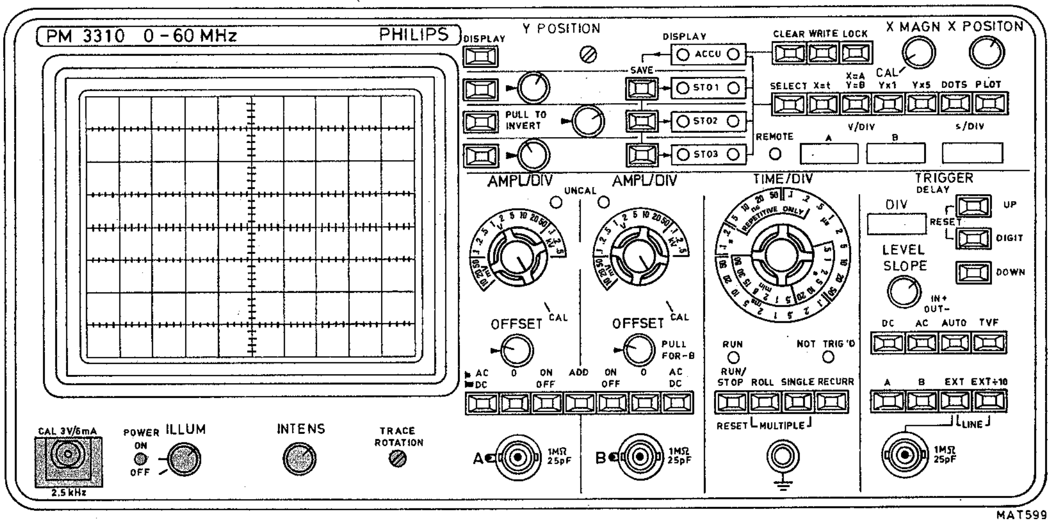
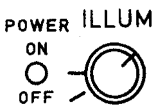


Fig. 3.1.

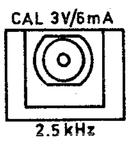


Continuously variable control of the graticule illumination, incorporating the POWER ON/OFF switch.
Pilot lamp indicates when the power is switched on.

Continuously variable control of the trace intensity.

Note: The PM 3310 is equipped with an automatic focus control. Therefore, external focus adjusting is superfluous.

Preset control for aligning the trace with the horizontal graticule lines (screwdriver control).



Output providing a 3 V_{p-p}, 2.5 kHz square-wave voltage, to calibrate vertical deflection AMPL control, or for frequency compensation of voltage divider probes.
Current loop with 6 mA_{p-p} for calibration of current probes.

3.3.2. Vertical section

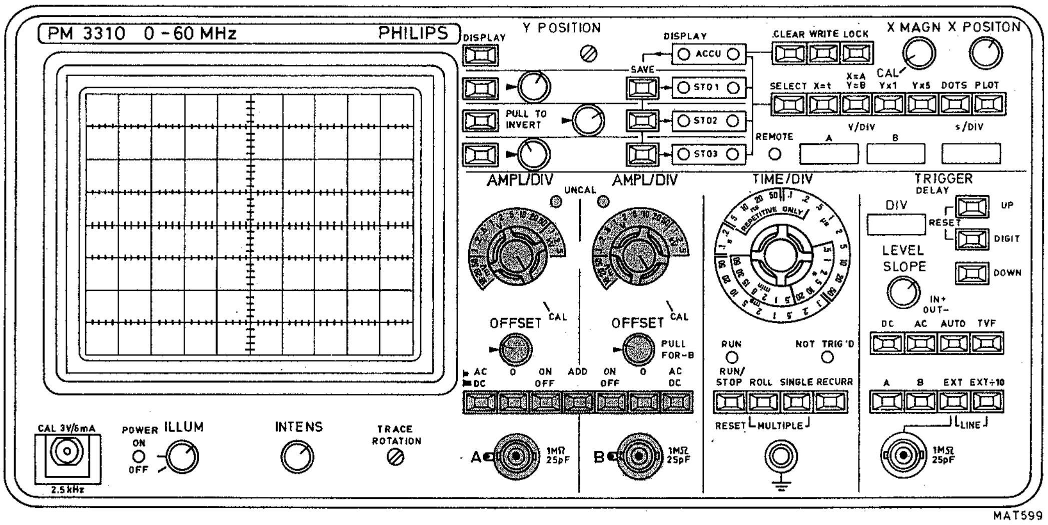
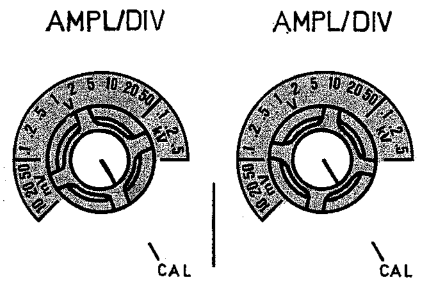


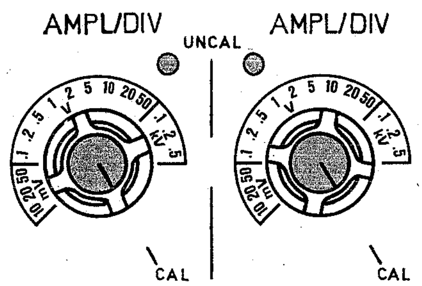
Fig. 3.2.



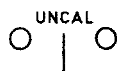
12-way step control of the vertical deflection coefficients, operating in a 1-2-5 sequence.
Using a 10:1 probe with range indication*, ranging is automatically effected from 0.1 V/div up to 0.5 kV/div.
With a 1:1 probe, ranging is possible from 10 mV/div up to 50 V/div.

Two indicator lamps are located under the AMPL/DIV outer knob scale. Normally the one on the left is ON, but when a 10:1 probe with probe indicator is used, the one on the right is ON.

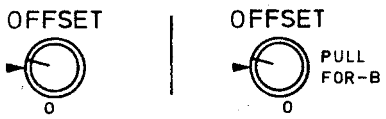
* Probes with range indication are delivered with the instrument.



Continuously variable control of the vertical deflection coefficients.
In the CAL position the selected deflection coefficient is calibrated.

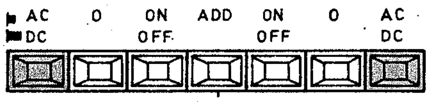


Pilot lamp indicating that the relevant AMPL/DIV switch off the CAL position. This situation is indicated by an asterisk (*) in the alpha-numeric display.



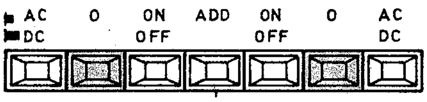
Continuous control for shifting the signal within the dynamic range of the memory (2 divisions on the screen).
If a part of the incoming signal is shifted out of the dynamic range of the memory, this part will be displayed on the CRT as a straight, flashing line at the top or bottom of the memory display part, depending if the signal has been shifted out of the upper or lower dynamic range.
If the complete signal is shifted out of the dynamic range, a complete straight flashing line will be displayed. The offset range is ± 4 times the selected attenuator setting.

A two-way push-pull switch is integrated with the channel B OFFSET control for the inversion of the signal polarity (PULL FOR –B).
This control is depressed for normal and pulled for –B.

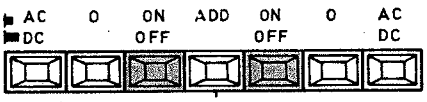


With AC/DC depressed, the relevant Y input coupling is achieved via a blocking capacitor (AC).

With AC/DC released the input coupling is direct (DC).



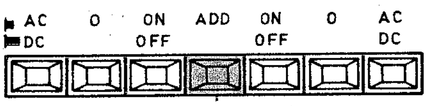
With 0 depressed, the connection between the Y input socket and its input circuit is interrupted and the input circuit is earthed.



With ON/OFF depressed, vertical deflection is achieved by the signal connected to the input socket of the relevant Y channel.

With ON/OFF released, the relevant Y channel trace will not be displayed.
To simplify operation, with both ON/OFF switches released, channel A will be displayed (i.e. the circuit makes allowance for human error!).

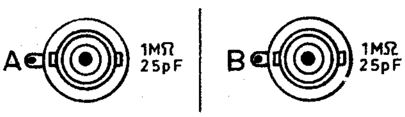
If both A and B channel are switched on as a result of setting both ON/OFF pushbuttons to ON, both signals will be stored in the accumulator memory. This ACCU memory contents is generally displayed in the upper two divisions of the CRT screen. (See also display section).



With ADD depressed, the sum signal (A + B) of channels A and B will be displayed.
In combination with PULL FOR –B, A-B will be displayed. The ADD mode can be selected independent of the ON/OFF switch settings.

For example, if channel A has been switched to OFF and channel B to ON, both A and B OFFSET controls are operative.

Note: With all pushbuttons released, channel A is automatically selected.



BNC input socket, including a range indicator input.

3.3.3. Horizontal section

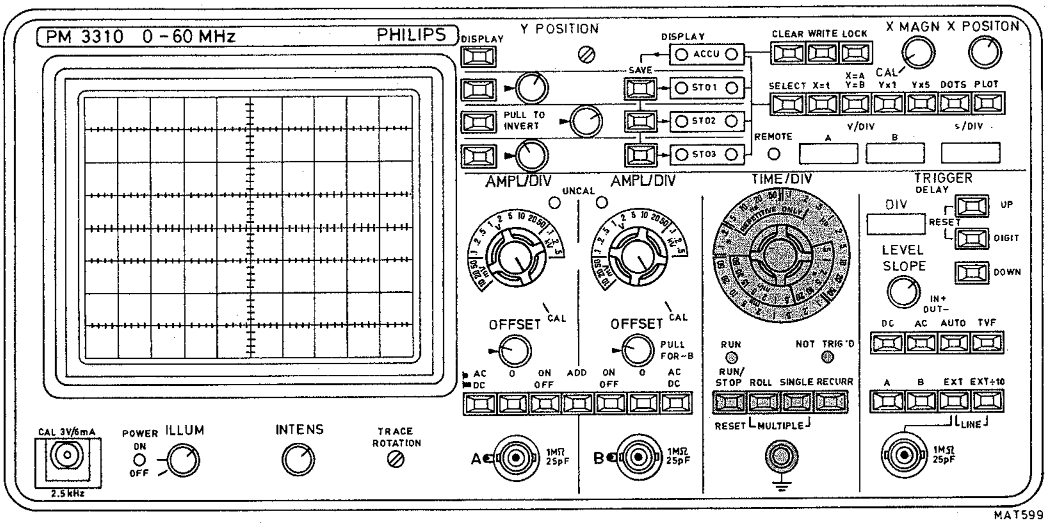
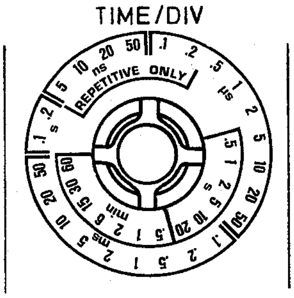


Fig. 3.3.



Time coefficient step control of the time-base:
24-way rotary switch (without stop).
The selected position is indicated by one of the indicator lamps located under the scale of this knob. In the positions marked with REPETITIVE ONLY, signals of a repetitive character may be measured only.

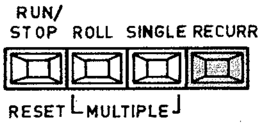
The inner scale ring is for ROLL mode only, and is automatically indicated by selecting ROLL mode.
The correct display of the input signal on the CRT screen can be found by turning the TIME/DIV switch from fast to slow (starting at position 0.5 ns/DIV) until the first triggered display is obtained.

RUN

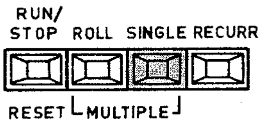
Pilot lamp indicating that the ROLL mode is operative and running.
This lamp blinks to indicate that the ROLL mode action is completed. (See also description "ROLL" function).

NOT TRIG'D

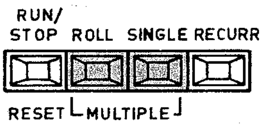
Pilot lamp indicating that there is no trigger signal present.
No light means:
A). In ROLL/RECURR mode: Time-base is triggered.
B). In SINGLE/MULTIPLE mode: Indicates that signal(s) is (are) captured.



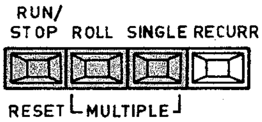
With RECURR depressed, the ACCU memory only is constantly overwritten by new information. This action occurs at particular time intervals depending on the position of the TIME/DIV and the trigger delay setting.



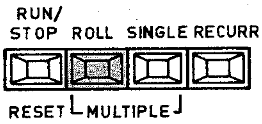
With SINGLE depressed, refreshment of the ACCU memory contents takes place only once, when the trigger level is reached and the time set with the trigger delay has elapsed.
This refreshment takes place only after pressing the RESET pushbutton. The signal is started according to the position of the trigger delay. During the waiting time, the accumulator contents are displayed and lamp NOT TRIG'D is ON.



With both ROLL and SINGLE pushbuttons depressed, the MULTIPLE mode is selected.
The SINGLE action occurs four times after pressing the RESET pushbutton once.
The first result is stored in the memory STO 3,
the second result in memory STO 2,
the third result in memory STO 1, and
the last result in the ACCU memory.



If SINGLE or MULTIPLE is selected, the time-base can be started again by pressing the RESET button.

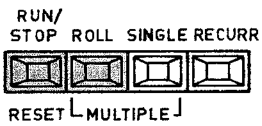


With ROLL depressed, the signal is built-up point-by-point at the right-hand side of the screen and moves to the left, after depressing the R/S button.
The RUN lamp indicates that the ROLL mode is operative.

When the accumulator is completely filled, the information is saved in memory STO 3, the next information in memory STO 2, the next in memory STO 1 and the last information in the ACCU memory (the RUN lamp will be ON continuously).
After this, the ROLL mode stops and the RUN lamp blinks to indicate this condition.

The ROLL mode may be used in the positions 0.5 sec/div up to 60 min/div indicated by the inner-ring indicator lamp of the TIME/DIV switch. If the TIME/DIV switch is set to an out-of-range position, this will be indicated by a flashing indicator lamp in the outer-ring of the TIME/DIV switch. In these positions, ROLL mode is still continued but in 0.5 s/div.

The total information will only be visible on the CRT screen after depressing the four display push-buttons for the ACCU, STO 1, STO 2 and STO 3.



By pushing the CLEAR button, the contents of the ACCU memory will be cleared and the ROLL mode action can be restarted by pushing the RUN/STOP switch. (See also display section).

During the ROLL mode action (i.e. while the RUN lamp is continuously ON) the action can be stopped and/or started by pressing the RUN/STOP pushbutton.

With the ROLL mode stopped by pressing RUN/STOP, the start/stop function of this pushbutton can be taken over by a signal applied to the EXT trigger input (TTL level):
+5 V ($>$ +2,4 V) logic HIGH means RUN.
0 V ($<$ 0,8 V) logic LOW means STOP.

Note: To simplify operation, with all pushbuttons released, RECURR is automatically selected.

Measuring earth socket.

3.3.4. Triggering

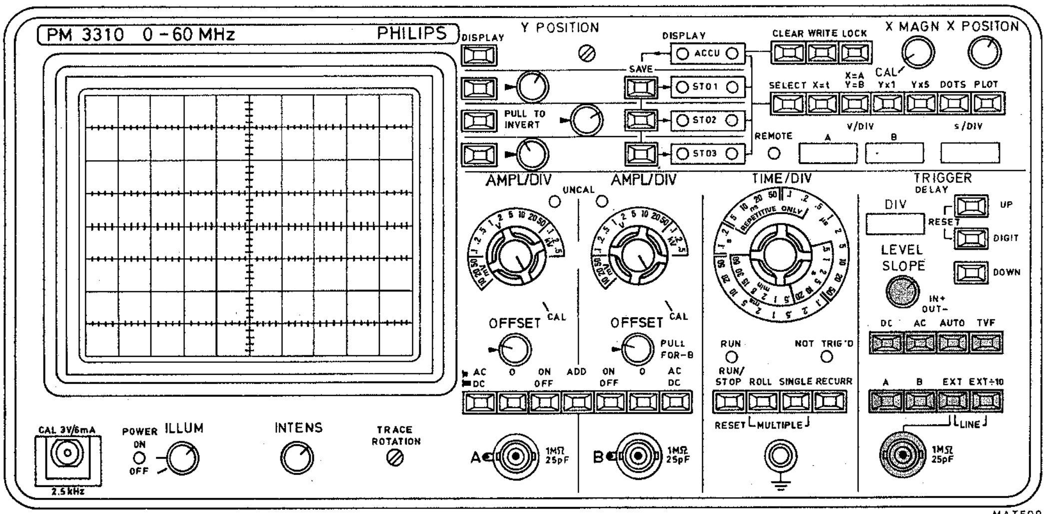


Fig. 3.4.

LEVEL
SLOPE

Continuously variable control for selecting the level of the trigger point on the input signal.

This control incorporates a push-pull switch that enables choice of triggering on either the positive or the negative-going edge of the triggering signal (IN +, OUT –).

Trigger Mode Selection

DC AC AUTO TVF

With DC depressed, the time-base generator is triggered by a trigger signal including DC.
(Trigger bandwidth DC ... 60 MHz).

DC AC AUTO TVF

With AC depressed, the time-base generator is triggered by a signal of which the DC component is blocked.
(Trigger bandwidth 10 Hz ... 60 MHz).

DC AC AUTO TVF

With AUTO selected, the time-base is free-running in the absence of trigger signals. (The DC component is blocked in this mode and the trigger bandwidth is 20 Hz ... 60 MHz).

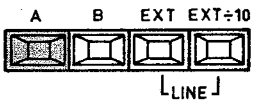
DC AC AUTO TVF

By selecting TVF, television frame signal synchronisation is obtained (For CCIR system 625 lines). *

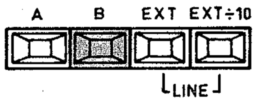
Note: To simplify operation , with all pushbuttons released the AUTO mode is selected.

* Check the correct setting of the trigger slope (in accordance to the T.V. system under test).

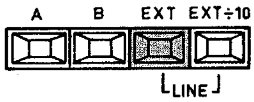
Trigger source selection



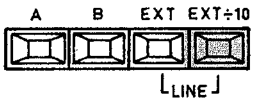
With A depressed, triggering is achieved on a signal internally derived from channel A.



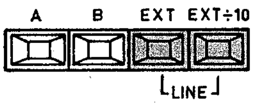
With B depressed, triggering is achieved on a signal internally derived from channel B.



With EXT depressed, triggering is from an external signal via the adjacent EXT trigger 1 M //25pF input socket.

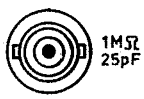


With EXT ÷ 10 depressed, external triggering is obtained as above but via a built-in 10:1 voltage divider.



With both the EXT and the EXT ÷ 10 buttons depressed, triggering is achieved by a signal internally derived from the line (mains) voltage.

Note: To simplify operation, with all pushbuttons released, A is automatically selected.



BNC input socket for external triggering or external RUN/STOP signal for ROLL mode.

3.3.5. Trigger delay

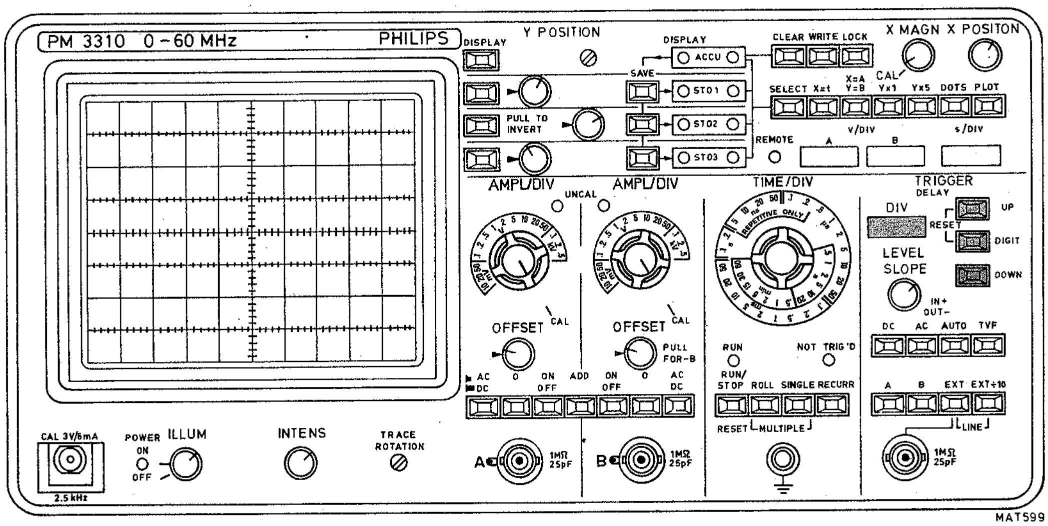
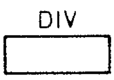


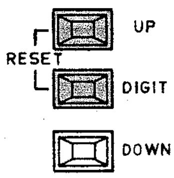
Fig. 3.5.



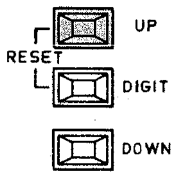
A four-decade display indicating the selected time in divisions between the trigger pulse and the beginning of the displayed signal on the CRT.
This trigger delay time can be varied between –9 and +9999 divisions in the 0.2 s to 0.5 μs/div positions of the TIME/DIV switch.
In positions 0.2 μs to 5 ns/div of the TIME/DIV switch (for repetitive signals only) the delay time range is 0 ... 100 divisions.

When switching on the instrument, the display is automatically reset to zero, except with memory back-up, where the previous value will be displayed.

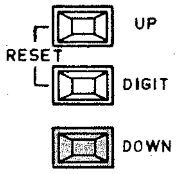
In the ROLL mode the next "OFF" will be displayed.



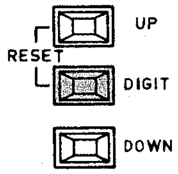
With both the pushbuttons UP and DIGIT depressed, the trigger delay time is reset to zero. This will be indicated in the DIV display.



The trigger delay time can be increased by pressing the UP pushbutton.



The trigger delay time can be reduced by pressing the DOWN pushbutton.



The decade in which counting occurs when pushbuttons UP or DOWN are operated, can be selected by pressing DIGIT. The selected digit is flashing in the DIV display.

By pushing DIGIT repeatedly, scrolling is selected; i.e. the digits run from the least-significant to the most-significant decade and then restart again at the least-significant decade.

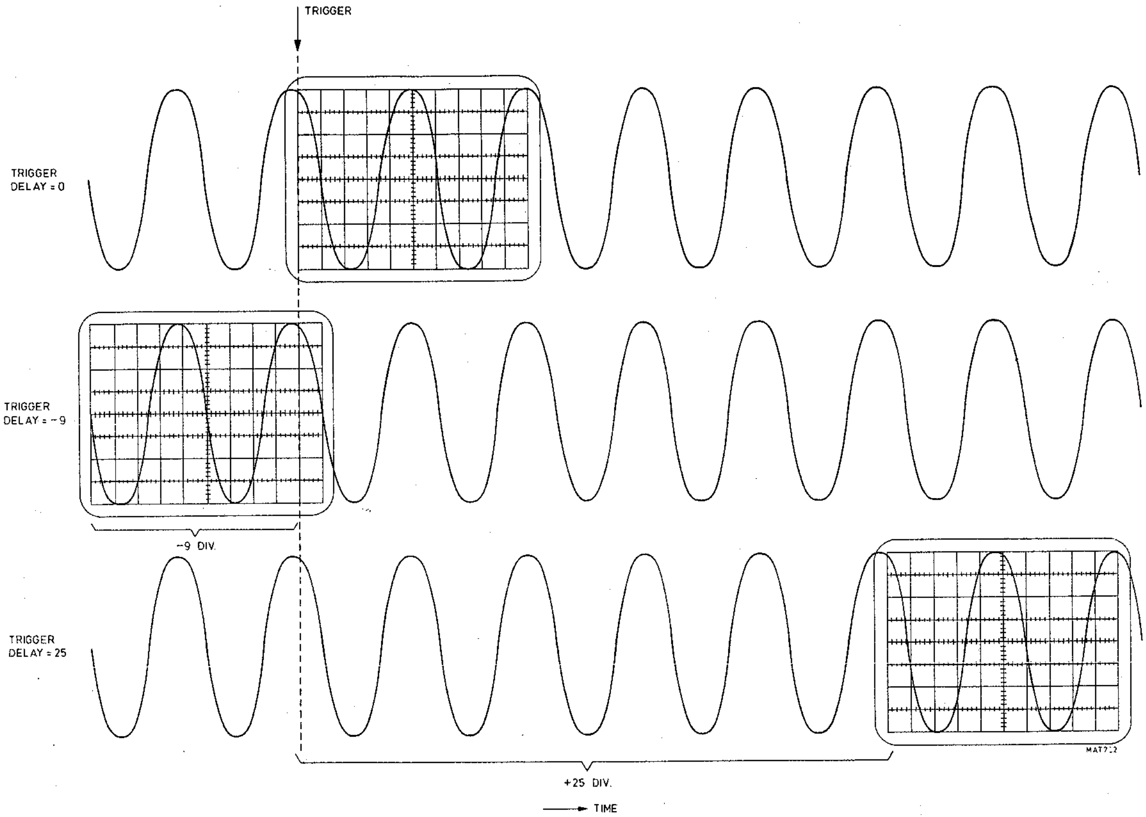


Fig. 3.6.

3.3.6. Display section

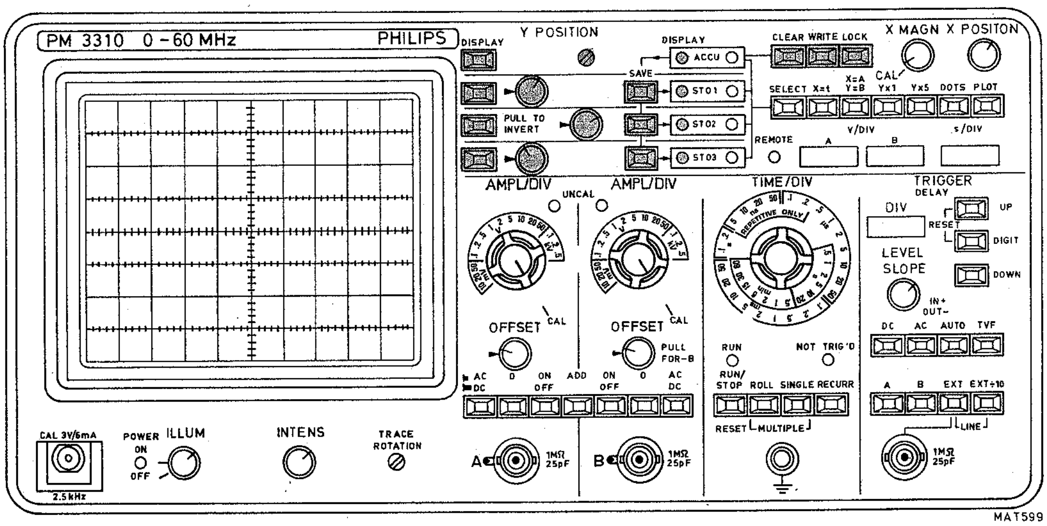
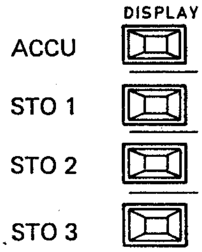
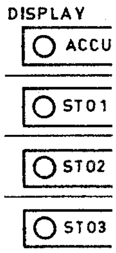


Fig. 3.7.

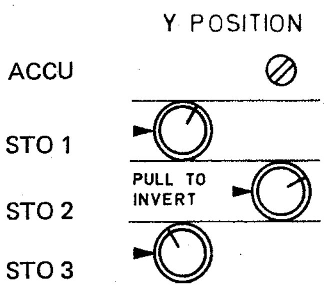


Depending on the settings of the four DISPLAY pushbuttons, the contents of one or more of the four memories ACCU, STO 1, STO 2, and STO 3 can be selected for display on the CRT screen.

With no DISPLAY pushbutton depressed, the ACCU LED indicates that the accu memory is selected. This can be influenced by pressing the SELECT pushbutton. In the case when all the DISPLAY pushbuttons are released, the memory that was last switched off is selected.



These pilot lamps indicate which memories are selected for display on the CRT screen by choice of DISPLAY pushbuttons or by the SELECT pushbutton when all DISPLAY buttons are released.



Continuously variable controls giving vertical shift of the display.
In the position marked  the channels are equally spaced over the whole screen area. Each channel occupies two divisions of the screen (see figure).
The ACCU positions control is screwdriver operated.

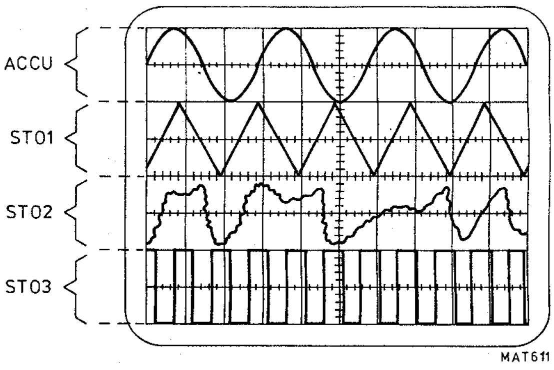


Fig. 3.8.

PULL TO INVERT

A two-way push-pull switch integrated with the STO 1, STO 2 and STO 3 POSITION controls for inversion of the signals on the CRT screen.
These controls are depressed for normal and pulled for invert (PULL TO INVERT).

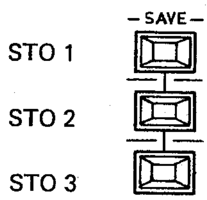
On pressing the CLEAR pushbutton the contents of the ACCU memory are cleared.
The other three memories can only be cleared by transferring the cleared memory contents of the ACCU into these memories. (Refer also to the function of the SAVE pushbuttons).

The ROLL mode action can be restarted by pushing the CLEAR pushbutton and then the RUN/STOP button.

With the WRITE pushbutton depressed, the input signal will be written into the ACCU memory after a trigger pulse and after passing the preset delay time.
(See also Section 3.3.4. Triggering).

With the LOCK pushbutton depressed, the whole memory system is locked, which means that the contents of ACCU, STO 1, STO 2 and STO 3 cannot be changed in this mode.

Note: For simplicity of operation, with all pushbuttons released, WRITE mode is automatically selected.



The contents of the ACCU memory are saved in the selected register STO 1, STO 2 or STO 3 by depressing the relevant pushbutton.
At the same moment, the information giving the settings of the channel A and B AMPL/DIV, the TIME/DIV and the trigger delay controls, is all stored in the internal memory of the instrument for alpha-numerical display purposes.
(See also V/DIV and s/DIV display).

3.3.7. AMPL/DIV and TIME/DIV switch settings

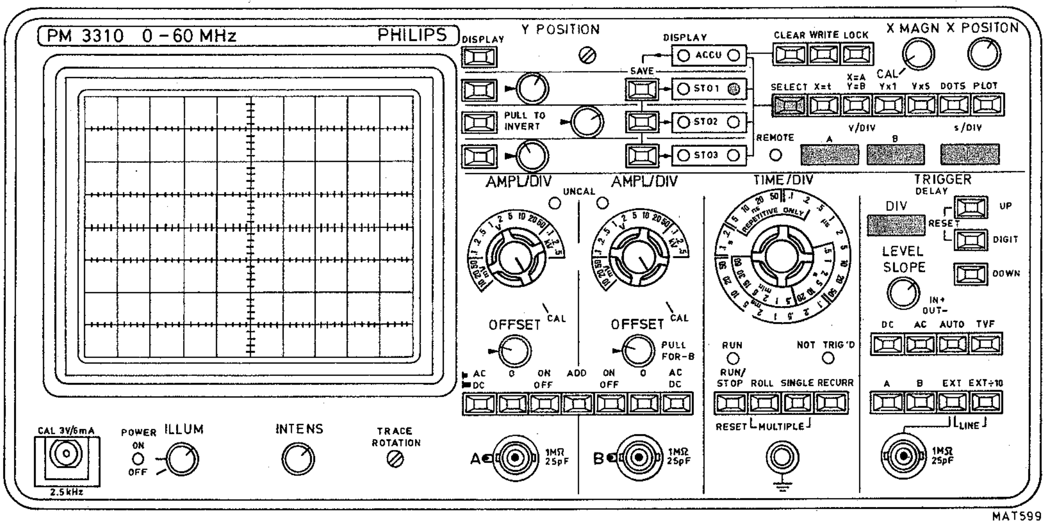
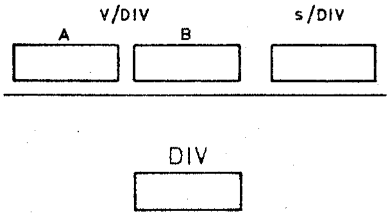
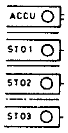


Fig. 3.9.



The displays indicate the settings of the AMPL/DIV and TIME/DIV switches and trigger delay settings appropriate to the register indicated by one of the pilot lamps:



To display the switch settings corresponding to one of the four memories, operate the SELECT button. Memories not displayed will be skipped.

The display shows a mantissa (decimal part) and a ten's exponent.

This exponent can be:

- Blank (0) to indicate Volts or seconds
- –3 for mV or ms
- –6 for μs
- –9 for ns

A * in the display indicates that the relevant AMPL/DIV continuous control was not in the CAL position during the storage of signals into one of the memories, so the display shows a more sensitive range than in calibrated position.

Other display possibilities are:

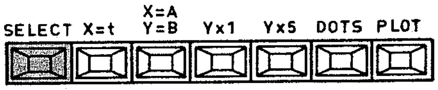
ADD: ADD mode was operating.

SUB : SUB mode was operating (ADD with channel B inverted).

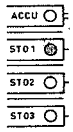
OFF : the relevant channel was not operating.

NOP : the relevant setting is not of interest; (e.g. after switch-on when no battery back-up is in use).

Note: In the ADD and SUB mode it is recommended to set both A and B AMPL/DIV switches in the same position in order to interpret the stored signal correctly.



The SELECT pushbutton enables selection of the memory of which the scale factors are to be displayed.
In this mode, the system scrolls between those memories selected by the DISPLAY pushbuttons.
The memory selected at any particular time is indicated by the relevant pilot lamp.



If one or more of the contents of the memories STO 1 - STO 2 - STO 3 is displayed on the CRT in combination with the ACCU memory contents, the alpha-numeric display is automatically switched to the ACCU settings by operating one of the control switches shown in the figure below.

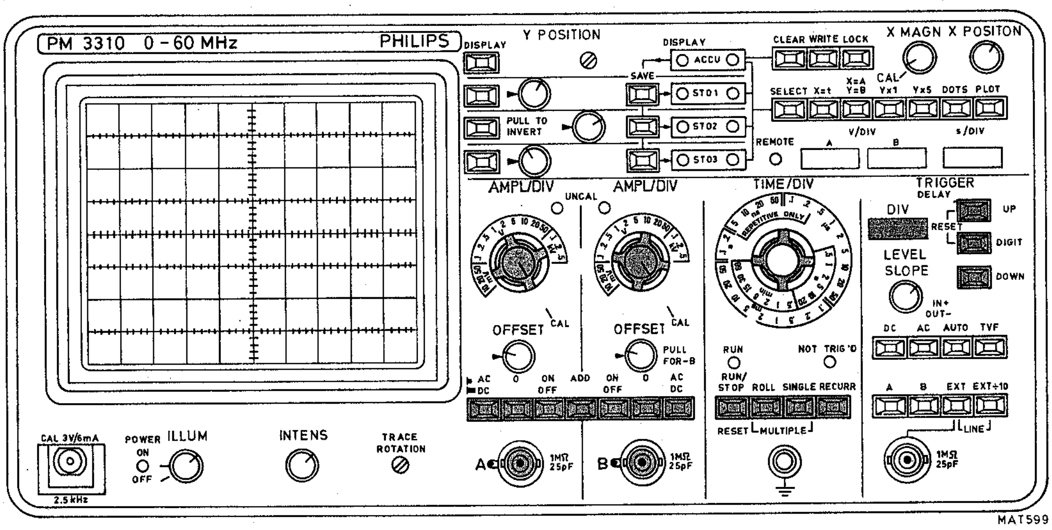
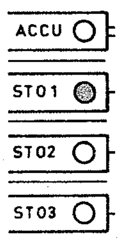


Fig. 3.10

With no DISPLAY pushbuttons depressed, use of the SELECT pushbutton results in scrolling of:

- the screen trace
- the pilot lamps
- the scale-factor displays.

The SELECT pushbutton is also functional in the PLOT mode.
(See Section 3.3.8. Display modes).



These pilot lamps indicate the particular memory to which the scale factors and trigger delay settings in the V/DIV, s/DIV and DIV displays relate.

Only one of the pilot lamps in ON at a time.

3.3.8. Display modes

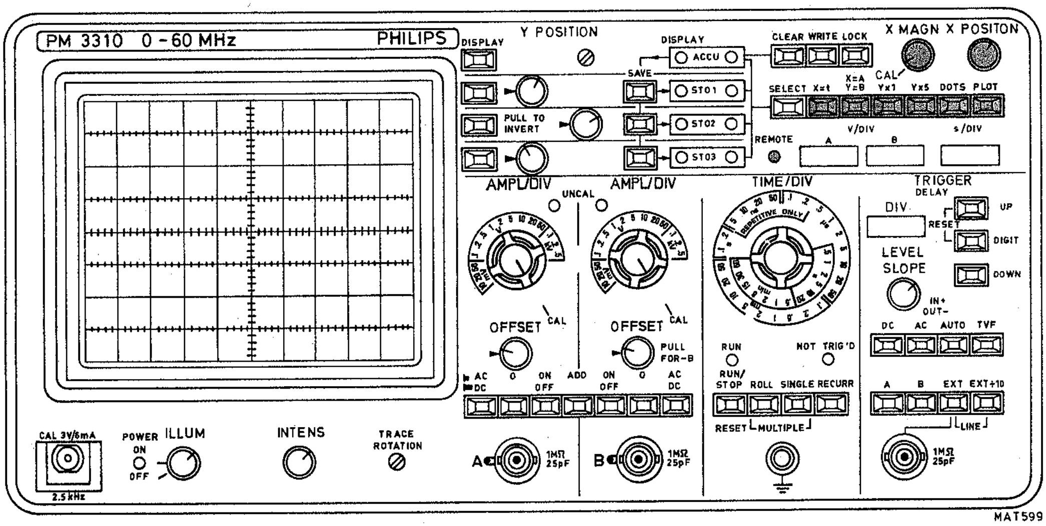
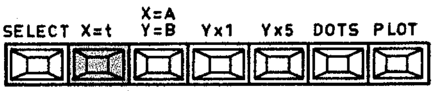
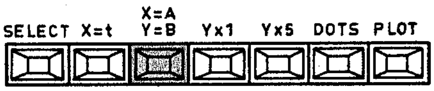


Fig. 3.11.

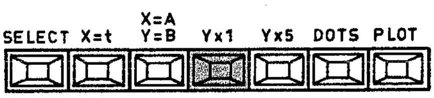


X = t display derived from the original setting of the time-base. (Information from memory).

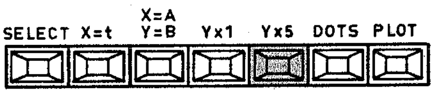


X/Y display from the A and B inputs.

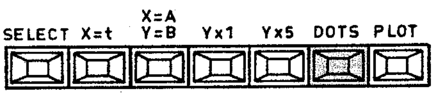
The A and B signals are used for horizontal and vertical deflection respectively.
A picture of 10 x 2 divisions is displayed.
When the Y x 5 mode is selected, a picture of 10 x 10 divisions can be obtained, of which 10 x 8 divisions can be displayed on the CRT screen.



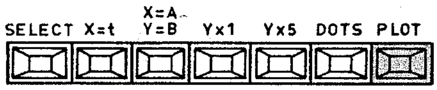
Vertical deflection coefficient x1.



Vertical deflection coefficient x5.
In this mode, the scale factor in the V/DIV display is also modified (divided by a factor of 5). The displayed memories are also displayed now over 10 vertical divisions. The zero lines, if correctly adjusted, are located at the same base-line.



With this pushbutton depressed, normal display (dot-join) is changed into a display of discrete dots.



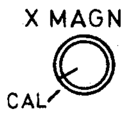
With the PLOT pushbutton depressed, output signals are available on the rear panel for plotting on an X/Y recorder or an X(t) recorder.
The memory containing the information to be plotted, can be chosen with the SELECT button.

When plotting in the A & B mode, the B plot is started after the A plot. An intensified dot on the CRT display indicates the progress during plotting.

For output voltages of X, Y and PEN LIFT see Section 3.3.9.
In order to make manual pen-positioning possible, a delay of about three seconds before, and six seconds after the plot sequence is provided. The complete plotting time is approx. 100 sec.

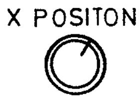
After the PLOT pushbutton is depressed again, the PLOT action stops.

Note: For simplicity of operation, with all pushbuttons released, X = t and Y x 1 are automatically selected.



Continuous horizontal x2.5 magnifier.

Note: There is no expand in the CAL position, and no indication in the s/DIV display.



Continuous control for horizontal shift of the trace on the screen.

Pilot lamp indicating that the IEC-bus overrules all the front-panel control settings.

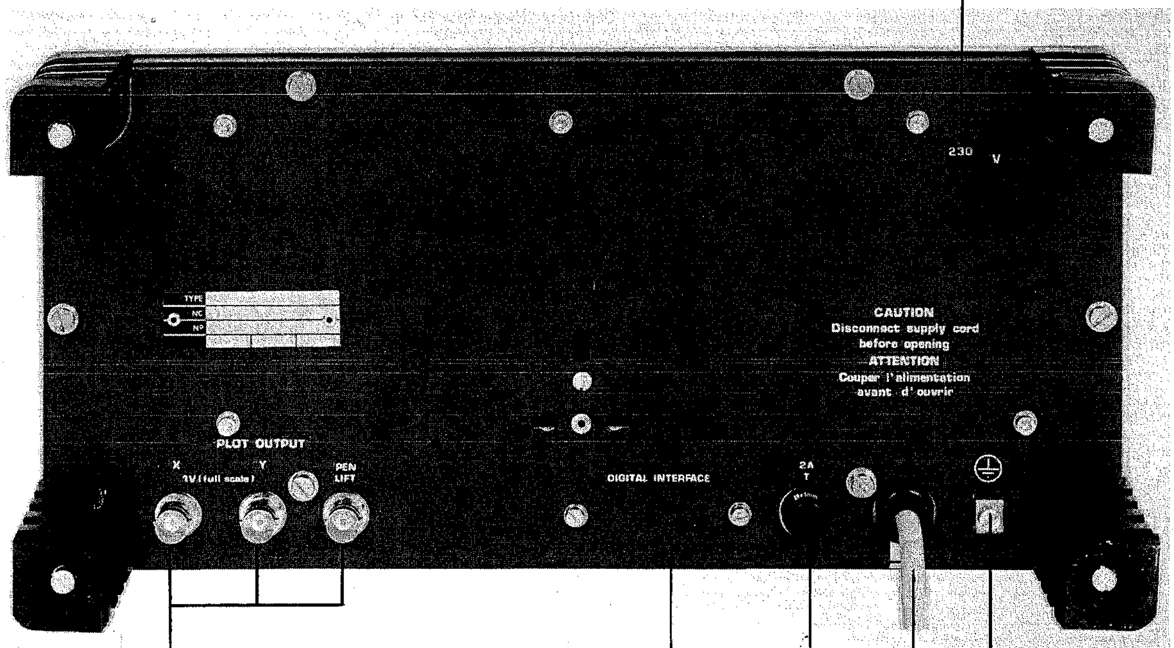
Resetting to "local" only can be provided from the IEC-bus controller or by switching the instrument off and on.

This facility only functions in instruments that are provided with the IEC-bus option PM 3325. Settings and outputs can then be controlled by other instruments external to the oscilloscope.
(Refer to the appropriate section of the Service Manual for mounting instructions and protocol of IEC-bus operation).

3.3.9. Rear panel

Mains adaptor switch set for 115 V (100 ... 120 V ±10 %)

Mains adaptor switch set for 230 V (220 ... 240 V ±10 %)



MAT 633

Protective earth terminal

Mains cable

Mains fuse-holder (Fuse 2 A delayed-action)

Cut-out for an IEC-bus socket (socket delivered with the IEC-bus option PM 3325)

X-Y and PEN LIFT outputs to connect a recorder to the oscilloscope

- The X output generates 1 V (full scale), i.e. 0.1 V per CRT screen division
- The Y output generates 1 V (full scale), i.e. 0.5 V per CRT screen division
- The PEN LIFT output is an open collector output with a maximum load: $U_{0L} < 0.5$ V at 500 mA continuous and switches the output to zero (TTL compatible)

Fig. 3.12.

3.4. DETAILED OPERATING INFORMATION

3.4.1. General

Before switching on, ensure that the oscilloscope has been correctly installed in accordance with the instructions given in Section 2, and that the various precautions outlined have been observed.

The following procedure gives a general indication of whether the oscilloscope is functioning correctly and provides a suitable starting routine before any measurements are made.
The procedure is especially useful for operators who are not familiar with this type of oscilloscope.

This instrument offers the facility to store a signal of channel A and a signal of channel B (including the AMPL/DIV and TIME/DIV, and trigger delay settings relating to these signals) in one of four internal memories: ACCU, STO 1, STO 2, or STO 3, depending on selection.

In the normal mode (Y x 1), 2 divisions are available for each memory as shown. With the POSITION controls at mid-range position, the display format is typically as shown in the diagram.

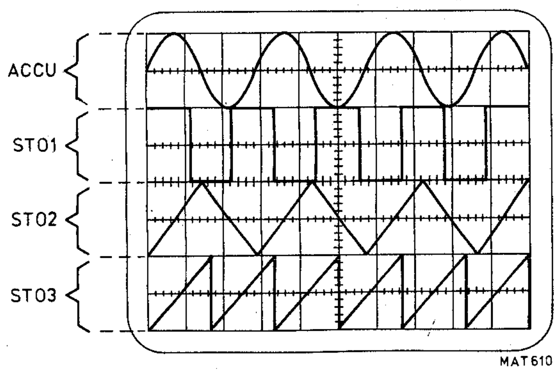


Fig. 3.13.

3.4.2. Displaying ACCU contents

To display the contents of the ACCU the following settings are necessary:

– No input signals connected.
– All pushbuttons released and all switches in the CAL position.

The following functions will now be operative

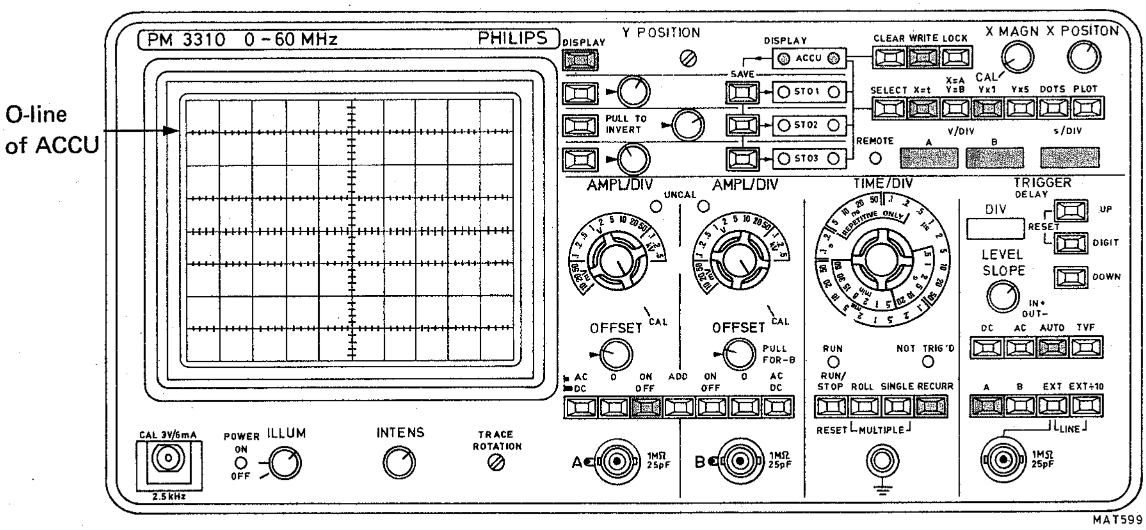


Fig. 3.14.

– Set POWER switch to ON. Check that pilot lamp is ON and that the power-up test starts. (See Section 3.2.2.).

A trace will now appear within the upper two divisions of the screen.

– Set the INTENS control for a suitable trace intensity.
– Adjust the OFFSET control of the A channel so that the displayed baseline coincides with the 0-line of the ACCU display part.

The oscilloscope is now ready to accept an input signal, but before continuing it is advisable to depress the pushbuttons as indicated in figure (view of controls).

Connect a sine wave signal to input A and set the TIME/DIV switch to a suitable position.

The correct display of the input signal on the c.r.t. screen can be found by turning the TIME/DIV switch from fast to slow (starting at position 5 ns/div.) until the first triggered display is obtained.

Note 1: *The AMPL/DIV switch of the A channel should be adjusted so that the input signal covers not more than two divisions of the screen.*
To indicate an overflow or incorrect OFFSET adjustment, the signal blinks until a correct setting is made.

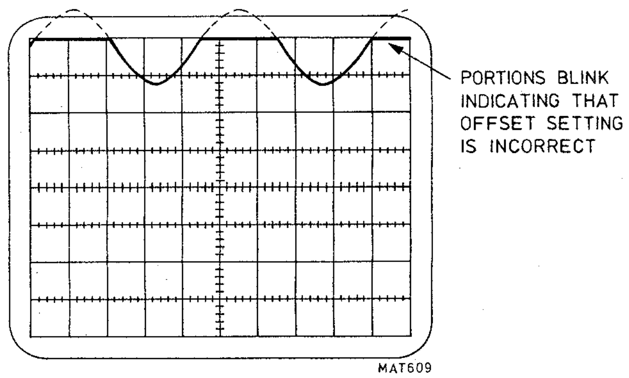


Fig. 3.15.

Note 2: *To obtain full screen display depress Y x 5 pushbutton.*
The zero line is then automatically located on the centre-line of the screen.

Note 3: *If both channel A and channel B are ON and input signals are connected to both channels, the traces will be superimposed.*

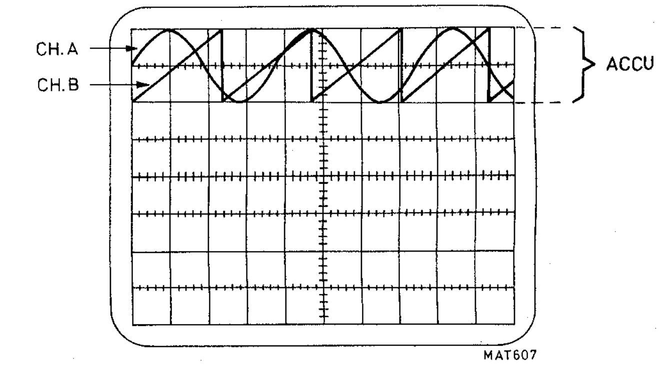


Fig. 3.16.

In this event, it is possible to adjust the AMPL/DIV switch and the OFFSET controls of channels A and B so that in the normal mode (Y x 1) each trace occupies one division.

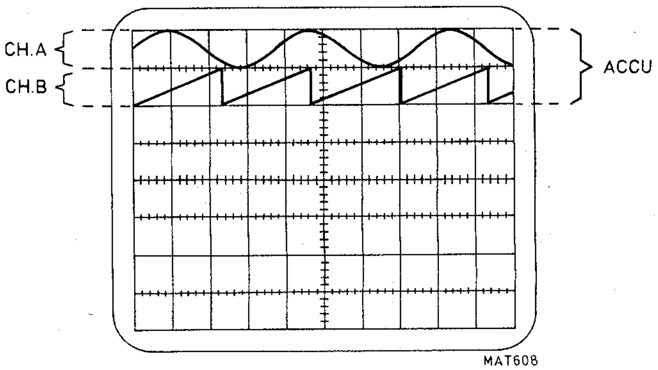


Fig. 3.17.

Note 4: *If one or more of the other DISPLAY push-buttons are depressed, there are two possible situations:*

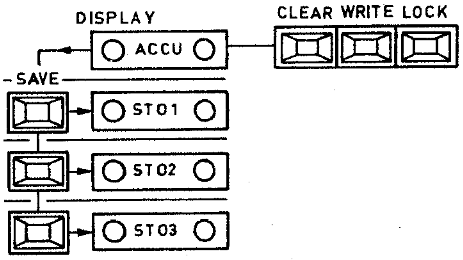
1. *When battery back-up is used, the contents of the associated memory (or memories) are displayed; i.e. the memory contents prior to switching off the instrument.*
2. *Without battery back-up, the CRT displays irrelevant information and the alpha-numeric display will indicate:*

V/DIV A	V/DIV B	s/DIV
NOP	NOP	NOP

DIV
NOP

3.4.3. Storing ACCU contents

The procedure for storing the ACCU contents in one of the memories STO 1, STO 2 or STO 3 is now described.
The memories STO 1, STO 2 and STO 3 are only able to store the contents of the ACCU.



- Depress the SAVE button of the memory chosen for storing the ACCU information.
- Verify that the information is written into the memory by pressing the DISPLAY button of that memory.

  The contents will now be displayed on the CRT screen.

A memory can be cleared (in WRITE mode only) by clearing the ACCU with the CLEAR pushbutton and then storing the cleared ACCU contents in that memory by pressing the relevant SAVE button. In other words, clearing a memory by storing blank ACCU contents.

3.4.4. Using the SELECT pushbutton

The functions of the SELECT pushbutton are:

a. To select the memory holding the settings V/DIV, s/DIV and DIV (delay) that have to be indicated.
b. To select the memory holding the contents to be plotted.
c. If no DISPLAY pushbutton is depressed, SELECT initiates scrolling of the displayed memories, the pilot lamps and the settings V/DIV, s/DIV and DIV (delay).

Note: – *If only* ***one*** *DISPLAY button is depressed, pushing SELECT has no visible effect.*
– *If two or more DISPLAY buttons are depressed, pushing SELECT causes the system to scroll the pilot lamps and the information in the V/DIV, s/DIV and DIV (delay) indicator.*

With pushbutton LOCK it is possible to keep all the memory contents unchanged.

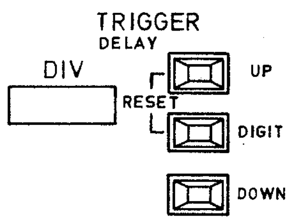
3.4.5. Trigger delay

a. Positive delay

The trigger delay enables the time (in divisions) between triggering and the start of the CRT display (left-hand side) to be chosen.

EXAMPLE: Suppose the 6th line in a TV pattern is desired (TV line = 64 μs).
Required trigger delay is therefore 5 x 64 μs = 320 μs.
i.e. after 5th line has passed.

Procedure:



- Select TVF.
- Set TIME/DIV switch to position 10 μs/DIV.
- Depress UP until the least-significant digit displays 2
- Depress DIGIT once.
- Depress UP until the second digit displays 3

A delay of 32 x 10 μs between frame pulse and the left-hand side of the CRT display is now obtained.
This results in displaying the information of the 6th line.

b. Negative delay

While the oscilloscope continuously stores information in the shift register it offers the capability of pre-triggering.
In effect, this means that a portion of the signal preceding the trigger point can be shown on the CRT display.
The trigger point can be chosen on any division of the CRT screen (0 to 9 divisions).

If the TIME/DIV switch is set to another position, the setting of the trigger delay (in divisions) will be automatically changed (recalculated) and displayed.

The result of this recalculation is to round off downwards to whole divisions (integers).

The starting point of recalculation is the momentary displayed number of divisions.

Note 1: The preset TRIGGER DELAY at a certain TIME/DIV switch position is internally stored and will always be the same preset delay, independent of the round off faults of operating the TIME/DIV switch.

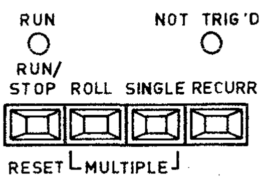
	first example		second example	
TIME/DIV	DIV	DIV	DIV	DIV
Set position → 5 μs	0095	0095	0095	0095
	1 ↓	12 ↑	1 ↓	10 ↑
10 μs	0047	0000	0047	0040
	2 ↓	11 ↑	2 ↓	9 ↑
20 μs	0023	0000	0023	0020
	3 ↓	10 ↑	3 ↓	8 ↑
50 μs	0009	0000	0009	0008
	4 ↓	9 ↑	4 ↓	7 ↑
. 1 ms	0004	0000	0004	0004
	5 ↓	8 ↑	5 ↓	6 ↑
. 2 ms	0002	0000	0002	0002
	6 ↓	7 ↑		
. 5 ms	0000	0000		
	range down	range up	range down	range up

Note 2: If by operation of the TIME/DIV switch a TRIGGER DELAY of "0" is reached, all lower positions will show a TRIGGER DELAY of "0".

The trigger delay is switched OFF in the ROLL mode, the indicator (DIV) then shows OFF

3.4.6. Single and multiple modes

When pushbutton SINGLE is depressed, the ACCU is refreshed once after a trigger pulse and delay, as also the accu display.
If the instrument is waiting for a trigger pulse, the pilot lamp NOT TRIG'D will light.



When both the ROLL and SINGLE pushbuttons are depressed, the SINGLE action is repeated four times. This is called the MULTIPLE mode. The result of the first action is stored in the memory STO 3, the second result is stored in STO 2, the third in STO 1 and the fourth in the ACCU.
When either the SINGLE or the MULTIPLE action is completed, the same mode can be chosen again by pressing the RESET button.

3.4.7. ROLL mode

The ROLL mode is typically used for very low frequency signals and is effective with TIME/DIV settings from 0.5 s ... 60 min. The signal is built-up point-by-point from the right-hand side of the CRT screen and "writes" towards the left. If ten divisions of the screen are built-up in the ACCU memory, then the SAVE action is started automatically, the contents of the ACCU being saved in memory STO 3.

Roll-mode action can be started by selecting ROLL and pushing pushbutton RUN/STOP once.

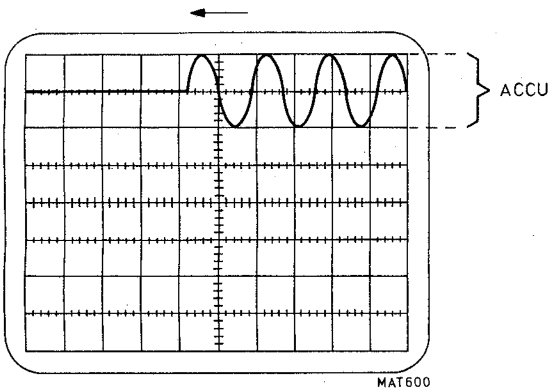


Fig. 3.18. Build-up of first information in the ACCU

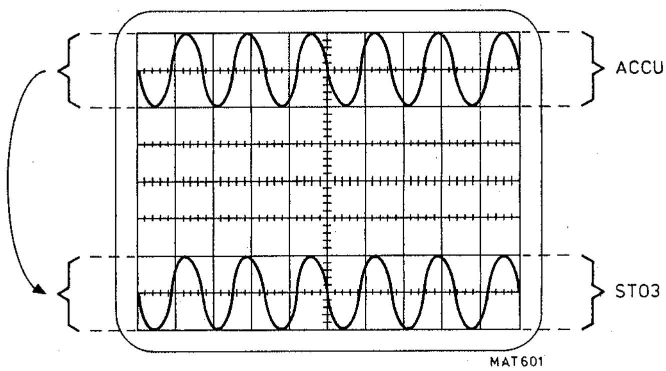


Fig. 3.19. First SAVE action

New information is now built-up in the ACCU memory point-by-point and after completion (ten divisions), the new information will be stored in memory STO 2.

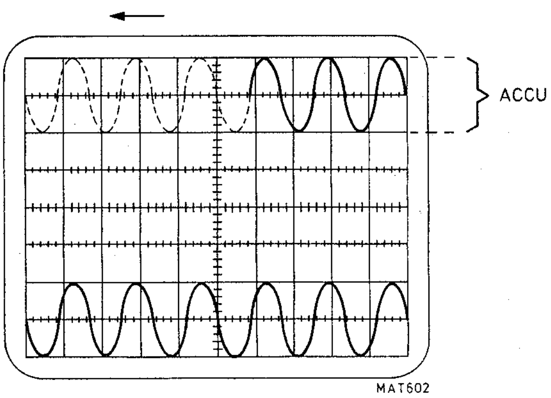


Fig. 3.20. Build up of second trace information in ACCU

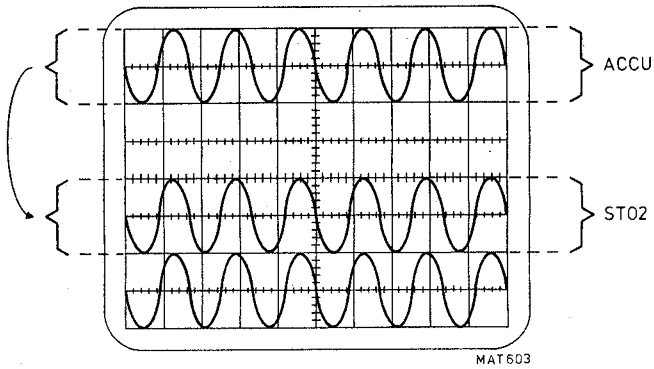


Fig. 3.21. Second SAVE action

The third information trace built-up in the ACCU is stored in STO 1 as shown below.

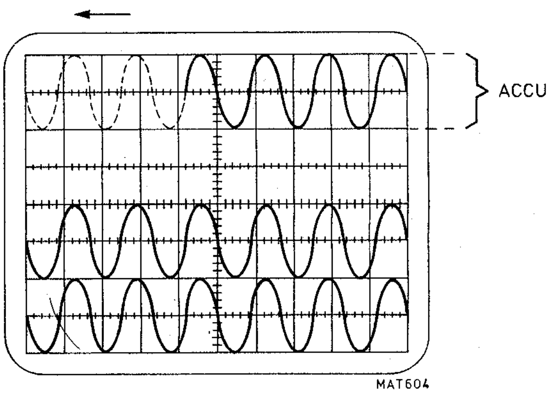


Fig. 3.22. Build-up of third trace information in the ACCU

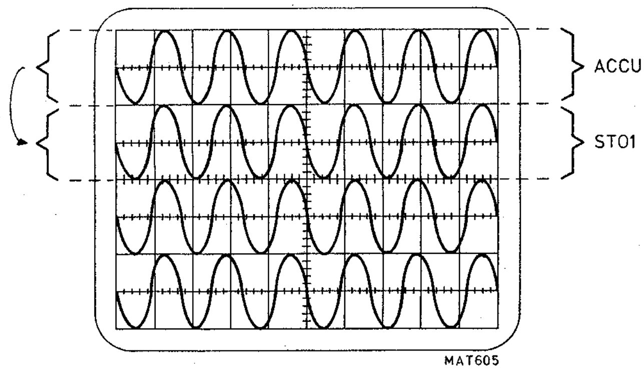


Fig. 3.23. Third SAVE action

The last information is stored in the ACCU itself as shown below.

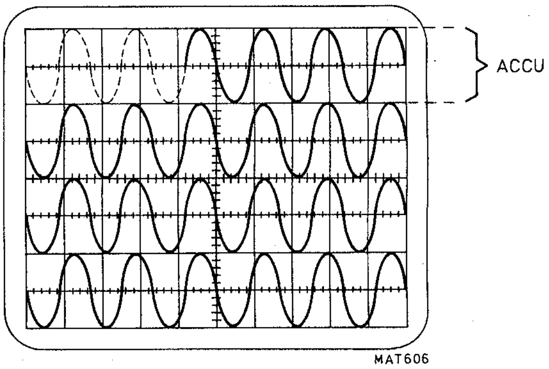


Fig. 3.24.

During the ROLL mode action, the RUN indicator lamp will light continuously and after completion of the action the lamp will flash. If during the ROLL mode action an interruption is necessary, then depress the RUN/STOP pushbutton. The ROLL mode is interrupted and the RUN indicator lamp will be extinguished. This action can also be effected by an external d.c. signal at TTL level, only if the ROLL-mode is stopped by operating the RUN/STOP button.

TTL = 1 → RUN TTL = 0 → STOP

By again depressing the RUN/STOP button the ROLL mode action is continued.
When the ROLL mode action is completed (flashing RUN light), the action can be restarted by pushing the CLEARbutton followed by the RUN/STOP button.

3.4.8. Plotting

- Connect the X, Y and PEN LIFT outputs of the oscilloscope to the recorder.
  The X output generates 0.1 V per CRT division (1 V per full scale).
  The Y output generated 0.5 V per CRT division (1 V per full scale).
  The PEN LIFT output is an open collector output with a maximum load of 500 mA continuous and switches the output to zero; it is TTL compatible.
- Press the SELECT pushbutton to select the memory containing the information to be plotted.
- Press the PLOT pushbutton to start the plot action, which is also visible on the CRT screen by an intensified point moving over the selected trace from left to right.
  The plot action can be interrupted by pressing the PLOT button once more.

If no automatic pen lift is available, manual pen up-pen down operation can be achieved as follows:

- Depress PLOT.
- Wait 2 seconds.
- Push pen down (after 1 second the plot action will start).
- Lift pen after the signal is plotted.
- In dual channel operation the pen will move after 6 seconds to the starting point of the second channel.
- Push pen down.
- Lift pen after the second channel is plotted.

Note 1: *During plotting, the oscilloscope is in the lock-mode, which means that the contents of all memories cannot be changed.*

Note 2: *In case of channel A and B plotting first channel A will be plotted and then channel B.*

Note 3: *The PLOT operation is provided with a delay of 3 seconds at the start and end of the action to give sufficient time for manual pen positioning.*

3.4.9. Adjustment of attenuator probes

- Connect the compensation box to socket A and place the tip of the probe on the CAL socket.
- Push Y x 5.
- Select an appropriate setting of the AMPL/DIV switch of channel A.
- Insert a small screwdriver through the hole in the compensation box and adjust the trimmer to obtain a correct display as shown in Fig. 3.25.

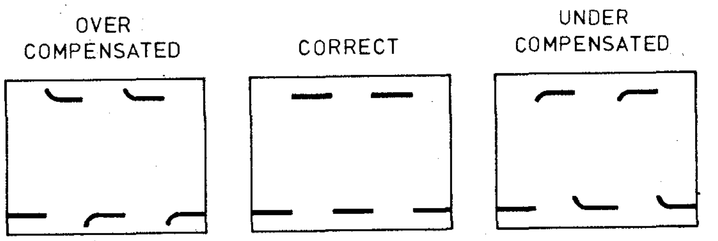


Fig. 3.25.

3.4.10. Differential mode

The A-B mode can be selected by depressing ADD and pulling the channel B OFFSET control.
In measurements where signal lines carry substantial common-mode signals (e.g. hum), the differential mode will cancel out these signals and leave the remainder of interest (A-B). The capability of the oscilloscope to suppress common-mode signals is given by the CMR factor (see Fig. 3.26).

To obtain the degree of common-mode rejection as specified, channel A and B gains must first be equalised. This can be done by connecting both channels to the CAL output connector, and adjusting one of the continuous controls with the AMPL/DIV switch for minimum deflection on the screen.

When passive 10:1 probes are used, a similar equalisation process is recommended by adjusting their compensating controls for minimum deflection.

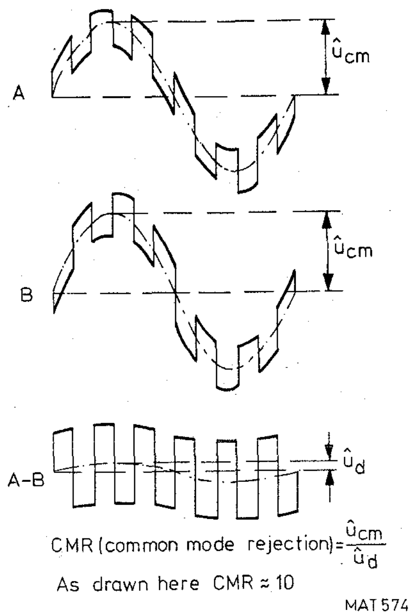


Fig. 3.26.

3.4.11. X = A and Y = B

In this mode the signal is built up point by point. This means that the dot join circuit is switched off automatically.

Procedure:

- Connect input signals to both channel A and channel B input sockets.
- Set the AMPL/DIV switches to an appropriate position.
- Depress X = A.
  Y = B.

  Horizontal deflection is now determined by the channel A input and vertical deflection by the channel B input.

4. BRIEF CHECKING PROCEDURE

4.1. GENERAL INFORMATION

This procedure is intended to check the oscilloscope using a minimum of test steps and actions.
It is assumed that the operator performing this test is familiar with oscilloscopes and their characteristics.

WARNING: Before switching on, ensure that the oscilloscope has been installed in accordance with the instructions outlined in Section 2.

If this test is started a few minutes after switching on, bear in mind that test steps may be out of specification, due to insufficient warming-up time. To avoid this situation, allow the specified warming-up time.

The test should be performed at an environmental temperature of 20 - 30 ^{o}C.

All the checks in this procedure can be made without removing the instrument's top and bottom covers.

For a complete check of every facet of the instrument's calibration, refer to the section Checking and Adjusting Procedure and omit the adjustment steps.

4.2. PRELIMINARY SETTINGS OF THE CONTROLS

- Start this check procedure with NO input signals connected, ALL pushbuttons released and ALL switches in the CAL position.
- Depress the pushbuttons as indicated in the figure below.

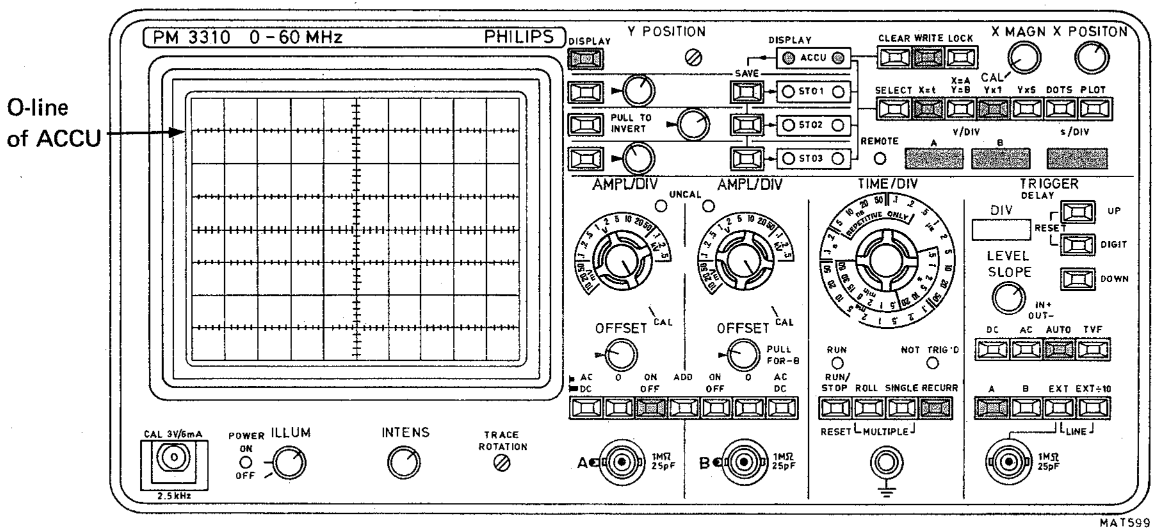


Fig. 3.27.

Unless otherwise stated the controls always occupy the same position as in the previous check.

4.3. CHECKING PROCEDURE

CRT section

- Set POWER switch to ON. Check that the pilot lamp lights and that the power-up test starts according to Section 3.3.2.
- After warm-up the CRT display will show the base-line of the ACCU memory contents.
- Check the screen illumination by turning the ILLUM control.
- Set the INTENS control for a suitable intensity of the display.
- A horizontal line should appear in the centre of the upper two divisions of the CRT display as long as the CLEAR button is depressed.

Vertical section

- Set the AMPL/DIV switch to position 5 V/div.
- Set the TIME/DIV switch to position 0.2 ms/div.
- Check that the displayed line runs exactly in parallel with the horizontal graticule lines.
  (Correction is possible by adjusting screw-driver control TRACE ROTATION at the front panel).
- Turn the OFFSET control clockwise and check that the trace is flashing at the top end of the screen.
  The trace will blink at the bottom line of the ACCU display part by turning OFFSET anti-clockwise.
- Adjust the OFFSET control so that the base-line is shifted to the centre of the upper two divisions.
- Connect the output signal of the CAL terminal to the A or B input socket. Check that horizontally each period covers two divisions and vertically the amplitude is 0.6 divisions.
- Depress the AC/DC input coupling switch to AC and check that the signal is symmetrical around the centre-line of the upper two divisions.
- Release the switch to DC.
- Depress the O switch. A base-line should appear on the centre line of the upper two divisions.
- Release the O switch.
- Check that the range of the continuous AMPL/DIV control is 2.5 times attenuation or more.
- If the continuous AMPL/DIV control is out of its CAL position the UNCAL pilot lamp should light and an asterisk * should appear in the V/DIV display.
  Set the continuous control in its CAL position.
- Check that the range of the continious AMPL/DIV control is 2.5 times attenuation or more (≈ 2 divisions).
  5 V/div.
- The previous check can now be made for the other channel.
- Push the channel B ON-OFF switch to ON.
- Set both channel A and B input coupling switches to AC.
- Connect the CAL signal to both channel A and B inputs.
  Adjust the OFFSET controls to overlap the traces.
- Push ADD and check that the displayed signal is doubled with respect to the amplitude.
- Operate the PULL FOR –B switch and check that a minimum signal amplitude is displayed.
- Set both input coupling switches to DC. Release ADD.
- Release the channel B ON OFF switch to OFF.
- Push the channel B OFFSET control for normal operation.
- Disconnect the B input signal.

Display section

- Depress all four DISPLAY pushbuttons and check that the DISPLAY lamps will light.
- Depress pushbutton CLEAR and check that the ACCU display part (i.e. the ACCU memory contents) is cleared.
- Check that the memories STO 1, STO 2 and STO 3 can also be cleared by simultaneously depressing the CLEAR and relevant SAVE pushbutton.
- Check that there are four traces on the screen e.g. the input signal and the three base-lines of STO 1, STO 2 and STO 3 and check that the three base-lines can be shifted in the vertical direction by turning the Y-POSITION controls.
  Adjust the Y-POSITION controls so that the traces are located on their base-lines.
- Check that the ACCU memory contents can be stored in the memories STO 1, STO 2 or STO 3 by depressing the relevant SAVE pushbuttons.
- Check that the STO 1, STO 2 and STO 3 traces can be inverted by pulling the Y-POSITION controls.
- Push the Y-POSITIONS controls.
- Depress LOCK and check that the memory contents are not influenced until WRITE is depressed.

Display modes

- Turn the X MAGN control fully clockwise.
- Check that by operating the X-POSITION control the magnified display can be completely shifted.
- Depress DOTS and check that separate dots are displayed on the screen.
- Switch X MAGN to CAL; release DOTS and set X-POSITION for correct display.

Set TIME/DIV to	Push SAVE for	ACCU	Push SELECT for	Read s/DIV
1 ms/div	STO 1		STO 1	1 - 3
. 5 ms/div	STO 2		STO 2	. 5 - 3
. 2 ms/div	STO 3		STO 3	. 2 - 3
. 1 ms/div		ACCU	ACCU	. 1 - 3

- Release the STO 1, STO 2 and STO 3 DISPLAY buttons.
- Depress the input coupling switch to AC.
- Check that by pushing Y x 5 full screen display can be obtained and that the zero line is located at the centre of the screen.
- Push Y x 1.
- Depress PLOT and check that an intensified dot appears at the left-hand side of the screen. This dot will follow the trace after a few seconds. Eventually check the recorder outputs at the rear (1 V full-scale).
- Wait until the PLOT action is finished.

Horizontal section

- Depress SINGLE.
  Each time the RESET button is depressed the ACCU memory contents are refreshed and so the display.
- Check that during the SINGLE action the NOT TRIG'D pilot lamp is on.
- Depress the STO 1, STO 2 and STO 3 DISPLAY buttons.
- Depress MULTIPLE (both ROLL and SINGLE) and check that the SINGLE action is repeated four times (in the four memories ACCU, STO 1, STO 2 and STO 3).
- Depress ROLL and apply a 1 Hz signal to the input socket and set AMPL/DIV to an appropriate position.
- Set TIME/DIV to . 5 s/DIV.
- Depress RUN and check that the signal is stored as described in Section 3.4.7.
- Check that the RUN lamp lights permanently when rolling and blinks if the RUN action is finished.
- Disconnect the input signal and depress RECURR.
- Check if all positions of the TIME/DIV switch are displayed correctly in the s/DIV display and set the TIME/DIV switch in . 2 ms/div.
- Connect the CAL output to the input socket.

Trigger delay

- Check that by pressing UP once the trace shifts one division to the left.
  Check that by pressing DOWN once the trace is shifted to its original position.
- Press DIGIT. Check that the next digit in the DIV display blinks and can be changed by pressing UP or DOWN.
  Pressing DOWN will never result in a reading less than –9.
- Check that the DIV display indicates O by pressing RESET (UP and DIV together).

5. PREVENTIVE MAINTENANCE

5.1. GENERAL INFORMATION

This instrument generally requires no maintenance, as the instrument contains no components that are subject to wear.
However, to ensure reliable and troublefree operation, the instrument should not be exposed to moisture, heat, corrosive elements or excessive dust.

5.2. CLEANING THE NEXTEL SUEDE COATING

WARNING: The Nextel suède coating is ethanol-resistant, but is susceptible to methylated spirit, which will attack the surface (due to one of the de-naturing substances).

The bright appearance of the cabinet, lacquered with Nextel suède coating will deteriorate after some time as the surface becomes soiled. Cleaning with a cloth soaked in water, ethanol or a common household cleansing agent does not always restore this lustre and leaves dirt in the holes and the pores.

The 3M Company have developed a new cleansing pad (White Cleansing Pad, Catalogue No. 8440) which when soaked in water, ethanol or a common household cleansing agent will also penetrate holes and pores.

This method is similar to that of abrasive cleaning pads but lacks their abrasive action.
Abrasive cleaning pads should not be used, otherwise surface scratches will result.

5.3. REMOVING THE BEZEL AND THE CONTRAST PLATE TO CLEAN THE CONTRAST FILTER

- Grip the bottom corners of the bezel and gently pull it from the front panel (Fig. 3.28.).
- The contrast filter can now be removed by gently pressing it out of the bezel.
- To prevent scratching the filter when cleaning, ensure that a soft cloth is used, free from dust and abrasive material.

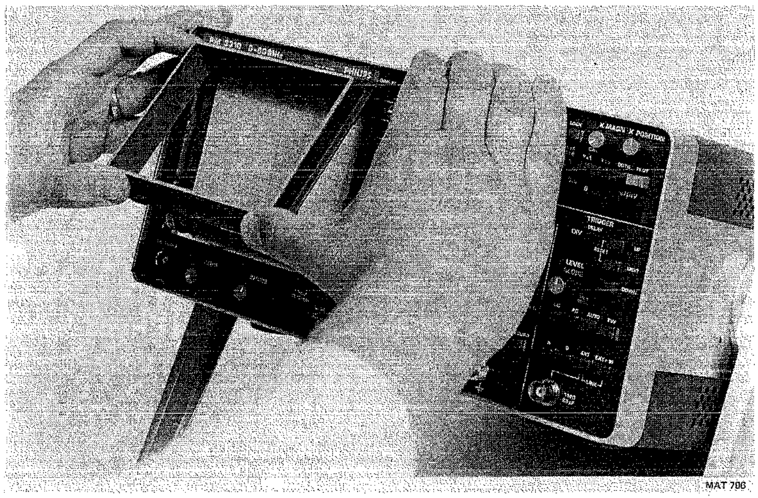


Fig. 3.28. Removing the bezel and the contrast plate.

5.4. RECALIBRATION

From experience it is expected that the oscilloscope operates within its specification for a period of at least 1000 hours or for six months if used infrequently.
In addition, replacement of components may necessitate recalibration of the affected circuits. The checking & adjusting procedure can also be helpful in localising certain troubles in the instrument.
In some cases, minor troubles may be revealed and/or corrected by recalibration. Complete checking & adjusting instructions are given in the Checking & Adjusting Section. (If only a partial calibration is performed, refer to the interaction chart).

SECTION 4 MECHANISM

SECTION 4-1 VHS DECK MECHANISM

SECTION 4-2
8mm DECK MECHANISM

SECTION1 SUMMARY

KEY TO ABBREVIATIONS

A	AC	Alternating Current
	ACC	Automatic Color Control
	ADJ	Adjust
	A/E	Audio Erase
	AFC	Automatic Frequency Control
	AFT	Automatic Fine Tuning
	AGC	Automatic Gain Control
	ALC	Automatic Level Control
	AM	Amplitude Modulation
	AMP	Amplifier
	ANT	Antenna
	APC	Automatic Phase Control
	ASS'Y	Assembly
	AUD	Audio
	AUTO	Automatic
	AUX	Auxiliary
B	B	Base
	BPF	Bandpass Filter
	BW or B/W	Black and White
C	C	Capacitor, Chroma, Collector
	CAN	Cancel
	CAP	Capstan
	CATV	Cable Television
	CBA	Circuit Board Assembly
	CCD	Charge Coupled Device
	CFG	Capstan Frequency Generator
	CH	Channel
	CHROMA	Chrominance
	CLK	Clock
	CNR	Chroma Noise Reduction
	COMB	Combination Comb Filter
	COMP	Comparator Composite Compensation
	CONV	Converter
	CS	Chip Select
	CST	Cassette
	CTL	Control
	CUR	Current
	CYL	Cylinder
D	D	Drum, Digital, Diode, Drain
	dB	Decibel
	DC	Direct Current
	DEMOD	Demodulator
	DET	Detector
	DEV	Deviation
	DHP	Double High Pass
	DIGITRON	Digital Display Tube
	DL	Delay Line
	DOC	Drop Out Compensator
	D/V	Dummy Vertical
E	E	Emitter
	EE	Electric to Electric
	EMP	Emphasis
	EP	Extended Play
	EQ	Equalizer
	ES	Electrostatically Sensitive
F	F	Fuse
	FB	Feed Back
	FBC	Feed Back Clamp
	FE	Full Erase
	FF	Fast Forward
	FG	Frequency Generator
	FL	Filter
	FM	Frequency Modulation
	F/R	Front/Rear
	FS	Frequency Synthesizer
	FSC	Subcarrier Frequency
	F/V	Frequency Voltage
	FWD	Forward
G	GEN	Generator
	GND	Ground
H	H	High, Horizontal
	Hz	Hertz
I	IC	Intergrated Circuit
	IF	Intermediate Frequency
	INS	Insert
	I/O	Input/Output
L	L	Low, Left, Coil
	LD	LED
	LECHA	Letter Character
	LP	Long Play
	LPF	Low Pass Filter
M	MAX	Maximum
	MD	Modulator
	MIC	Microphone
	MIN	Minimum
	MIX	Mixer, Mixing
	M.M.	Mono Multi Vibrator
	MMV	Monostable Multivibrator
	MOD	Modulation, Modulator
	MODEM	Modulator-Demodulator
N	NR	Noise Reduction
O	OSC	Oscillator
	OSD	On Screen Display
P	PB	Playback
	PCB	Printed Circuit Board
	PG	Pulse Generator
	PLL	Phase Locked Loop
	P-P	Peak-to-Peak
	PRE-AMP	Preamplifier
	PS	Phase Shift
	PWM	Pulse Width Modulation
Q	Q	Transistor
	QH	Quasi Horizontal
	QSR	Quick Setting Record
	QTR	Quick Timer Record
	QV	Quasi Vertical
R	R	Resistor, Right
	RE(or RC)	Remocon, Receiver
	REC	Recording
	REF	Reference
	REG	Regulated, Regulator
	REMOCON	Remote Control(unit)
	REV	Reverse
	REW	Rewind
	RF	Radio Frequency
	R/P	Record/Playback
	RTC	Real Time Counter
S	S	Serial
	SH	Shift
	SHARP	Sharpness
	SIF	Sound Intermediate Frequency
	SLD	Side Locking
	S/N	Signal to Noise Ratio
	SP	Standard Play
	SUB	Subtract, Subcarrier
	SW or S/W	Switch
	SYNC	Synchronization
	SYSCON	System Control
T	T	Coil
	TP	Test Point
	TR	Transistor
	TRK	Tracking
	TRANS	Transformer
	TU	Tuner, Take-Up
U	UHF	Ultra High Frequency
	UNREG	Unregulated
V	V	Volt, Vertical
	VA	Always Voltage
	VCO	Voltage Controlled Oscillator
	VGC	Voltage Gain Control
	VHF	Very High Frequency
	VISS	VHS Index Search
	VR	Variable Resistor or Volume
	V-Sync	Vertical Synchronization
	VTG	Voltage
	VV	Voltage to Voltage
	VXO	Voltage X-tal Oscillator
W	W	Watt
	WHT	White
	W/O	With Out
X	X-TAL	Crystal
Y	Y/C	Luminance/Chrominance
	YNR	Luminance Noise Reduction
Z	ZD	Zener Diode

IMPORTANT SAFETY PRECAUTIONS

Prior to shipment from the factory, the products are strictly inspected to conform with the recognized product safety and electrical codes of the countries in which they are to be sold. However, in order to maintain such compliance, it is equally important to implement the following precautions when a set is being serviced.

• Precautions during Servicing

1. Locations requiring special caution are denoted by labels and inscriptions on the cabinet, chassis and certain parts of the product. When performing service, be sure to read and comply with these and other cautionary notices appearing in the operation and service manuals.

2. Parts identified by the ⚠ symbol and shaded (▩) parts are critical for safety.
   Replace only with specified part numbers.
   Note: Parts in this category also include those specified to comply with X-ray emission standards for products using cathode ray tubes and those specified for compliance with various regulations regarding spurious radiation emission.

3. Use Specified internal wiring. Note especially:
   1) Wires covered with PVC tubing
   2) Double insulated wires
   3) High voltage leads

4. Use specified insulating materials for hazardous live parts. Note especially:
   1) Insulation Tape
   2) PVC tubing
   3) Spacers
   4) Insulation sheets for transistor

5. When replacing AC primary side components (transformers, power cords, noise blocking capacitors, etc.) wrap ends of wires securely about the terminals before soldering.(Fig. 1)

6. Observe that wires do not contact heat producing parts (heatsinks, oxide metal film resistors, fusible resistors, etc.)

7. Check that replaced wires do not contact sharp edged or pointed parts.

8. When a power cord has been replaced, check that 10-15Kg of force in any direction will not loosen it.(Fig. 2)

9. Also check areas surrounding repaired locations.

10. Products using cathode ray tubes (CRTs)
    In regard to such products, the cathode ray tubes themselves, the high voltage circuits, and related circuits are specified for compliance with recognized codes pertaining to X-ray emission. Consequently, when servicing these products, replace the cathode ray tubes and other parts with only the parts specified. Under no circumstances attempt to modify these circuits. Unauthorized modification can increase the high voltage value and cause X-ray emission from the cathode ray tube.

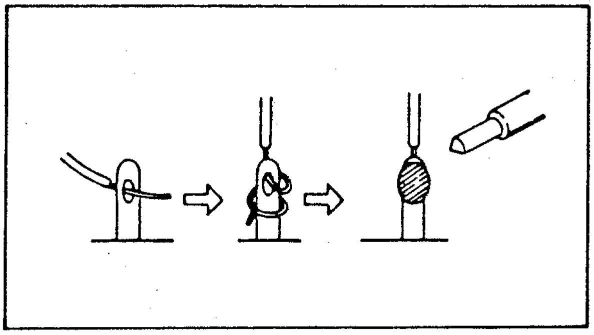


Fig. 1

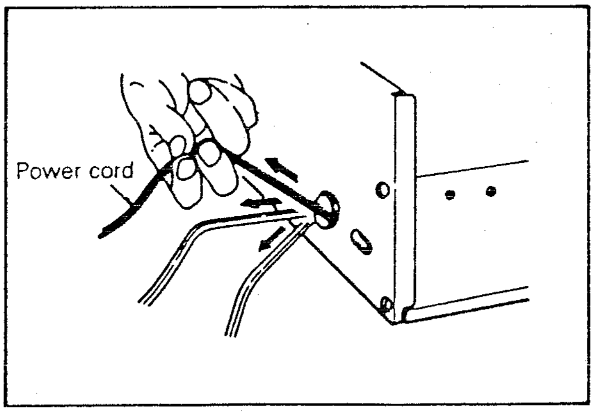


Fig. 2

SAFETY CHECK AFTER SERVICING

Examine the area surrounding the repaired location for damage or deterioration. Observe that screws, parts and wires have been returned to original positions. Afterwards, perform the following tests and confirm the specified values in order to verify compliance with safety standards.

• Insulation resistance test

Confirm the specified insulation resistance or greater between power cord plug prongs and externally exposed parts of the set (RF terminals, antenna terminals, video and audio input and output terminals, microphone jacks, earphone jacks, etc.). See table below.

• Dielectric strength test

Confirm specified dielectric strength or greater between power cord plug prongs and exposed accessible parts of the set(RF terminals, antenna terminals, video and audio input and output terminals, microphone jacks, earphone jacks, etc.). See table below.

• Clearance distance

When replacing primary circuit components, confirm specified clearance distance (d), (d') between soldered terminals, and between terminals and surrounding metallic parts. See table below.

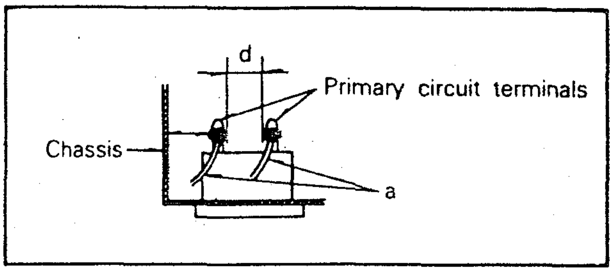


Fig. 3

Table 1:Ratings for selected areas

AC Line Voltage	Region	Insulation Resistance	Dielectric Strength	Clearance Distance(d),(d)
*110 to 130 V 200 to 240 V	Europe Australia	≧10 MΩ/500 V DC	4kV 1 minute	≧6mm(d) ≧8mm(d) (a Power cord)

*Class II model only.

Note. This table is unofficial and for reference only. Be sure to confirm the precise values for your particular country and locality.

• Leakage Current test

Confirm specified or lower leakage current between B(earth ground, power cord plug prongs) and externally exposed accessible parts (RF terminals, antenna terminals, video and audio input and output terminals, microphone jacks, earphone jacks, etc.)

Measuring Method: (Power ON)
Insert load Z between B(earth ground, power cord plug prongs) and exposed accessible parts. Use an AC voltmeter to measure across both terminals of load Z. See figure and following table.

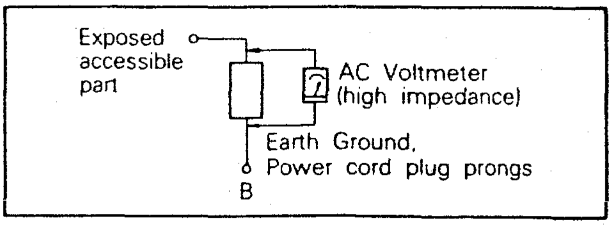


Fig. 4

Table 2:Leakage current ratings for selected areas

AC Line Voltage	Region	Load Z	Leakage Current(i)	Earth Ground (B) to:
100 to 130 V	Europe	2kΩ	i≦0.7m A peak i≦2m A dc	Antenna earth terminals
200 to 240 V	Australia	50kΩ	i≦0.7m A peak i≦2m A dc	Other terminals

Note. This table is unofficial and for reference only. Be sure to confirm the precise values for your particular country and locality.

INTRODUCTION

This service manual provides a variety of service information. It contains the mechanical structure of the Double Deck Video Cassette Recorder together with mechanical adjustments and the electronic circuits in schematic form. This Double Deck VCR was manufactured and assembled under our strict quality control standards and meets or exceeds industry specifications and standards.

FEATURES

- the VHS and 8 mm system with HQ-picture technology for extraordinary picture-sharpness and high resolution.
- the digital tracking automatic which makes the enjoying manual control obsolete.
- automatic power and playback.
- four VHS video heads for a clear still image and a variable slow motion.
- three 8 mm video heads for 8 mm playback only.
- assemble editing from 8 mm tape to VHS tape.
- the easy searching of your recordings by automatic and manual index marking, that can also be erased.
- the quick mechanism for fast tape function transitions.
- the long play VHS recording and playback facility.
- the real time tape counter and the VHS remaining tape time display.
- 8 timer programme memories, also for daily or weekly recurring recordings, within one year can be programmed at the same time.
- the on-screen display of many functions e.g. the stored timer programmes.
- and many more, like additional audio and video input at the front, Euro-AV sockets, audio dubbing, child lock, immediate recording timer, and title generator.
- TV Programmer, Digital Link.
- SHOWVIEW
  ShowView is a trademark applied for by Gemstar Development Corp.
  ShowView system is manufactured under license from Gemstar Development Corporation.

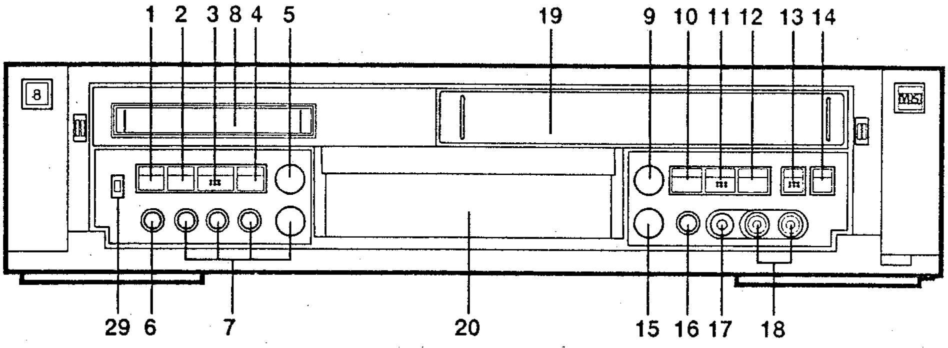
SPECIFICATIONS

General		
Power supply :		AC 230V(± 10%), 50Hz
Power consumption :		Approx. 45W
Cabinet size(W × H × D) :		430 × 99 × 390mm
Weight :		Approx. 8Kg
Operating temperature :		5° C to 35° C surrounding temperature
Operating humidity :		35-80%
8 mm Player section		
Format :		8 mm PAL Standard
Heads :		3 video heads
Tape speed :	(SP)	20.05 mm/sec.
	(LP)	10.025 mm/sec.
Tape width :		8 mm
Video output :		1 Vpp 75 ohm unbalanced
Audio output :		500 mV, <1 kohm
VHS Recorder section		
Format :		VHS PAL Standard
Heads :		4 video heads
Tape speed :	(SP)	23.39 mm/sec.
	(LP)	11.635 mm/sec.
Tape width :		12.7 mm
Video :		PAL B/G, SECAM-L
Recording/playback time :		300 min. (LP : 600 min.) with E-300
Aerial input :		PAL : VHF 2-12 (SECAM) UHF 21-69 CATV S1-S40
RF output :		UHF channels 32~40 (Variable)
Video input :		1 Vpp 75 ohm unbalanced
Video output :		1 Vpp 75 ohm unbalanced
S/N ratio (video) :		45dB nominal
Audio input :		500 mV, >50 kohm
Audio output :		500 mV, <1 kohm
S/N ratio (audio) :		45 dB nominal
Audio frequency range :		63-12,500 Hz nominal

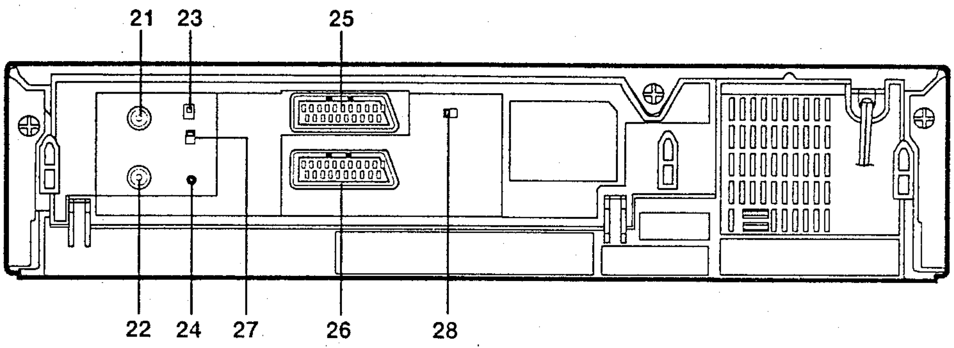
* Designs and specifications are subject to change without notice.

LOCATION OF CUSTOMER CONTROLS

FRONT



REAR



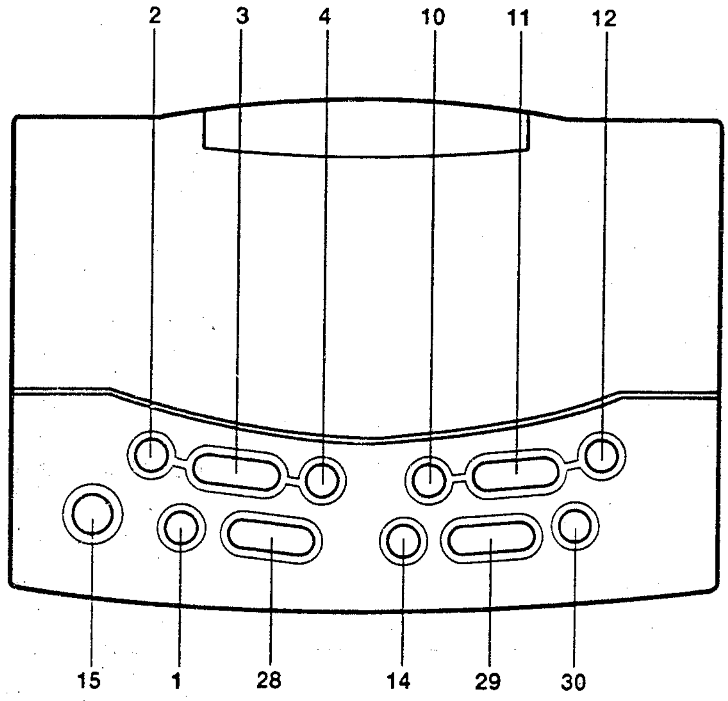
8 mm Player section

1. STILL BUTTON
2. REWIND/REVIEW BUTTON
3. PLAY BUTTON
4. FAST FORWARD/CUE BUTTON
5. STOP/EJECT BUTTON
6. V.INSERT BUTTON
7. ASSEMBLE EDITING BUTTONS
8. CASSETTE COMPARTMENT

VHS Recorder section

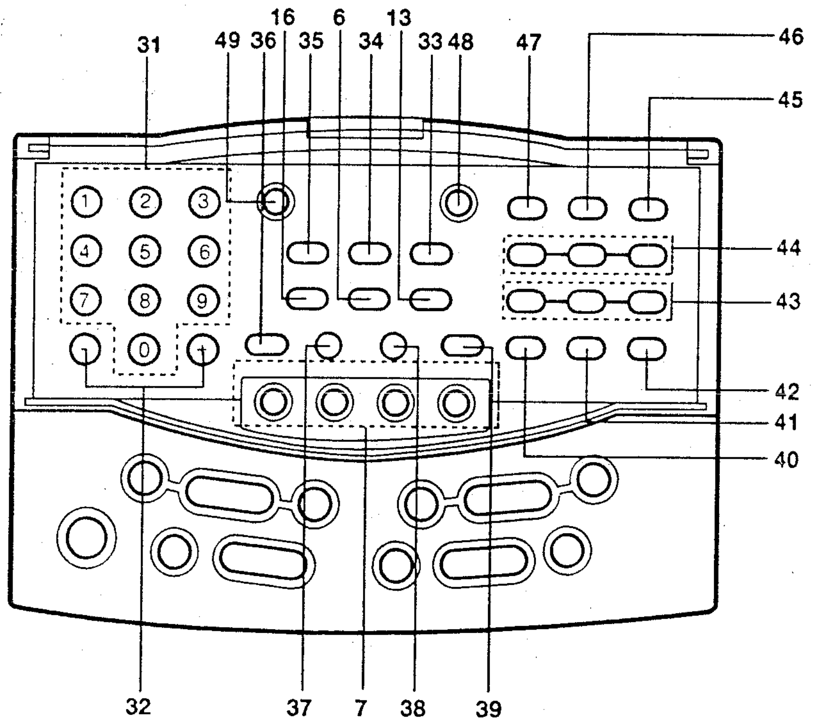
9. STOP/EJECT BUTTON
10. REWIND/REVIEW BUTTON
11. PLAY BUTTON
12. FAST FORWARD/CUE BUTTON
13. REC/QSR BUTTON
14. P/STILL BUTTON
15. OPERATE ON/OFF BUTTON
16. AUDIO DUBBING BUTTON
17. MIC IN JACK
18. AUDIO/VIDEO IN JACKS
19. CASSETTE COMPARTMENT
20. VCR DISPLAY
21. AERIAL INPUT SOCKET
22. RF OUT SOCKET
23. TPSG ON/OFF SWITCH
24. RF CHANNEL CONTROL
25. EURO-AV 1 SOCKET
26. EURO-AV 2 SOCKET
27. SYSTEM SELECT SWITCH
28. COLOR ON/OFF SWITCH
29. TV/VTR BUTTON

REMOTE CONTROL



1. STILL BUTTON
2. REWIND/REVIEW BUTTON
3. PLAY BUTTON
4. FAST FORWARD/CUE BUTTON
6. V. INSERT BUTTON
7. ASSEMBLE EDITING BUTTONS
10. REWIND/REVIEW BUTTON
11. PLAY BUTTON
12. FAST FORWARD/CUE BUTTON
13. REC/QSR BUTTON
14. P/STILL BUTTON
15. OPERATE ON/OFF BUTTON
16. AUDIO DUBBING BUTTON

28. STOP BUTTON
29. STOP BUTTON
30. FRAME ADVANCE BUTTON
31. NUMBER BUTTONS
32. PROG/TRK BUTTONS (+/−)
33. TAPE SPEED BUTTON
34. TU/AV BUTTON
35. MIC MIX BUTTON
36. AUTO TRACKING BUTTON
37. 8 mm RESET BUTTON
38. VHS RESET BUTTON



39. REST BUTTON
40. MENU BUTTON
41. DISPLAY/PG. OUT BUTTON
42. CLEAR/PG. CLR BUTTON
43. SLOW/MFT BUTTONS
44. VISS BUTTONS
45. CHILD LOCK BUTTON
46. TV/VTR BUTTON
47. VPS BUTTON : *
48. SHOWVIEW BUTTON
49. MONITOR BUTTON

※ * : Optional Function

SECTION 2 CABINET & MAIN FRAME
SERVICE FIXTURE CONNECTING METHOD

1. SVC FIXTURE Connecting Method

A. FIXTURE Cable ① Connecting Method.

a) Connect the FIXTURE Cable ① between Main C.B.A and Junction C.B.A. (P2J01, P2J02, P2J03)

b) At this time, should be in the left side " ← LEFT" mark on the P.C.B of the FIXTURE Cable ①. (See Fig. 2-a, 2-c)

c) Connect the connector of "MAIN" mark of FIXTURE Cable ① with the Main C.B.A and the connector of "JUNCTION" mark with the Junction C.B.A. (See Fig. 2-a, 2-c)

B. FIXTURE Cable ② Connecting Method.

a) Connect the FIXTURE Cable ② between Main C.B.A and Pre-Amp Ass'y. (P3P01=P9301, P3P02=P9302)

b) At this time, should be in the left side " ← LEFT" mark on the P.C.B of the FIXTURE Cable ②. (See Fig 2-a, 2-b)

c) Connect the connector of "MAIN" mark of FIXTURE Cable ② with the Main C.B.A and the connector of "JUNCTION" mark with the Pre-Amp Ass'y. (See Fig. 2-a, 2-b)

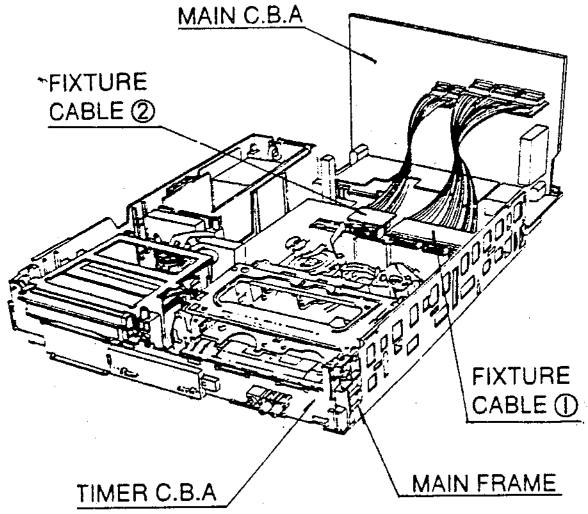


Fig. 2-a

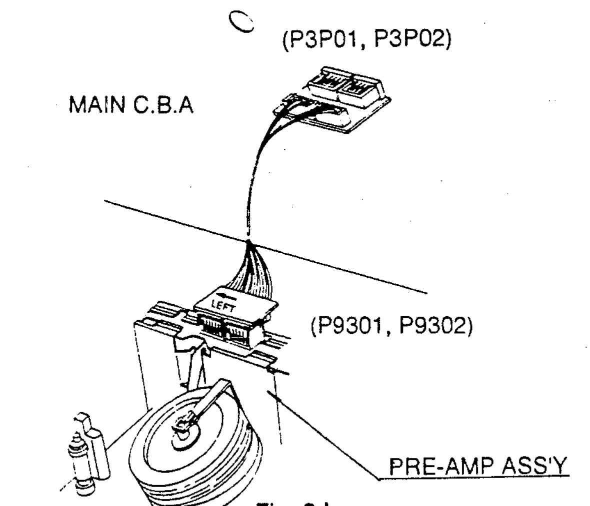


Fig. 2-b

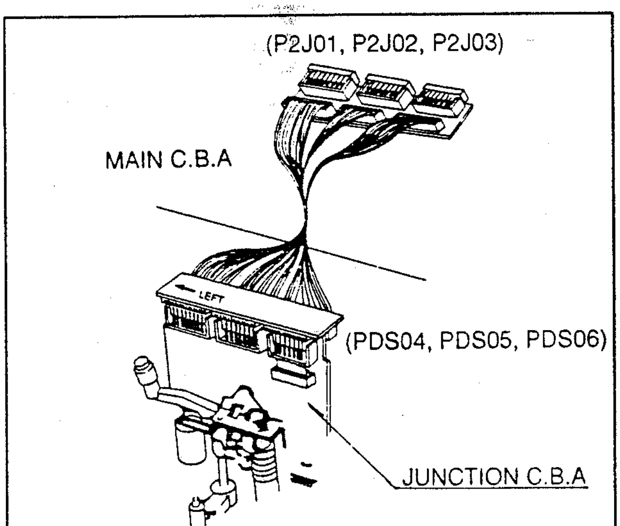
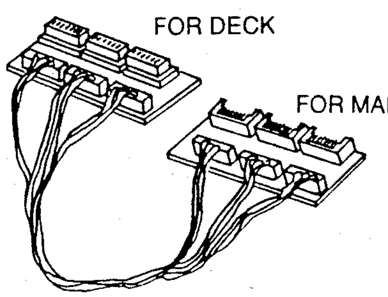


Fig. 2-c

2. Electrical Service Fixture List

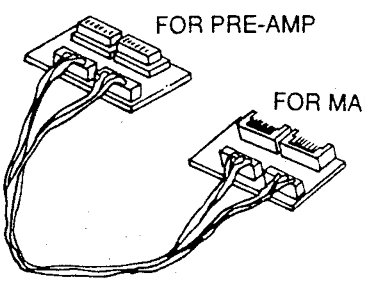
A. Fixture Cable ①.

Parts No.: 232-972A (Optional Parts)



B. Fixture Cable ②.

Parts No.: 515-789A (Optional Parts)



CABINET DISASSEMBLY

1. Top Case

A. Release 7 screws (1).
B. Hold the back of Top Case and lift it up slightly backward to remove it.

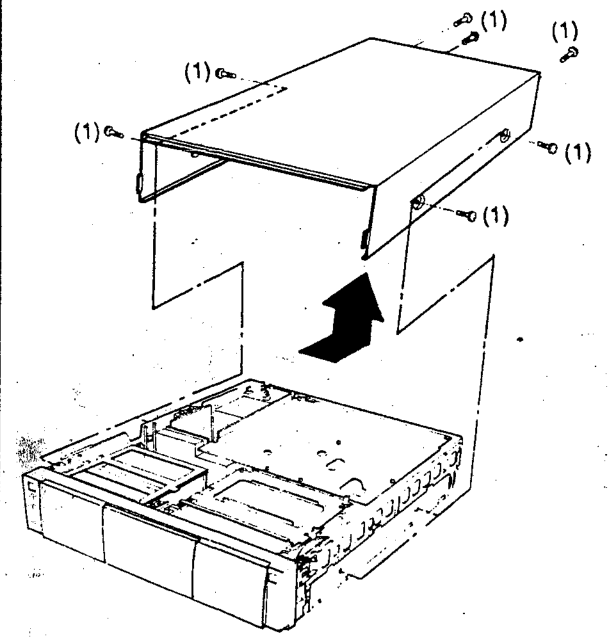


Fig. 2-1

2. Bottom Cover

A. Release 9 screws (2) to remove the Bottom Cover.

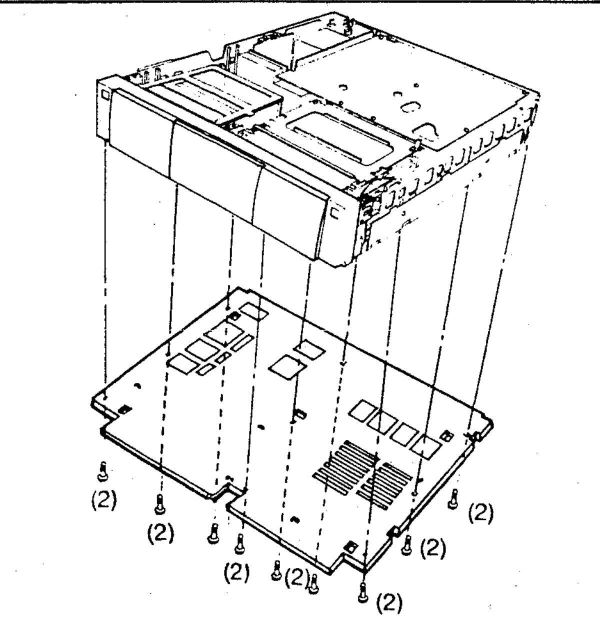


Fig. 2-2

3. Front Panel

A. Release 2 screws (3).
B. Remove the stoppers on the top of Front Panel.
C. Remove the stoppers on the bottom side Front Panel.

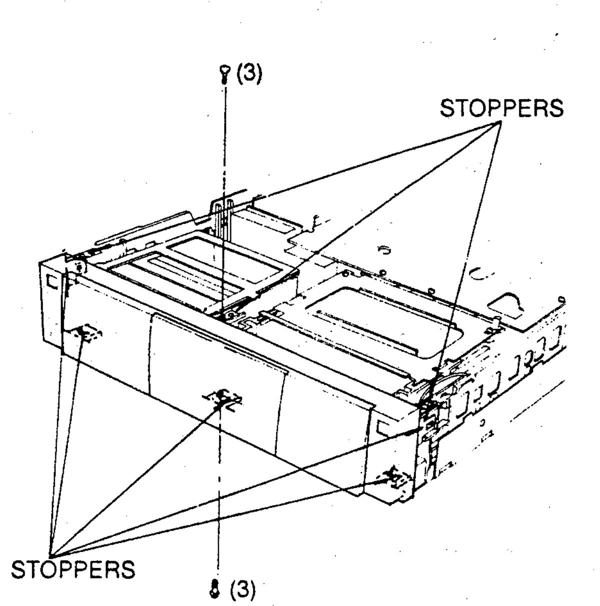


Fig. 2-3

* Caution

When reassemble the Front panel, assemble it in condition of inserting the Door Cassette inside, as shown in Fig.2-4

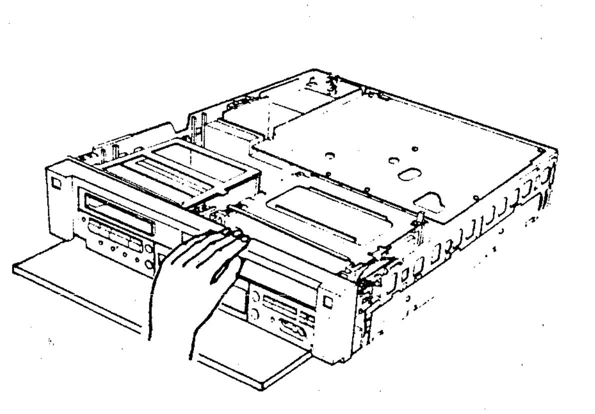


Fig. 2-4

CIRCUIT BOARD DISASSEMBLY

1.Circuit Board Arrangement

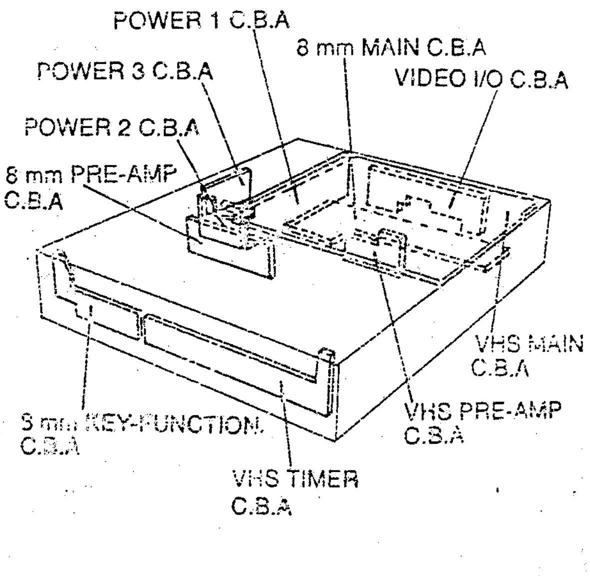


Fig. 2-5

2. VHS Main Circuit Board

A. Release 4 screws (4).
B. Remove the Main C.B.A in the direction of arrow (A).

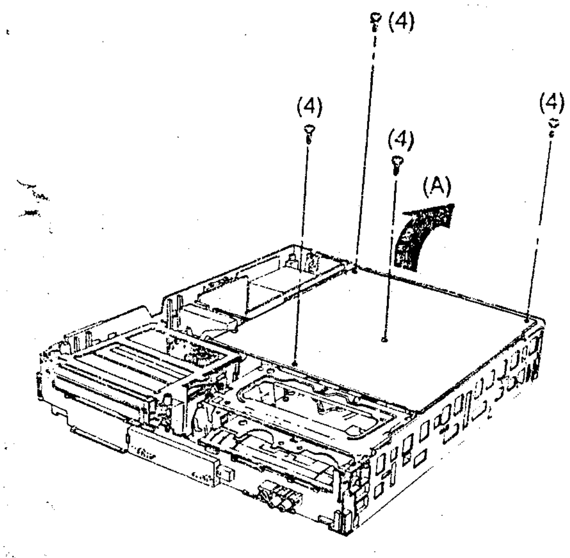


Fig. 2-6

3. Power 1, 2, 3 Circuit Board

A. Remove the Bottom Cover. (Fig. 2-2)
B. Release 4 screws (5).
C. Remove the Power C.B.A in the direction of arrow (B).

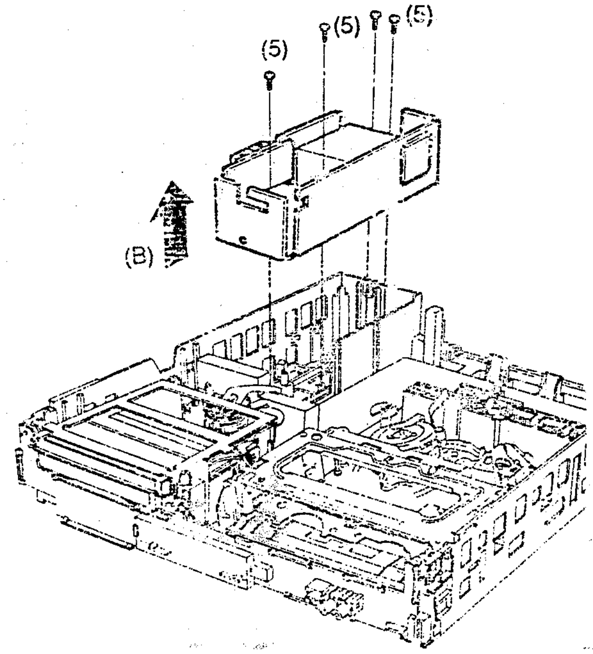


Fig. 2-7

4. 8mm Main Circuit Board

A. Release 2 screws (6).
B. Remove the 8mm Main C.B.A in the direction arrow (C).

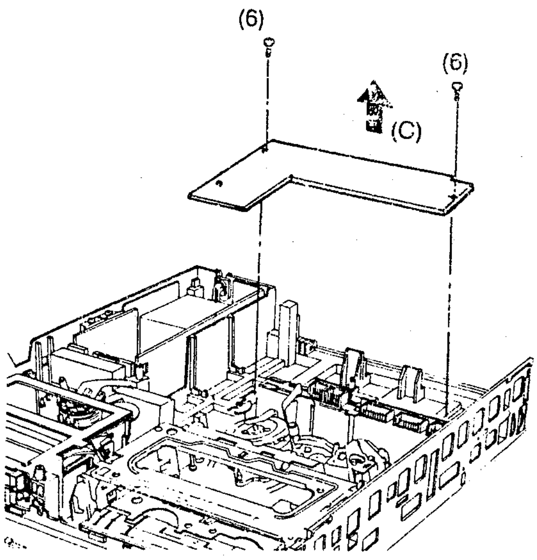


Fig. 2-8

5. 8mm/VHS Pre-Amp Circuit Board

A. Release 2 screws (7).
B. Remove the 8mm Pre-Amp C.B.A.
C. Release 3 screws (8).
D. Remove the VHS Pre-Amp C.B.A.

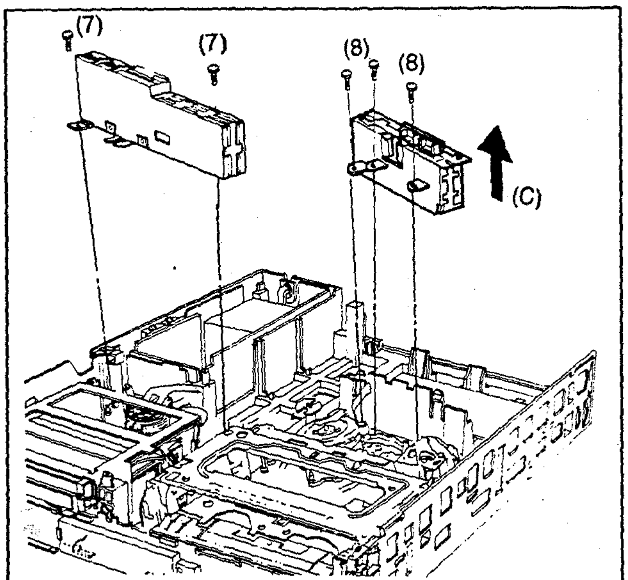


Fig. 2-9

6. 8 mm/VHS Key Function Circuit Board

A. Release screw (9).
B. Release 5 stoppers in the direction arrow (D).
C. Remove the 8mm/VHS Key Function C.B.A in the direction arrow (E).

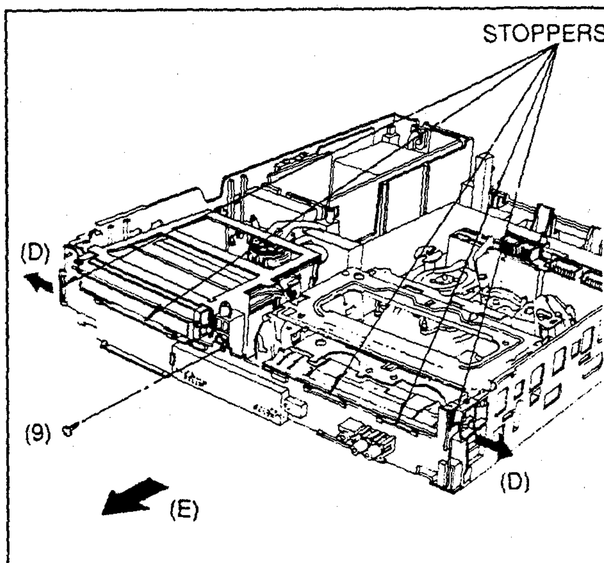


Fig. 2-10

SECTION 3 ELECTRICAL

ELECTRICAL ADJUSTMENT PROCEDURES

• Electronic Test Equipment Requirement

• Oscilloscope	• Monitor Scope
• Video signal Generator	• + Driver
• Modem Tester	• Test Tape (SP)-PAL, SECAM (VHS, 8mm)
• Level Meter	• Recording Tape (VHS)
• Frequency Counter	• Digital Multimeter
• Power Supply	

1. VHS Circuit Adjustment

1-1. Servo Circuit

1-1-1. PG Adjustment

MODE	SPECIFICATION	MEASUREMENT POINT	ADJUSTMENT POINT
PLAYBACK	6.5H±0.5H (1H=64.0μsec)	TP201 (H.SW) TP202 (V.Out terminal)	VR201

Procedure :

a. Playback a VHS PAL SP test tape.
b. Connect CH-1 of oscilloscope to TP201 (H.SW) and CH-2 to TP202 (Video Out terminal).
c. Trigger the complex Video signal to CH-1 H.SW, and adjust VR201 so that the distance from switching point of H.SW signal to the starting point of horizontal synchronized signal is 6.5H± 0.5H (416±32μsec)

Waveform

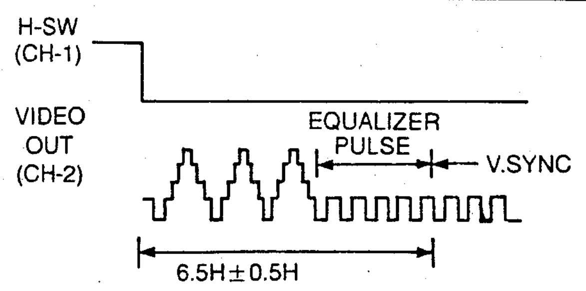


Fig. 3-1-1

1-2. Y/C Circuit

1-2-1. EE Level Adjustment

MODE	SPECIFICATION	MEASUREMENT POINT	ADJUSTMENT POINT
STOP	2.0±0.1Vp-p	TP202	VR304

Procedure :

a. Connect the Video signal Generator to Video in terminal.
b. Input Color Bar signal to Video in terminal.
c. Connect CH-1 of oscilloscope to TP202.
d. Adjust VR304 so that the value from the lower part of synchronism to 100% white signal is 2.0 ±0.1Vp-p.

Waveform

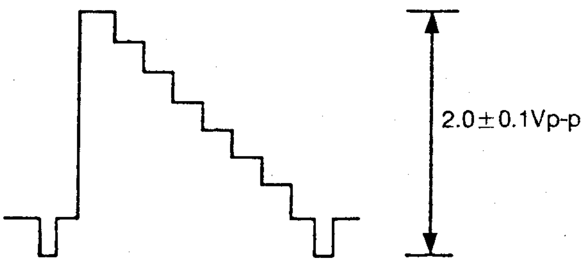


Fig. 3-1-2

1-2-2. Playback Luminance Level Adjustment

MODE	SPECIFICATION	MEASUREMENT POINT	ADJUSTMENT POINT
PLAYBACK (SP)	2.0±0.1Vp-p	TP202	VR305

Procedure :

a. Connect CH-1 of oscilloscope to TP202.
b. Playback a VHS PAL SP test tape (with 100% white signal).
c. Adjust VR305 so that the value from the lower part of synchronism to 100% white signal is 2.0 ±0.1Vp-p.

Waveform

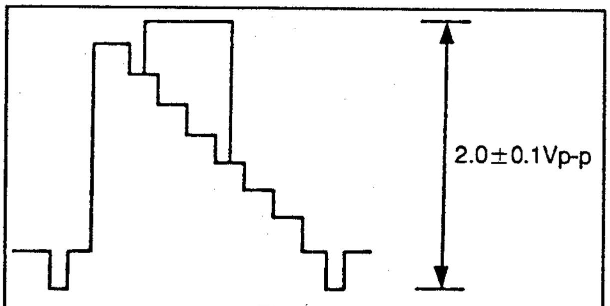


Fig. 3-1-3

1-2-3. FM Carrier Frequency Adjustment

MODE	SPECIFICATION	MEASUREMENT POINT	ADJUSTMENT POINT
RECORD LINE mode	3.8MHz±0.05MHz at SYNC Tip	TP301 (CAR/DEV TP)	VR303

Procedure :

a. Input Color Bar signal (with 100% white signal) to Video in terminal (Scart Jack).
b. Connect In terminal of Modem Tester to TP301.
c. Connect Out terminal of Modem Tester to CH-1 of oscilloscope (But the set and the Modem Tester should be connected with 10:1 probe).
d. The terminal position of Modem Tester is operated to be ATT.0dB, PAL/SECAM mode, Demod, Marker on.
e. Adjust VR303 so that SYNC Tip of video signal is agreed with 3.8MHz Marker on scope.

Waveform

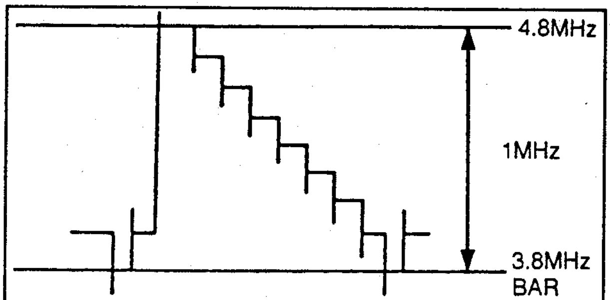


Fig. 3-1-4

1-2-4. FM Deviation Frequency Adjustment

MODE	SPECIFICATION	MEASUREMENT POINT	ADJUSTMENT POINT
RECORD LINE mode	4.8MHz±0.05MHz at White Peak	TP301 (CAR/DEV TP)	VR301

Procedure :

a. Input Color Bar signal (with 100% white signal) to Video in terminal (Scart Jack).
b. Connect In terminal of Modem Tester to TP301.
c. Connect Out terminal of Modem Tester to CH-1 of oscilloscope (But the set and the Modem Tester should be connected with 10:1 probe).
d. The terminal position of Modem Tester is operated to be ATT.0dB, PAL/SECAM mode, Demod, Marker on.
e. Adjust VR301 so that 100% white peak of Video signal is agreed with 4.8MHz Marker on scope.

Waveform

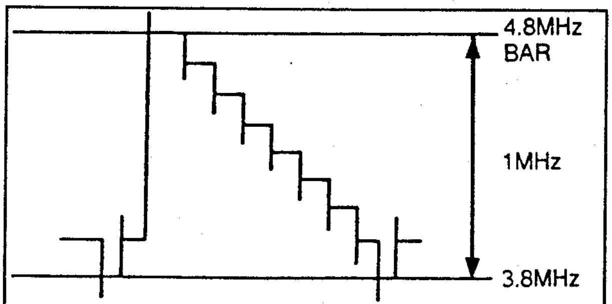


Fig. 3-1-5

1-2-5. Recording Luminance Level Adjustment

MODE	SPECIFICATION	MEASUREMENT POINT	ADJUSTMENT POINT
RECORD LINE mode	350mVp-p	TP302 (REC-Y)	VR302

Procedure :

a. Input Color Bar signal (with 100% white signal) to Video in terminal (Scart Jack).
b. Connect CH-1 of oscilloscope to TP202.
c. Connect CH-2 of oscilloscope to TP302.
d. Record the SP mode.
e. Adjust VR302 so that the waveform is 350mVp-p.

Waveform

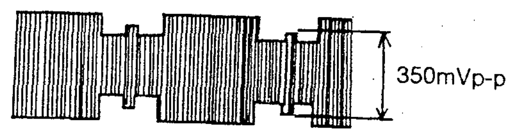


Fig. 3-1-6

1-2-6. SECAM Playback Gate Timing Adjustment

MODE	SPECIFICATION	MEASUREMENT POINT	ADJUSTMENT POINT
PLAYBACK	CH-1 & CH-2 Refer to waveform	TP202 TP303	VR306

Procedure :

a. Connect CH-1 of oscilloscope to TP202.
b. Connect CH-2 of oscilloscope to TP303.
c. Playback a VHS SECAM test tape (with 100% white color bar signal).
d. Adjust VR306 so that SYNC Gate signal of CH-2 is agreed with starting point of video signal sync period on scope CH-1.

Waveform

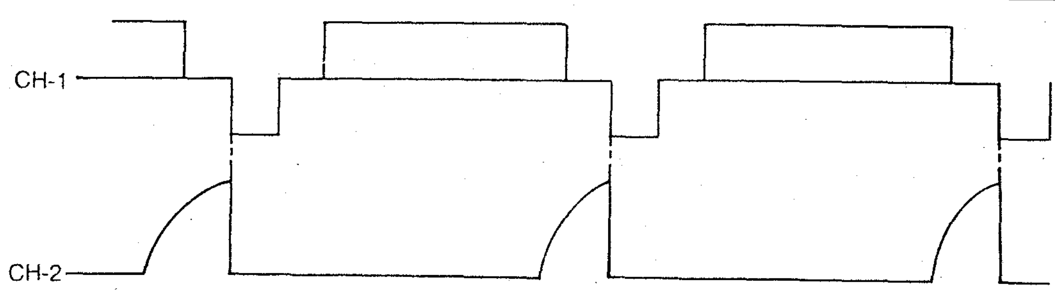


Fig. 3-1-7

1-2-7. SECAM Playback Input Bell Adjustment

MODE	SPECIFICATION	MEASUREMENT POINT	ADJUSTMENT POINT
PLAYBACK	Refer to waveform	TP202 TP304	FL306

Procedure :

a. Connect CH-1 of oscilloscope to TP202.
b. Connect CH-2 of oscilloscope to TP302.
c. Playback a VHS SECAM test tape (with 100% white color bar signal).
d. Adjust FL306 so that the envelope waveform of color signal become a flat level it not flat.

Waveform

Before Adjustment

After Adjustment

Fig. 3-1-8

1-2-8. SECAM Playback Output Bell Adjustment

MODE	SPECIFICATION	MEASUREMENT POINT	ADJUSTMENT POINT
PLAYBACK	Refer to waveform	TP202 TP305	FL308

Procedure :

a. Connect CH-1 of oscilloscope to TP202.
b. Connect CH-2 of oscilloscope to TP305.
c. Playback a VHS SECAM test tape (with 100% white color bar signal).
d. Adjust FL308 so that the Magenta part of color signal become a flat level if not flat.

Waveform

Before Adjustment

After Adjustment

Fig. 3-1-9

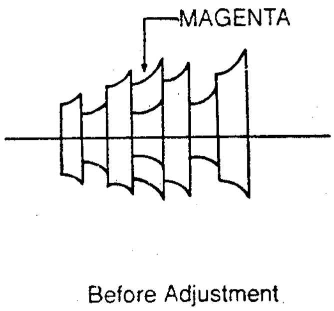
1-2-9. SECAM Recording Bell Adjustment

MODE	SPECIFICATION	MEASUREMENT POINT	ADJUSTMENT POINT
RECORD	Refer to waveform	TP202 TP304	FL305

Procedure :

a. Connect CH-1 of oscilloscope to TP202.
b. Connect CH-2 of oscilloscope to TP304.
c. Input SECAM Color bar signal (with 100% white signal) to Video in terminal (Scart Jack).
d. Record the SP mode.
e. Adjust FL305 so that the Magenta part of color signal become a flat level if not flat.

Waveform



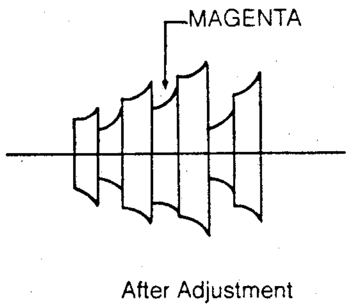


Fig. 3-1-10

1-3. Audio Circuit

1-3-1. Record Bias Adjustment

MODE	SPECIFICATION	MEASUREMENT POINT	ADJUSTMENT POINT
RECORD (SP)	2.6±0.05mVrms	R436 Both Terminal	VR401

Procedure :

a. Loading the recording tape and record.
b. Connect (+), (−) terminal of Level Meter to both terminals R436.
c. Adjust VR401 so that the oscillation voltage fit to specification.

1-4. Tuner/IF Circuit

1-4-1. VIF Adjustment

MODE	SPECIFICATION	MEASUREMENT POINT	ADJUSTMENT POINT
EE	2.5V±0.1V	TP702	T701

Procedure :

a. Connect as shown in Fig. 3-1-11.
b. Receive the CH-11 (217.25MHz).
c. Adjust T701 so that the Digital voltmeter 1 is 2.5 ±0.1V.

CONNECTION DIAGRAM

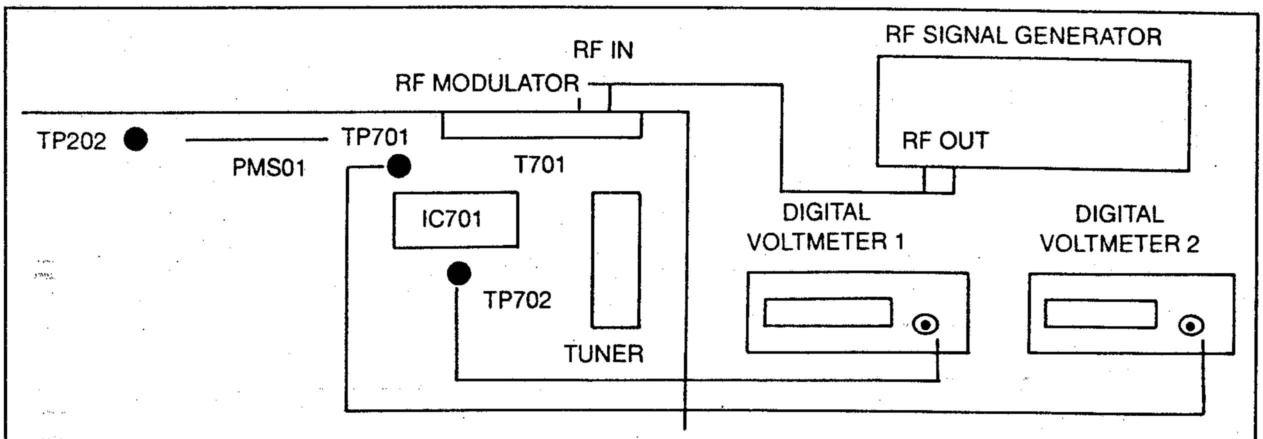


Fig. 3-1-11

***Caution in testing**

1. When practing this adjustment, adjust after more than 10minutes with TV set turning on.
2. Adjust after completing itself test of measuring apparatus.
3. Sweep OSC marker frequency is followed by Table 1.

***Abbreviation**

- APC : Adjacent Picture Carrier
- SIF : Sound Intermediate Frequency
- CIF : Color Intermediate Frequency
- CEN : Center Frequency
- PIF : Picture Intermediate Frequency
- ASC : Adjacent Sound Carrier

Table 1 Frequency Table (MHz)

BROADCASTING SYSTEM	ADJUSTMENT MARKER FREQUENCY					
	APC	SIF	CIF	CEN	PIF	ASC
PAL B/G+SECAM L	31.90	33.40	34.47	36.00	38.90	40.40

1-4-2. RF AGC Adjustment

MODE	SPECIFICATION	MEASUREMENT POINT	ADJUSTMENT POINT
EE	$4.7^{+0.1}_{-0}$V	TP701	VR701

Procedure :

a. Connect as shown in Fig. 3-1-11.
b. Receive the CH-11 (217.25MHz, strength of input electric field : 70dBμV).
c. Adjust VR701 so that the Digital voltmeter 2 is $4.7^{+0.1}_{-0}$V.

2. 8mm Circuit Adjustment

2-1. Servo Circuit

2-1-1. PG Adjustment

MODE	SPECIFICATION	MEASUREMENT POINT	ADJUSTMENT POINT
PLAYBACK	7H±1.8H (1H=64.0μ sec)	TP4K1 (H.SW) TP3A1 (V.Out terminal)	VR501

Procedure :

a. Playback a 8mm PAL SP test tape.
b. Connect CH-1 of oscilloscope to TP4K1 (H.SW) and CH-2 to TP3A1 (Video Out terminal)
c. Trigger the complex Video signal to CH-1 H.SW, and adjust VR501 so that the distance from switching point of H.SW signal to the starting point of horizontal synchronized signal is 7H± 1.8H (448±115.2μsec).

Waveform

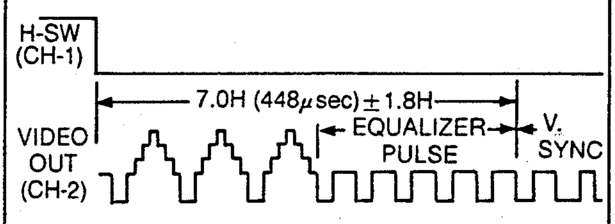


Fig. 3-2-1

2-2. Y/C Circuit

2-2-1. Playback Output Level Adjustment

MODE	SPECIFICATION	MEASUREMENT POINT	ADJUSTMENT POINT
PLAYBACK (SP)	1.0±0.05Vp-p	TP3A1	VR3A1

Procedure :

a. Connect CH-1 of oscilloscope to TP3A1.
b. Playback a 8mm PAL SP test tape (Color bar with 100% white signal).
c. Adjust VR3A1 so that Video out level is 1.0± 0.05Vp-p.

Waveform

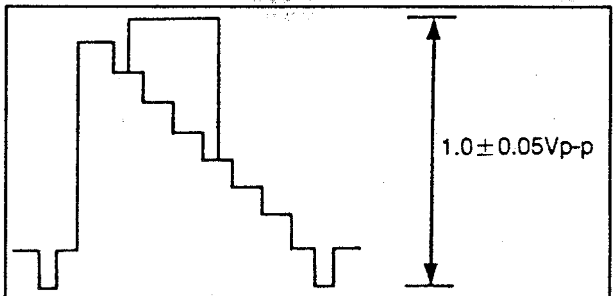


Fig. 3-2-2

2-2-2. Color VCO Adjustment

MODE	SPECIFICATION	MEASUREMENT POINT	ADJUSTMENT POINT
PLAYBACK (SP)	DC2.5±0.1Vp-p	TP3A2	FL3A2

Procedure :

a. Connect CH-1 of oscilloscope to TP3A2.
b. Playback a 8mm PAL SP test tape (Color bar with 100% white signal).
c. Adjust FL3A2 so that DC level is 2.5±0.1Vp-p.

2-3. Audio Circuit

2-3-1. FM VCO Adjustment

MODE	SPECIFICATION	MEASUREMENT POINT	ADJUSTMENT POINT
PLAYBACK (SP)	DC2.1±0.1Vp-p	TP4A2	VR4A2

Procedure :

a. Connect CH-1 of oscilloscope to TP4A2.
b. Playback a 8mm PAL SP test tape (with 400Hz Audio signal).
c. Adjust VR4A2 so that Center Voltage is DC2.1± 0.1Vp-p.

Waveform

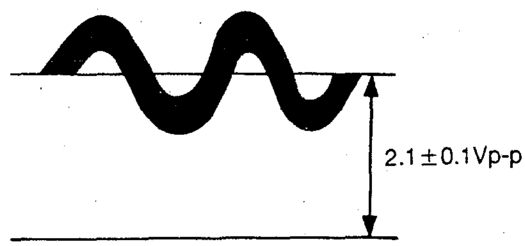


Fig. 3-2-3

2-3-2. FM Deviation Adjustment

MODE	SPECIFICATION	MEASUREMENT POINT	ADJUSTMENT POINT
PLAYBACK (SP)	6±0.5dBm	TP4A1 (Audio Out terminal)	VR4A1

Procedure :

a. Connect (+) terminal of Level Meter to TP4A1 (Audio Out terminal).
b. Playback a 8mm PAL SP test tape (with 1KHz or 400Hz Audio signal).
c. Adjust VR4A1 so that level is 6±0.5dBm.

INHALT

1. ALLGEMEINES

1.1. EINLEITUNG

Das Digitale Speicheroszilloskop PM 3310 ist ein tragbares, Zweikanal 60 MHz Messgerät mit mikroprozessorgesteuerten elektronischen Schaltungen.
Seine kompakte ergonomische Konstruktion erleichert die ausgebreiteten Messmöglichkeiten des Geräts. Die vielseitige Schaltungsanordnung kombiniert mit der Software des Mikroprozessors sind die Grundlage für den bemerkenswerten Umfang an Eigenschaften, wie:

- Helles Bild
- Vor-Trigger Darstellung
- Speicherung von zwei Kanälen mit vier verschiedenen "Ereignis" Signalen pro Kanal.
- IEC-Bus, wahlweise (mit Hilfe des PM 3325)
- Plotterausgang
- Triggerverzögerung
- Speicher Batterienünterschutzung (Batterien nicht einbegriffen).

Ein grosser 8cm x 10cm Bildschirm mit Rasterbeleuchtung vereinfacht die Beobachtung, eine 10kV Beschleunigungsspannung liefert eine Leuchtspur hoher Intensität mit einem eindeutig definiertem Leuchtfleck.

Der Einsatz von zahlreichen integrierten Schaltungen gewährleistet einen stabilen Betrieb und reduziert die Anzahl der Einstellpunkte.
Die Versorgungsspannung ist für zwei Bereiche einstellbar: 100 . . . 120V ± 10% oder 220 . . . 240V ±10%.
Dank der oben erwähnten Merkmale eignet sich das Oszilloskop für einen ausgedehnten Anwendungsbereich, beispielsweise für die Messung und die Beobachtung von:

- Anstiegszeit (liefert sehr helle Bildintensität)
- sehr schnellen Signalen (mit sehr niederiger Wiederholfrequenz)
- Signalen sehr niedriger Frequenz (bis zu 1 Stunde/Teil)

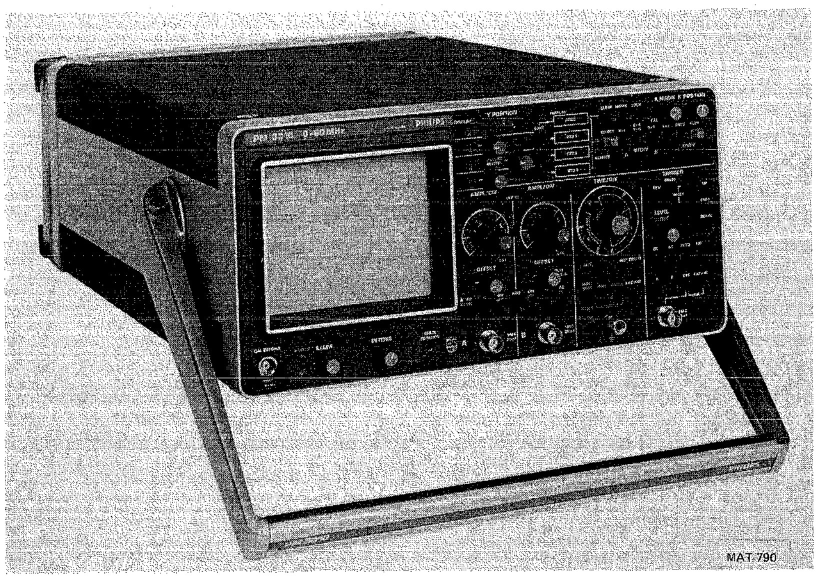


Bild 1.1. 60 Hz Digitales Speicheroszilloskop PM 3310

1.2. TECHNISCHE DATEN

Dieses Gerät ist gemäss IEC 348, Sicherheitsbestimmungen für Mess- und Regeleinrichtungen, gebaut und geprüft und hat das Werk in sicherheitstechnisch einwandfreiem Zustand verlassen. Um diesen Zustand zu erhalten und einen gefahrlosen Betrieb sicherzustellen, muss der Anwender die Hinweise und Warnvermerke beachten, die in vorliegender Anleitung enthalten sind.

- Diese Kenndaten gelten nach einer Anwärmzeit des Geräts von 30 Minuten (Bezugstemperatur 23 °C).
- Zahlenwerte mit Toleranzangaben werden vom Hersteller garantiert.
  Zahlenwerte ohne Toleranzangaben sind Durchschnittswerte und dienen nur zur Information.
- Ungenauigkeiten (absolut oder in %) sind bezogen auf den angegebenen Bezugswert.

1.2.1. Elektronenstrahlröhre

Elektronenstrahlröhre	D14 - 292 GH/39	
Beschleunigungsspannung	10 kV	
Bildschirmabmessung	8 x 10 cm	Metallhinterlegt
Bildschirmtyp	P31 (GH)	
Raster	Innenraster	Mit Zentimeterteilung und 2 mm-Teilung auf der vertikalen Mittelachse
Rasterbeleuchtung	Deutlich sichtbar unter normalen Lichtbedingungen und kontinuierlich einstellbar	
Ausrichtung der Schreibspur	Schraubenziehereinstellung auf der Frontplatte	
Fokussierung	Automatische Einstellung	

1.2.2. Vertikaleingang

Frequenzbereich	DC ... 60 MHz AC 10 Hz ... 60 MHz	
Anstiegzeit	< 6 ns	
Impulsverformungen	± 3 %	Gemessen in Y-Dehnung mit einem Testimpuls von 8 Teil; Anstiegszeit 1 ns; Frequenz 1 MHz (ausser die ersten 0.2 cm gemessen vom Mittelimpuls)
Vertikalablenkung		
Ablenkkoeffizienten	10 mV/Teil ... 50 mV/Teil	12 kalibrierte Stufen in 1-2-5 Folge
Fehlergrenze	± 3 %	±5 % in Y-Dehnung
Stufenloser Einstellbereich	1 : > 2.5	
Eingangsimpedanz	1 MΩ // 25 pF	
Kopplung	AC-0-DC	
Maximal zulässige Eingangsspannung	± 400 V	Gleichspannung + Spitzenwert einer Wechselspannung
Darstellungsarten	A allein B allein addiert A und B	Kanal B kan invertiert werden

Gleichtaktunterdrückung	100 : 1	Bei 2 MHz maximales Gleichtaktsignal 8 Teilungen
Dynamischer Bereich	2x Spannungsbereich	
DC-Offset	± 4 x Spannungsbereich	
Max. Abtastrate	> 50 MHz	
Sichtbare Signalverzögerung	10 ns	siehe auch "Verzögerung"

1.2.3. Zeitbasis

Zeitkoeffizienten		
Nur wiederholend	5 ns ... 0.2 µs/Teil	
Direkt	0.5 µs ... 0.2 s/Teil	
Rollfunktion	0.5 s ... 60 min/Teil	
Koeffizientenfehler	< 2 %	4 % Kombiniert mit Verzögerung in "REPETITIVE ONLY"
Auflösung	25 Abtastungen/Teil	

1.2.4. Triggerung

Triggerquelle	A B EXT EXT: 10 Netz	
Triggerempfindlichkeit		
Intern	0,3 Teil 0,15 Teil	bei 60 MHz bei 40 MHz
Extern	0,3 V 0,15 V	bei 60 MHz bei 40 MHz
Ext : 10	3 V 1,5 V	bei 60 MHz bei 40 MHz
Triggerflanke	+ oder –	
Triggerungsarten	Automatisch DC AC TV-Bild (1/1 Bild)	
Pegelbereich		
Autom.	Proportionell mit dem Spitze-Spitzewert des Triggersignals	
AC/DC	± 3 Teil	
Verzögerung		
Bereich	–9 ... +9999 Teil 0 ... 100 Teil	0.2 s ... 0.5 µs/Teil 0.2 µs ... 5 ns/Teil
Genauigkeit	±2 mm oder 0.01 % ±2 Teil + sichtbare Verzögerung	0.2 s ... 0,5 µs/Teil 0.2 µs ... 5 ns/Teil
Eingangsimpedanz	1 MΩ // 25 pF	
Maximale Eingangsspannung	± 400 V	Gleichspannung + Wechselspannungs Spitzenwert

1.2.5. Speicher

Speicheranzahl	4	1 Akkumulator Speicher und 3 STO Speicher
Auflösung, horizontal	1 : 250	
Auflösung, vertikal	1 : 250	

1.2.6. Betriebsarten

Einmalig	Auffrischung des Akkumulator Speichers erfolgt, sobald der Triggerpegel erreicht und die mit der Triggerverzögerung eingestellte Zeit vorüber ist. Das Signal wird entsprechend der Position der Triggerverzögerung gespeichert. Während der Wartezeit wird der Akkumulator dargestellt und die LED "NOT TRIG'D" leuchtet auf.	0.5 µs ... 0.2 s/Teil
Wiederholend	Das Signal im Akkumulatorspeicher wird auf dem Bildschirm dargestellt. Nach Verstreichen der mit der Triggerverzögerung eingestellten Zeit wird der Speicher mit neuer Information überschrieben.	5 ns ... 0.2 s/Teil
Rollfunktion	Signal wird Punkt für Punkt an der rechten Bildschirmseite aufgebaut und bewegt nach links. Wenn der Akkumulator vollständig gefüllt ist, wird die Information an Register 3 übergeben dann nach 2 und 1 und danach in den Akkumulator. Hiernach endet die Rollfunktion, dies wird von Blinklicht "RUN" angezeigt.	0.5 s ... 60 min./Teil
Mehrfach	4 mal einmalig mit Übertragung in Speicher	0.5 µs ... 0.2 s/Teil

1.2.7. Darstellungsarten

Speicher	Belegt 2 cm Bildschirmhöhe	
Kanaldarstellungs-Kombinationen		
Akkumulator	Je nach Eingangseinstellung	
Register	Information, wie gespeichert im Akkumulator kann für Speicherung in jedes der drei Register gewählt werden und wird nach Eindrücken der DISPLAY-Taste dargestellt.	Die gesamte Information, gespeichert in STO 1, 2 oder 3 kann invertiert werden
Bereich der vertikalen Lag	± 8 Teile	
Vertikale Dehnung	5x	Speicher belegt 10 cm Schirmhöhe. Angezeigt von LED im Darstellungsteil

Horizontale Dehnung	1 : > 2.5	Kontinuierlich
X-Y Einstellung	Ablenkung in X-Richtung lässt sich durch die Zeitbasis oder durch Speicherinhalt über den A-Eingang bewirken	
Speicher Betriebsarten	CLEAR (Löschen)	Akkumulatorspeicher wird gelöscht
	SAVE (3x) (aufbewahren)	Der Inhalt des Akkumulatorspeichers wird im gewählten Register gespeichert.
	WRITE (Schreiben)	Das Eingangssignal wird in den Akkumulatorspeicher geschrieben
	LOCK (Sperren)	Speichersystem gesperrt
Punktverbinden	Drucktaste DOTS	Verändert die normale Darstellungsart (verbundene Punkte) in Darstellung von nur Punkten.

1.2.8. Ausgang PLOT (Aufzeichnung)

Horizontal	1 V/gesamten Skalenumfang	
Vertikal	1 V/gesamten Skalenumfang	
Pen lift (Schreibstiftabhebung)	TTL kompatibel "0" = nicht unterdrückt (Stift aufgesetzt) "1" = unterdrückt (Stift abgehoben)	Offener Koll-Ausgang Max. Belastung 0,5V ; 500 mA
Plotdauer (Aufzeichnungsdauer)	etwa 100 s	
Plotfolge	B Plot nach A Plot	

1.2.9. Interfaces

IEC-Bus	Wahlweise mittels einer Einsteck-Leiterplatte
IEC-Bus	Einstellungen und Ausgang regelbar über Bus-line Steuerung
Local/Remote	Mit IEC-Steckverbindung

1.2.10. X-Y Darstellung

X = t	Von Zeitbasis	
X = A Y = B	Von YA Eingang	Punktverbindung nicht wirksam
Bandbreite	siehe YA	
Genauigkeit	< 5 %	Einschliesslich Röhre
Phasendifferenz	Der Abstand zwischen A entnommenem und B entnommenem Signal beträgt 1/25 Teil	
Lage	0 des gespeicherten A Signals befindet sich in Schirmmitte	

1.2.11. Kalibrierausgang

Frequenz	2.5 kHz
Spannung	3 V
Strom	6 mA

1.2.12. Versorgung

Netzspannung	100 ... 120 V ± 10 % 220 ... 240 V ± 10 %	
Netzfrequenz	50 ... 400 Hz ± 10 %	
Leistungsaufnahme	< 65 W	
Batterie		zum Beispiel
Typ	2 "pen light" Batterien von 1,5 V	2x 1.5 V Lithium SAFT 2x 1.5 V Duracell
Isolation	Die Isolation der Stromversorgung erfüllt die Sicherheitsnorm nach IEC 348 für Klasse I Metallgehäuse-Geräte	

1.2.13. Einflussgrössen

Bemerkung: Die angegebenen Daten gelten nur dann, wenn das Gerät gemäss den offiziellen Prüfverfahren kontrolliert wurde. Einzelheiten, die dieses Verfahren und die Fehlergrenzenkriterien betreffen, können von der PHILIPS-Organisation Ihres Landes oder von N.V. PHILIPS' GLOEILAMPENFABRIEKEN, TEST AND MEASURING DEPT., EINDHOVEN, HOLLAND angefordert werden.

Umgebungstemperatur	+ 5 °C ... +40 °C –10 °C ... +40 °C –55 °C ... +75 °C	Nominaler Betriebsbereich Arbeitsbereich Lagerungsbereich entsprechend MIL 28800 und maximal 24 Std. bei hohen und/oder niedrigen Temp.
Höhe		
max. Arbeitshöhe	5000 m	Erfüllt die Anforderungen nach IEC 68-2-13, Test M
max. Transporthöhe	15000 m	
Feuchte	Erfüllt die Anforderungen nach IEC 68 Db	Das Gerät übersteht 95 % relative Luftfeuchtigkeit über einen Temperaturbereich von 25 °C bis 40 °C (Gerät ausgeschaltet)
Schock	30 m/s^2	In Betrieb; 1/2 Sinus, 11 ms Dauer; 3 Schocks in jeder Richtung, insgesamt 18 Schocks
Vibration	3 m/s^2	In Betrieb; max. 20 min. in jeder der drei Richtungen; 10 min. mit einer Frequenz von 5 - 25 Hz und einer Amplitude von 1,016 mm_{s-s}; 10 min. mit einer Frequenz von 25 - 55 Hz und einer Amplitude von 0,5 mm_{s-s}; zusätzliche 10 min. an der Resonanz der Frequenz mit dem höchsten Amplitudenanstieg. Das Gerät ist befestigt auf einem Vibrationstisch ohne schockdämpfendem Material.

Abmessungen	Länge	460 mm	Ohne Handgriff und Bedienungselemente
	Breite	316 mm	Ohne Handgriff
	Höhe	154 mm	Ohne Füsse Siehe Abbildung 1.2.
Gewicht	etwa 12 kg		

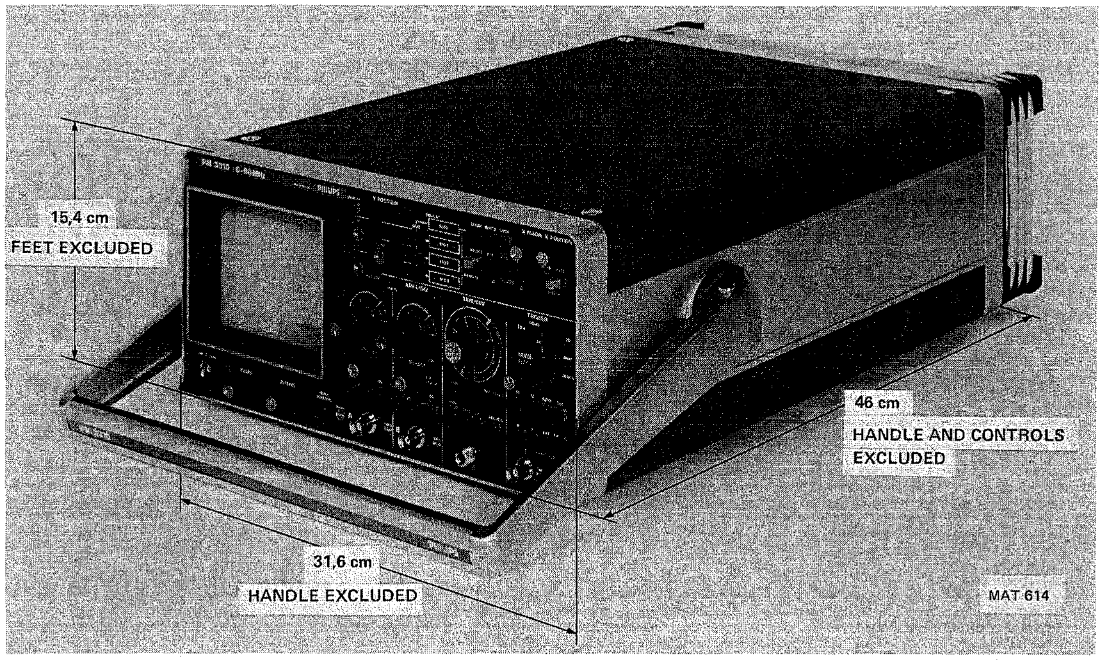


Bild 1.2. Abmessungen

1.3. ZUBEHÖR

1.3.1. Mitgeliefertes Zubehör

- 2x 10:1 Tastkopf, 1,5 m mit Bereichsanzeige.
- 1x Adapter Cal-Buchse / BNC.
- 1x Kontrastfilter, blau.
- 1x Lichtschutztubus PM 9366, faltbar.
- 1x Abdeckhaube für Frontseite mit Aufbewahrungsraum für 3 Tastköpfe.
- 1x Gerätehandbuch.
- 2x BNC - 4 mm Bananenstecker Adapter PM 9051.

1.3.2. Wahlzubehör

- Batterien für Speicher Batterieunterstützung.
- PM 3325 Leiterplatte mit Steckverbindung und Befestigungsmaterial für IEC-Bus Betrieb (IEC-625).
- PM 8960 19" Gestelleinbausatz.

1.4. ZUBEHÖRBESCHREIBUNG

1.4.1. 10:1 Tastkopf (1,5 m) mit Bereichsanzeige

Der mit dem Oszilloskop PM 3310 gelieferte Tastkopf ist dem Standard-Tastkopf PM 8927S vergleichbar. Es ist ein 10x Abschwächer Tastkopf, ausgelegt für Oszilloskope bis 80 MHz, mit BNC Eingangsstecker und einer Eingangskapazität von 14 ... 40 pF ‖ 1 MΩ. Bei Lieferung ist der Tastkopf für die Eingangskapazität des PM 3310 eingestellt.
Der Tastkopf ist mit einem speziellen BNC-Stecker ausgestattet um Bereichsanzeige zu ermöglichen.
Das besagt, dass der Abschwächer - Maszstab des Oszilloskops automatisch an die Tastkopfabschwächung angepasst wird.

Technische Daten

Elektrisch

Abschwächung	10x ±2 % (Oszilloskopeingang 1 MΩ)
Eingangswiderstand DC	10 MΩ ±2 % (Oszilloskopeingang 1 MΩ)
AC	Siehe Kurve, Bild 1.3.
Eingangskapazitat DC und NF	11 pF ± 1 pF (Oszilloskopeingang 1 MΩ ±5 % ‖ 13 pF ± 3 pF)
Eingangsreaktanz HF	Siehe Kurve, Bild 1.3.
Nützbare Bandbreite	Siehe Kurve, Bild
Max. Eingangsspannung	500 V DC + AC_{Spitze}, minderend mit Frequenz Oszillosopeingang 1 MΩ und die zwischen der Tastkopfspitze und dem geerdeten Teil des Tastkopfkörpers angelegte Spannung. Testspannung 1500 V, DC über eine Sekunde, bei 15 und 25 °C Temperatur und maximal 80 % rel. Luftfeuchtigkeit und Meeresspiegelhöhe.
Nullprüfungsknopf Tastkopfgehäuse	Die gleiche Funktion wie der Eingangskopplungs-Schalter des Oszilloskops
Kompensationsbereich	14 ... 40 Pf

Einflussgrössen

Der Tastkopf arbeitet innerhalb der Spezifikationen in folgenden Bereichen:

Temperatur	–25 °C bis +70 °C
Höhe	Bis auf 5000 m (15 000 Fuss)
Übrige Einflussgrössen	Die gleichen wie geltend für das Oszilloskop mit welchem der Tastkopf verwendet wird.

Mechanisch

Abmessungen	Tastkopfkörper 103 mm x 11 mm Ø (max) Kabellänge 1500 mm oder 2500 mm Kompensationsdose 55 x 30 x 15 mm, einschl. BNC
Masse	140 g einschl. Standardzubehör

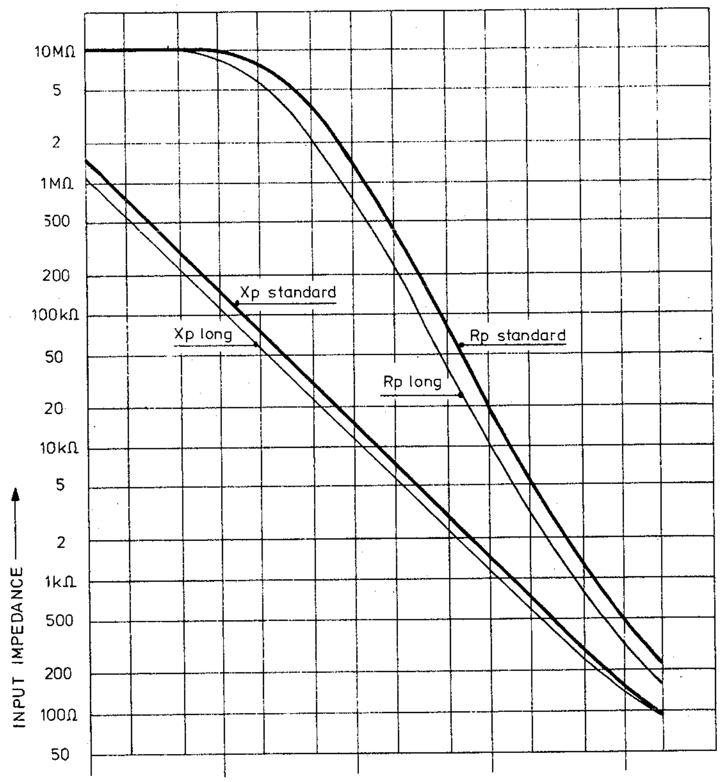


Bild 1.3.

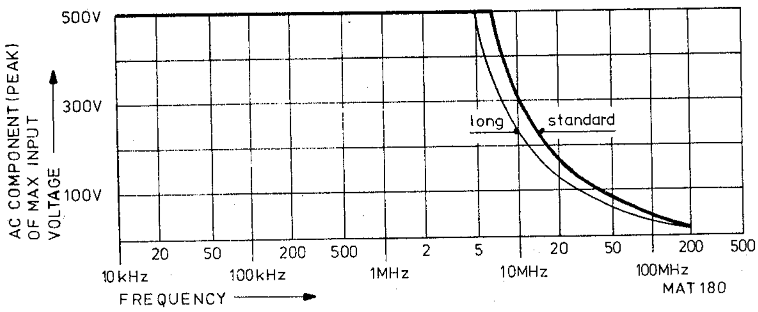


Bild 1.4.

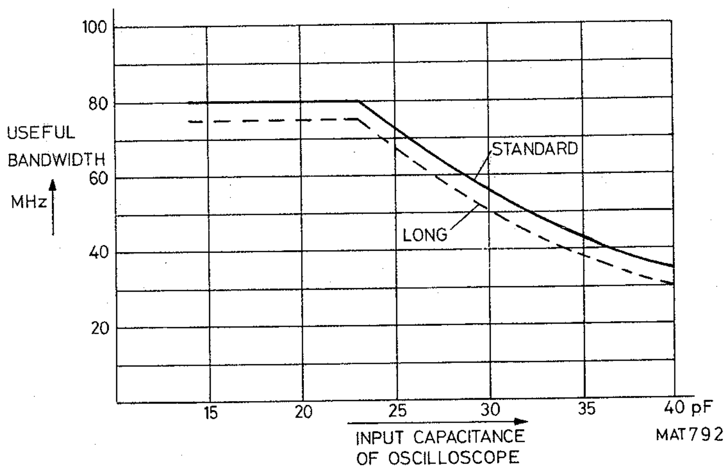


Bild 1.4a.

Einstellungen

Anpassen des Tastkopfs an Ihr Oszilloskop

Der Tastkopf wurde vom Hersteller justiert und überprüft. Zur Anpassung des Tastkopfs an das von Ihnen verwendete Oszilloskop sind jedoch nachstehende Handlungen erforderlich.
Den Meszstift mit der CAL Buchse des Oszilloskops verbinden.
Ein Trimmer C2 (Bild 1.11) ist durch eine Öffnung in der Kompensationsdose zugänglich und einstellbar um ein optimales Rechtecksignal zu erlangen.

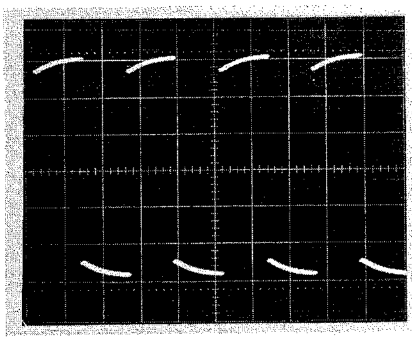


Bild 1.5. Uberkompensation (Einstellung C2)

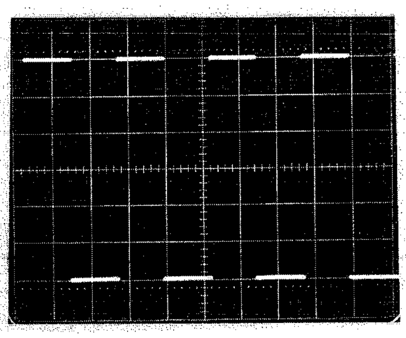


Bild 1.6. Einwandfreie Kompensation (Einstellung C2)

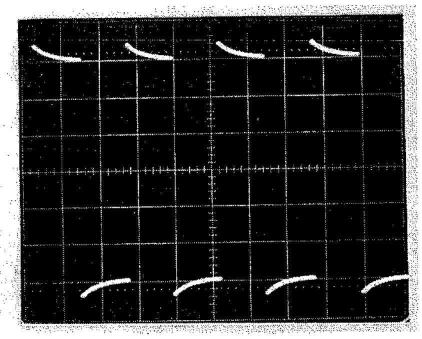


Bild 1.7. Unterkompensation (Einstellung C2)

Einstellen des HF Frequenzgang

Die Einstellung des HF Kenlinienkorrektur-Netzwerks zur Anpassung an den Oszilloskopeingang wurde vom Hersteller vorgenommen.
Für ein optimales Impulsverhalten mit gesondert gelieferten Tastköpfen lässt sich der Tastkopf an das von Ihnen verwendete Oszilloskop anpassen. Spätere Neueinstellung ist nur dann erforderlich, wenn der Tastkopf mit einem Oszilloskop anderen Typs angewandt wird oder nach dem Ersetzen eines elektrischen Bauteils.
Die Einstellung geschieht wie folgt:
Den Tastkopf an einen schnellen Impulsgenerator (Anstiegszeit nicht über 1 ns), der mit seiner charakteristischen Impedanz abgeschlossen ist, anschliessen. Die Kompensationsdose ausbauen. Den Generator für 100 kHz einstellen. R2 und R3 abwechseln einstellen bis ein wie in Bild 1.8. veranschaulichtes Oszillogramm erhalten wird.
Wichtig ist, dass die ansteigende Flanke so steil und das obere Teil so flach wie möglich ist. Unrichtige Einstellungen von R2 und R3 führen zu Impulsverzerrungen wie in Bild 1.9. und 1.10. ersichtlicht.

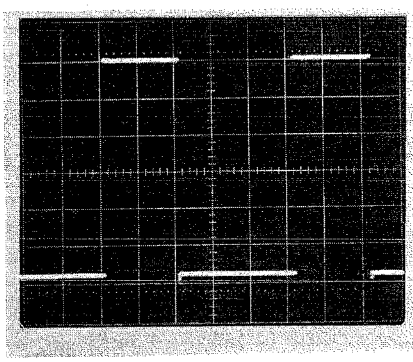


Bild 1.8. Voreinstell-Potentiometer einwandfrei eingestellt

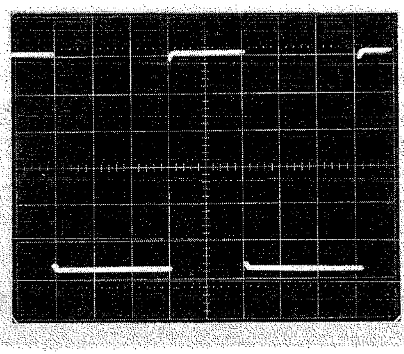


Bild 1.9. Rundung als Folge unrichtig eingestellter Potentiometer

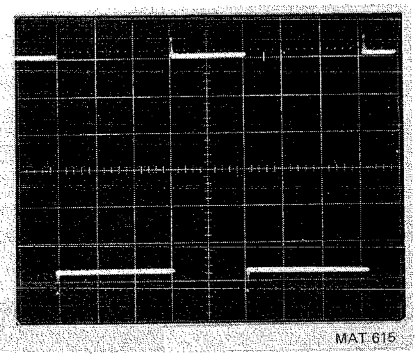


Bild 1.10. Uberschwingen als Folge unrichtig eingestellter Potentiometer

Ausbau

Ausbau des Tastkopfs (Bild 1.11.)

Das vordere Teil des Tastkopfs (11) kann vom rückwärtigen Teil (13) abgeschraubt werden. Pos. 11 lässt sich dann von 12 und 13 entfernen.
Die RC-Kombination (12) ist an 13 festgelötet. Betreffend das Ersetzen von 12 siehe Abschnitt "Ersetzen von Teilen".

Ausbau der Kompensationsdose (Bild 1.11.)

Den gerändelten Kragen zwischen Kompensationsdose und Kabel losschrauben. Das Gehäuse 14 lässt sich nun seitwärts von der Kompensationsdose schieben. Die elektrischen Bauteile auf der Platine sind nun zugänglich.

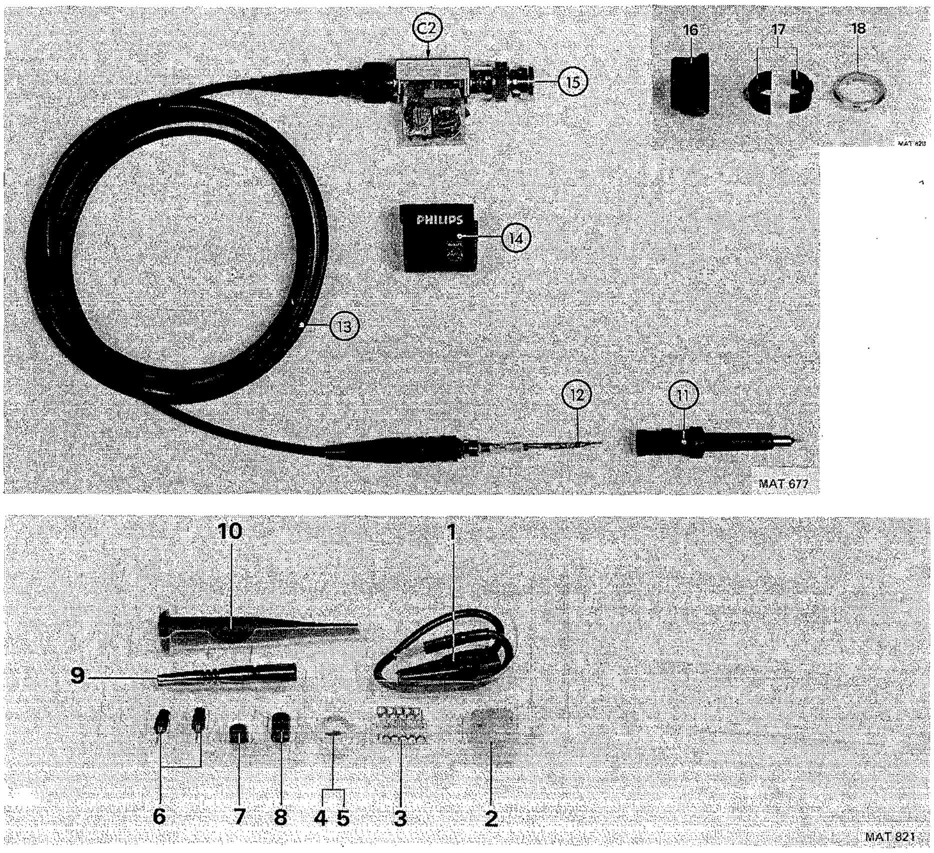


Bild 1.11. Ausbau + Zubehör.

Ersetzen von Teilen

Zusammenbau des Tastkopfs

Ein neues RC-Netzwerk über das Kabelnippel schieben, danach die Kabelader an den Widerstandsdraht löten. Bei Zusammenbau des Tastkopfes muss das RC-Netzwerk genau in der Mitte der Tastkopfspitze liegen.

Ersetzen der Kabelzusammenstellung

Die Kompensationsdose ausbauen
Die Verbindung zwischen dem Ihnenleiter und der Platine loslöten. Das Gehäuse der Kompensationsdose festhalten und das Kabelnippel am Sechskantteil mit Hilfe eines 5 mm Schlüssels lösen. Kabel ersetzen und in umgekehrter Arbeitsfolge wieder befestigen.

BNC Ersetzen

Kompensationsdose ausbauen.
Die Verbindung zur Platine loslöten. Die Kompensationsdose festhalten und den BNC mit einem 3/8" Schlüssel lösen. BNC ersetzen und in umgekehrter Arbeitsfolge wieder befestigen.

Ersetzen der Tastkopfspitze

Die beschädigte Spitze mit einer Flachzange herausziehen. Eine neue Spitze muss fest eingedrückt werden.

Ersatzteilliste

Mechanische Teile (siehe Bild 1.11. und 1.12.)

Pos. 1 bis 10 sind als Standardzubehör im Lieferumfang des Tastkopfes enthalten.

Pos.	Bestellnummer	Anzahl	Bezeichnung
1	5322 321 20223	1	Erdkabel
2	5322 256 94136	1	Tastkopfhalter
3	5322 255 44026	10	Lötklemmen, die als Routinemesspunkte in Schaltungen einbezogen werden können
4	5322 532 64223	2	Markierungsring, rot
5	5322 532 64224	2	Markierungsring, weiss
	5322 532 64225	2	Markierungsring, blau (nicht abgebildet)
6	5322 268 14017	2	Tastkopfspitzen
7	5322 462 44319	1	Isolierkappe für Abschirmung von Metallteilen des Tastkopfes bei Messungen in dicht verdrahteten Schaltungen
8	5322 462 44318	2	Kappe für Messungen an "Dual in Line" integrierten Schaltungen
9	5322 264 24018	1	Wickelstift (Wrap-pin)-Adapter
10	5322 264 24019	1	Feder-Testklemme
11	5322 264 24021	1	Tastkopfumhüllung mit Nullprüftaste
12	5322 216 54152	1	RC-Netzwerk
13	5322 320 14063	1	Kabel-Zusammenstellung
14	5322 447 64016	1	Abdeckkappe
15	5322 268 44019	1	BNC-Steckverbindung
16	5322 532 64277	1	Halter
17	5322 532 64278	2	Ring
18	5322 532 14696	1	Kontaktring
–	5322 492 64765	1	Kontaktfeder
R	5322 116 55552	1	Wiederstand 2K32

Elektrische Teile

Pos.	Bestellnummer	Bezeichnung
C1	–	Teil des RC-Netzwerks (wird nicht gesondert geliefert)
C2	5322 125 54003	Trimmer 60 pF, 300 V
R1	–	Teil des RC-Netzwerks (wird nicht gesondert geliefert)
R2	5322 101 14047	Potentiometer 470 Ω, 20 %, 0,5 W
R3	5322 100 10112	Potentiometer 1 kΩ, 20 %, 0,5 W

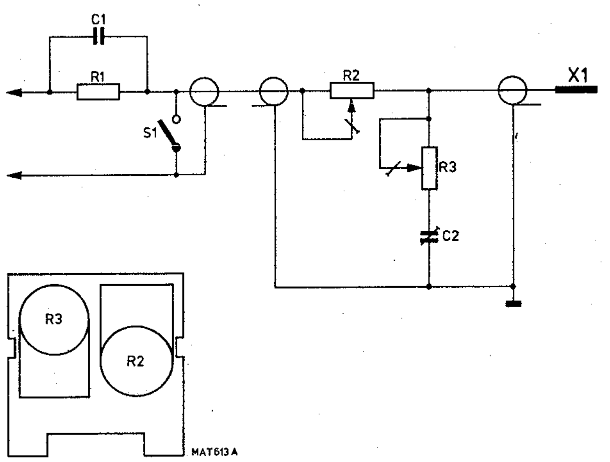


Bild 1.12. Einstellelemente auf der Platine und Schaltbild

1.4.1.1. ANSCHLUSS CAL-BNC ADAPTER

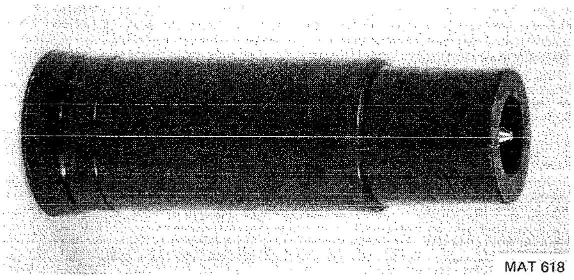


Bild 1.13.

1.4.1.2. BLAUER KONTRASTFILTER

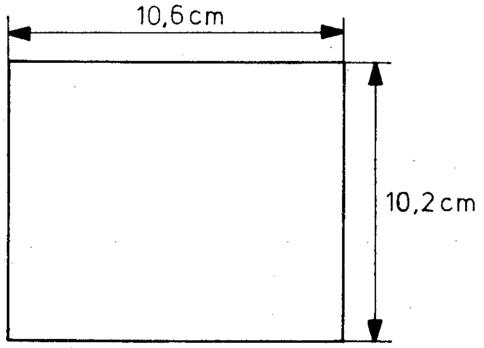


Bild 1.14.

1.4.1.3. FALTBARER LICHTSCHUTZTUBUS

Bild 1.15.

1.4.1.4. FRONT ABDECKHAUBE

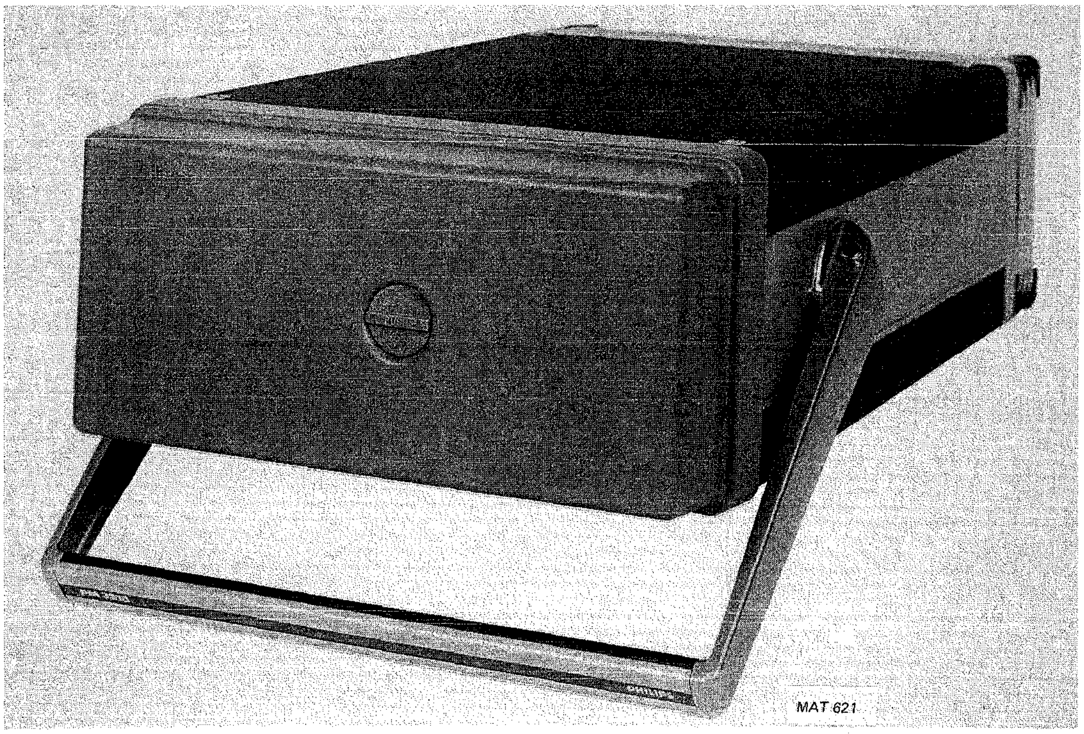


Bild 1.16.

1.4.1.5. ANSCHLUSS BNC ADAPTER 4mm PM 9051

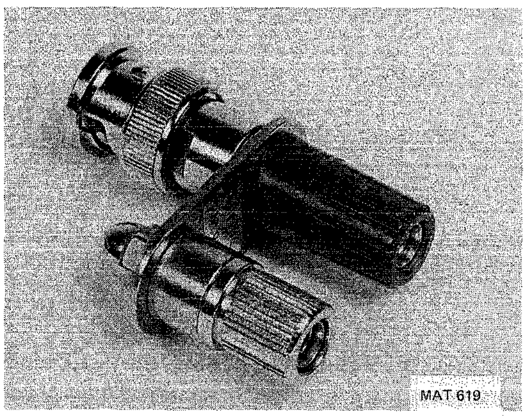


Bild 1.17.

1.4.2. Information betreffend Wahlzubehör

1.4.2.1. BATTERIEN FÜR SPEICHER-BATTERIEUNTERSTÜTZUNG

Das Gerät umfasst eine Batterieunterstützungs-Einrichtung, mit derer Hilfe der Speicherinhalt sowie die Schaltereinstellungen erhalten bleiben wenn Schalter POWER auf OFF steht.
Bei Anwendung von Batterieunterstützung, wird die vor Ausschaltung des Geräts in dem RAMs (Speicher mit wahlfreiem Zugriff) gespeicherte Information wieder dargestellt wenn dass Gerät nach einiger Zeit wieder eingeschaltet wird.

Der Speicher mit der zuletzt gespeicherten Information wird automatisch dargestellt zugleich sind auch die zugehörigen Schaltereinstellungen wieder verfügbar.

Fehlerhafte oder schwache Batteriefunktion wird vom Oszilloskop nicht angezeigt. In einem solchen Fall funktioniert das Gerät wie ohne Speicher-Batterieunterstützung.

Aus technischen Gründen sind keine Batterien eingeschlossen. Falls Speicher-Batterieunterstützung erforderlich ist, sind die Batterien, wie nachstehend beschrieben einzubauen.

Ersetzen der Batterie

WARNUNG: Immer sicherstellen dass das Gerät vollständig vom Netz getrennt ist, bevor Gerätabdeckplatten entfernt werden.
Das Gerät ist durch vier Abdeckungen geschützt: eine Frontplattenabdeckung, eine Rückwand und eine untere und eine obere Gehäuseplatte.
Die Batterien sind nach Abnahme der oberen Geräteplatte zugänglich.

Die Abnahme der Abdeckplatte erfolgt wie nachstehend erläutert:

- Die obere Gehäuseplatte lässt sich nach Lockern der schnell lösbaren Verschlüsse (Befestigungsschrauben an den Ecken der Platte entfernen).Um zu verhindern, dass Verschlüsse auseinanderfallen, nicht mehr als zwei Drehungen lockern.

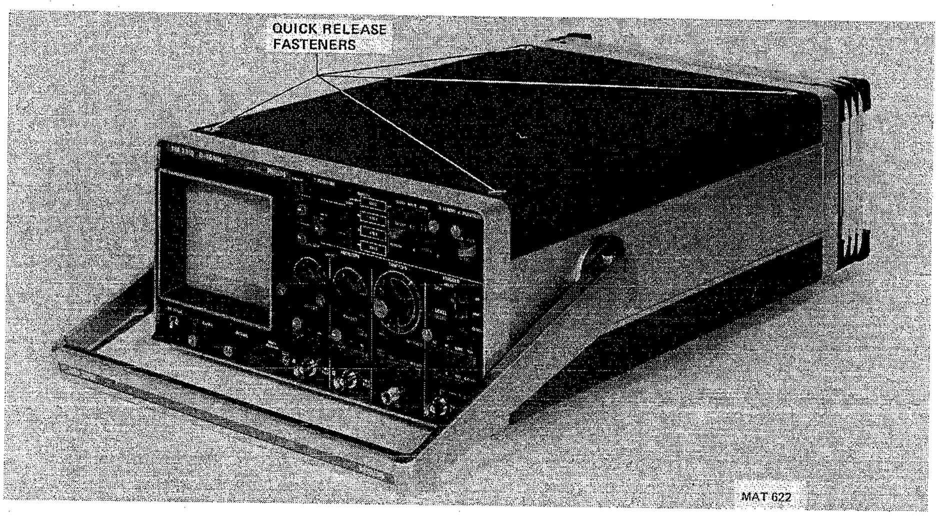


Bild 1.18. Abnehmen der Geräteabdeckungen

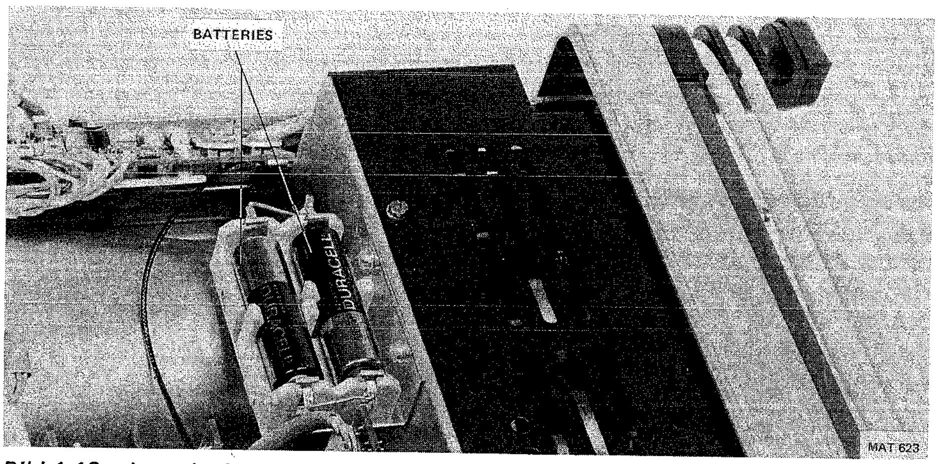


Bild 1.19. Lage der internen Batterie

Empfohlene Batterietypen : 2 x 1,5 V Lithium SAFT oder 2 x 1,5 V Duracell

1.4.2.2. EINBAU ANLEITUNGEN FÜR GESTELLEINBAU ADAPTERSATZ PM8960

Einleitung

PM 8960 ist ein Adaptersatz zur Anpassung des PM 3310 für Einbau in ein 19" Gestell oder Gehäuse. Ein mit Hilfe dieses Adaptersatzes eingebautes Gerät ist ausschiebbar und schwenkbar, wodurch Kontrolle des Geräts erleichtert wird.

Inhalt des Adaptersatzes PM8960

Pos. in Abb. 2	Beschreibung	Anzahl pro Satz
1	Handgriff	2
2	Frontplatte	1
3	Stütze, rechts	1
4	Zylinderschraube M4x12	4
5	Gekrümmter Federring 4,1	10
6	Verrieglungbügel	2
7	Stütze, links	1
8	Stützwinkel	2
9	Teleskopschiene	2
10	Senkschraube M4x10	6
11	Sechskantmutter M4	6
12	Stützwinkel	2
13	Zylinderschraube M5x10	8
14	Gekrümmter Federring 5,1	8
15	Unterlegscheibe 5,3x10	8
16	Tellerfederring 5,3x12	4
17	Senkschraube M5x12	4

Einbauanleitungen

Montieren der Teleskopschiene

- Die Stützwinkel Pos. 8 mit Hilfe der Senkschrauben Pos. 10, der gekrümmten Federringe Pos. 5 und der Sechskantmuttern Pos. 11 an den Teleskopschienen Pos. 9 befestigen. Die Befestigungsbohrungen sind durch eine Öffnung in der Mittelführung der Teleskopschienen zugänglich.
- Stützwinkel Pos. 12 mit Hilfer gleicher Teile Pos. 5, 10 und 11 am rückwärtigen Ende der Teleskopschienen festschrauben.
- Die Zusammenstellung mit Hilfe von Zylinderschrauben, Pos. 13 gekr. Federring, Pos. 14 und Unterlegscheibe Pos. 15 zwischen die Montagestützen des 19" Gehäuses oder Gestells schrauben.

Abnehmen des Tragbügels

- Die oberen und die unteren Geräte-Abdeckplatten entfernen.
- Den um den Griff geklemmten Plastikstreifen abzwängen.
- Die vier Schrauben mit welchen der Griff am Bügel befestigt ist lösen.
- Die beiden Drehzapfenknöpfe im Bügel eindrücken und den Handgriff horizontal nach oben drehen (über das Oszilloskop).
- Den Knopf am rechten eingedrückt halten und den Bügel aus seinen Lagern ziehen.
- Den Griff vom anderen Bügel abnehmen.
- Den Drehzahpfenknopf des linken Bügels eindrücken und diesen horizontal unter den Boden des Geräts drehen.
- Knopf eingedrückt halten und den Bügel aus seinen Lagern ziehen.

Befestigen des Handgriffe und Stützen an der Frontplatte

Die Stützen, Pos. 3 und 7 durch die Löcher in der Frontplatte, Pos. 2 mit Hilfe der Zylinderschrauben, Pos. 4 und der gekr. Federringe, Pos. 5 an die Handgriffe schrauben.

Befestigen der Frontplatte am Oszilloskop

Die beiden Stützen (Pos. 3 und 7) etwas nach aussen biegen und die Frontplatte über die Oszilloskop-Vorderseite schieben. Darauf achten dass der schmale Teil der "Schlüsselloch"-Schlitze in den Stützen 3 und 7 nach oben weist. Falls sie nach unten gerichtet sind, die Kombination Frontplatte/Stützen um 180° drehen und dann wieder um das Oszilloskop schieben. Die grössen Löcher in den Stützen in die Tragbügellager des Oszilloskops einhängen. Die Stützen sperren, indem man die Verriegelungsbügel, Pos. 6 in die Tragbügelschlitze steckt.

Befestigen des Oszilloskops auf den Teleskopschienen

Die Teleskopschienen ganz herausziehen. Die "Schlüsselloch" Schlitze in den Stützen (Pos. 3 und 7) über die Hutmuttern im Vorderteil der Schiene gleiten lassen und das Oszilloskop so weit schieben bis der schmale Teil des "Schlüsselloch"-Schlitzes in den Hutmuttern einrastet.
Das Ganze in das Gestell oder Gehäuse schieben und mit den Senkschrauben, Pos. 17 und Tellerfederringen, Pos. 16 sichern.

Schwenken des Oszilloskops zur Erleichterung der Kontrolle

Das Oszilloskop soweit möglich aus dem Gestell oder Gehäuse ziehen.
Die vorderen "Schlüsselloch"-Schlitze aus ihren Hutmuttern aushängen und das Oszilloskop schwenken bis es gegen Gestell oder Gehäuse anlehnt.
Zurückbringen des Oszilloskops in die normale Lage, erfolgt in umgekehrter Reihenfolge.

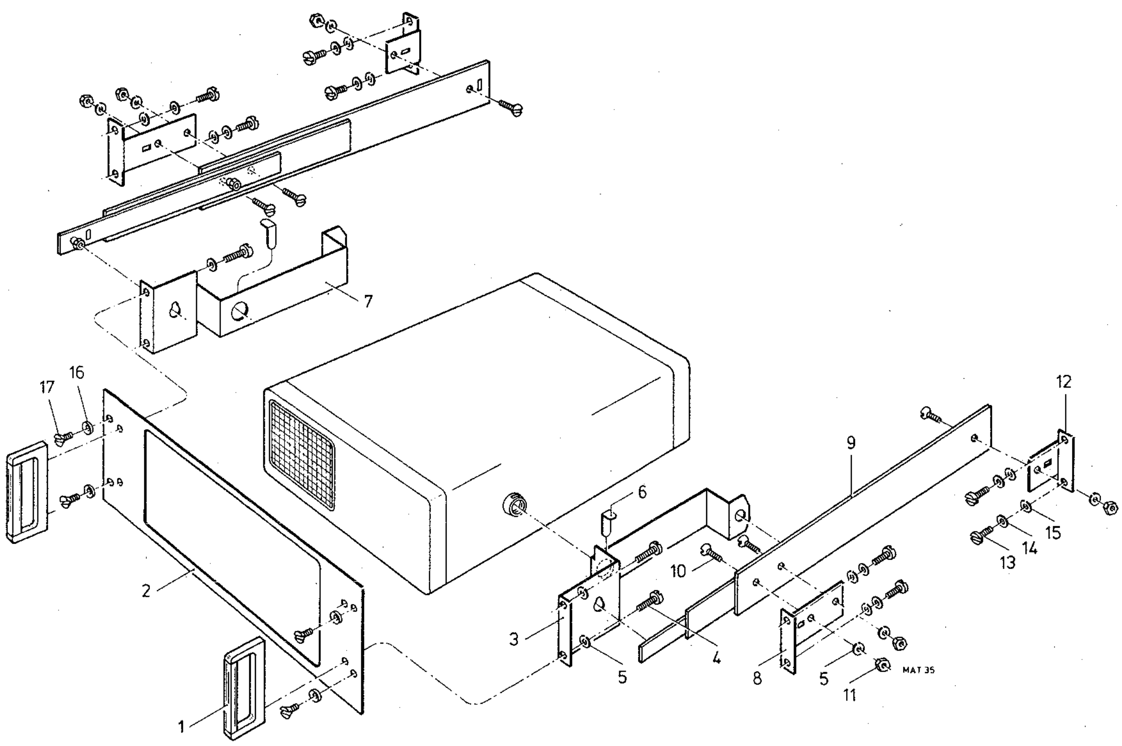


Bild 1.20

1.4.2.3. IEC-Bus-Interface PM 3325

Allgemeines

Die PM 3325, ist ein Mehrzweck-Bus-Interface, entsprechend IEV-TC 66, einschliesslich Selbsttest-möglichkeiten.
Die Adressenwahl erfolgt mit fünf Schaltern (5 niedrigstwertige Bits der ASCII-Zeichen). Eine Karten-identifikation wird ebenfalls ausgeführt.

Interface funktionen

Interfacefunktion	*Symbol*	*Identification*	*Bemerkung*
Source-Funktion	SH	SH1	
Acceptor-Funktion	AH	AH1	
Talker-Funktion	T	T6	
Listener-Funktion	L	L4	
Service Request-Funktion	SR	SR1	PM 3310 kann Funktion Service Request ausführen
Fernb./manuell	RL	RL2	
Device Clear-funktion	DC	DC1	
Parallelabfrage	PP	PPØ	Nicht vorhanden
Device Trigger-Funktion	DT	DT1	
Controller-Funktion	C	CØ	Nicht vorhanden

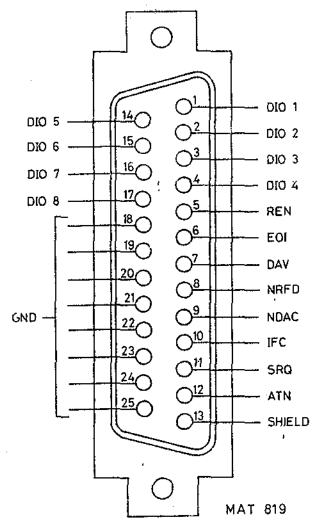
Service Request (SRQ) (Bedienungsanruf)

Der PM 3310 kann zur Anzeige einer besonderen Gerätezustandes ein SRQ senden.
Ein SRQ wird gegeben:
– Wenn Messungen beendet sind
– Nach "POWER ON" oder "RESET" wenn das startverfahren beendet ist
– Wenn ein nicht korrekter Programmcode empfangen worden ist

Nach SRQ kann der Bediener den PM 3310 als "Serial Poll Talker" adressieren; dann wird das Statuswort auf den Bus gesetzt (DI08 . . . DI01).

Aufbau Statuswort

Bit 8		Nicht Gebraucht
Bit 7 . . .	"1"	SRQ wurde vom PM 3310 ausgegeben
	"0"	Kein SRQ ausgegeben
Bit 6 . . .	"1"	Wenn ein Fehler wurde festgestellt
	"0"	Normalzustand
Bit 5 . . .	"1"	Beschäftigt
	"0"	Fertig
Bit 4 . . .		Nicht Gebraucht
Bit 3 . . .		Nicht Gebraucht
Bit 2 . . .		Nicht Gebraucht
Bit 1 . . .		Nicht Gebraucht



Ein-/Ausgabe

Ein-/Ausgabe-System	Bitparallel–Zeichenseriell
Ein-/Ausgabe-Code	ISO 7 bit Code ISO 646 (ähnlich ASCII) Ein-/Ausgabe-Niveaus: L = –0,5 V . . . +0,8 V H = +2 V . . . +5,5 V Logische Niveaus für die 8 DIO - Leitungen: L = 1 H = 0
Steckerbelegung	
Stecker	Philips Steckerleiste Typ F161

Montage

Für Montageanleitung siehe mit dem PM 3325 mitgelieferte Information.

Signalfunktionen

Kurzzeichen	*Bezeichnung*	*Richtung*	*Bedeutung*
DIO 1	Daten Ein/Aus 1	E ⟺ O	Daten Ein-/Ausgabe
DIO 2	Daten Ein/Aus 2	E ⟺ O	Daten Ein-/Ausgabe
DIO 3	Daten Ein/Aus 3	E ⟺ O	Daten Ein-/Ausgabe
DIO 4	Daten Ein/Aus 4	E ⟺ O	Daten Ein-/Ausgabe
REN	Fernbedienung eingesch.	E → O	Fernbedienung eingeschaltet
EOI	Ende oder Identifizierung	E ⟺ O	Ende oder Identifizierung
DAV	Daten gültig	E ⟺ O	Informationszustand
NRFD	Nicht aufnahmebereit für Daten	E ⟺ O	Gerät beschäftigt
NDAC	Keine Datenannahme	E ⟺ O	Zustand Datenannahme
IFC	Rückstellen Interface	E → O	Rückstellen Interface
SRQ	Service-Anfrage	E ← O	Oszilloskop fragt um Service
ATN	Achtung	E → O	Achtung
SHIELD		E – O	
DIO 5	Daten Ein/Aus 5	E ⟺ O	Daten Ein-/Ausgabe
DIO 6	Daten Ein/Aus 6	E ⟺ O	Daten Ein-/Ausgabe
DIO 7	Daten Ein/Aus 7	E ⟺ O	Daten Ein-/Ausgabe
DIO 8	Daten Ein/Aus 8	E ⟺ O	Daten Ein-/Ausgabe
GND	Ende	E – O	Gemeinsam
GND	Ende	E – O	Gemeinsam
GND	Ende	E – O	Gemeinsam
GND	Ende	E – O	Gemeinsam
GND	Ende	E – O	Gemeinsam
GND	Ende	E – O	Gemeinsam
GND	Ende	E – O	Gemeinsam
GND	Ende	E – O	Gemeinsam

E = Externer Controller
O = Digitaler speicher Oszilloskop

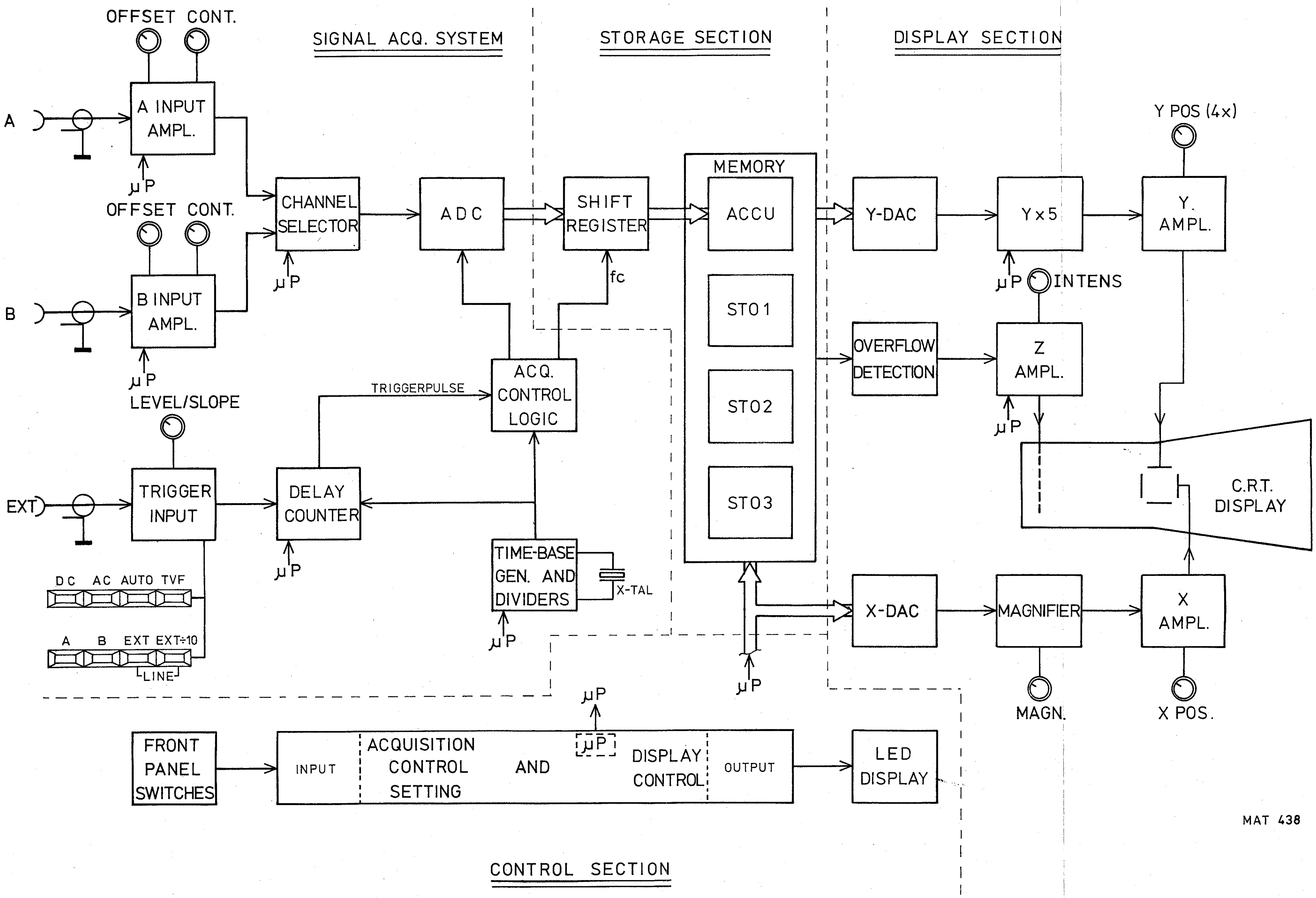
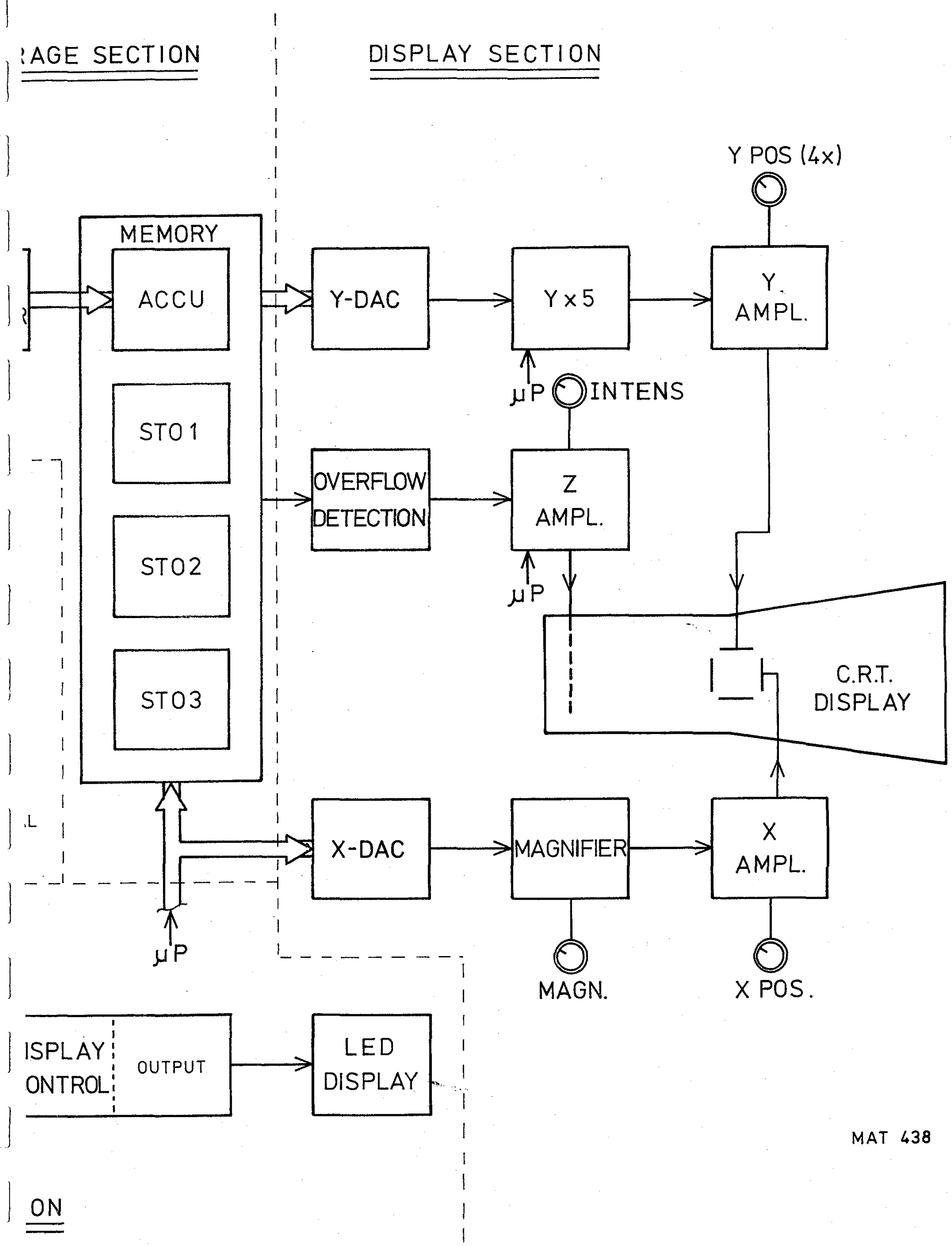


Bild 1.21 Funktionsprinzip.



Adressenwahl

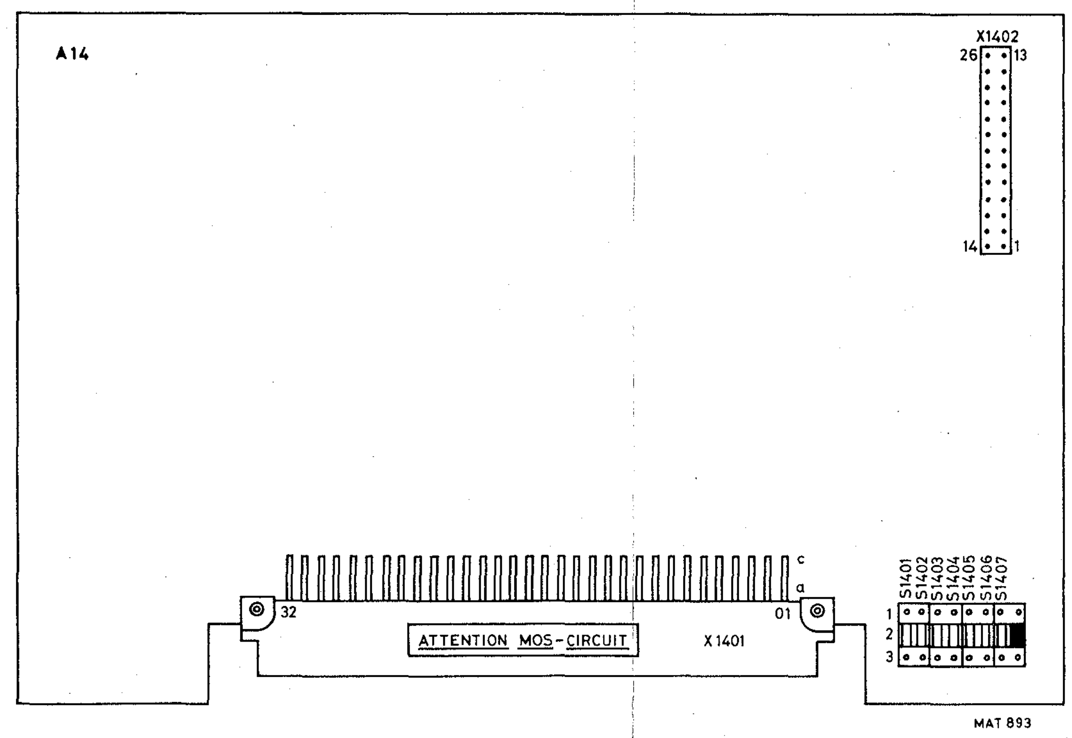
Adresse des IEC-Bus-Interface (Geräteadresse) durch Einstellen von S1401 ... S1405 wählen. S1405 niedrigstwertiges Bit und S1401 höchstwertiges Bit.

Beispiel

	S1401 A5	S1402 A4	S1403 A3	S1404 A2	S1405 A1	
01	0	0	1	0	1	"Listen" Adresse 5
10	0	0	1	0	1	"Talk" Adresse 5

Gesteuert durch System Controller.

"Listen only" -Funktion kann mit Schalter S1407 gewählt werden (Fig. 15).
"Talk only" - Funktionswahl mit Schalter S1406.



Für mehr detailierter Information ziehe das IEC-Bus betrieb Buch in dieses Service Handbuch.

1.5. FUNKTIONSPRINZIP (Siehe Bild 1.21)

Dieser Abschnitt behandelt das Funktionsprinzip des PM 3310 auf Blockschaltbild-Grundlage, wobei besonderer Nachdruck auf jene Teile der Schaltung gelegt wird, die sich von normaler Oszilloskoppraxis unterscheiden, nämlich die digitale Speicherung und Steuerung.

1.5.1. Allgemeines

Das Speicher-Oszilloskop PM 3310 umfasst vier Grundeinheiten:

- Ein Signalerfassungs System.
- Ein Speicherteil.
- Ein Darstellungsteil.
- Ein Steuerteil.

Auf diese Einheiten wird im folgenden näher eingegangen.

1.5.2. Das Signalerfassungs System

Das Signal, welches dargestellt werden soll, wird über einen Abschwächer und einen Verstärker an den Kanalwähler gelegt. Die Einstellungen der Bedienungselemente auf der Frontseite werden vom Steuerteil (des Mikroprozessorsystems) abgetastet. Nach Decodierung wird diese Information dem Abschwächer, dem Verstärker und dem Kanalwähler zugeführt zur Bestimmung der richtigen Einstellungen.

Der Ausgang des Kanalwählers gelangt an den Analog/Digital Umsetzer (ADC) zur Umsetzung eines analogen Signals in digitale Form. Eine Umsetzung beginnt sobald der ADC einen Steuerimpuls von der Acquisition Control Logic (Erfassungs-Steuerlogik), abgekürzt ACL, empfängt. Bei Empfang eines Steuerimpulses wird vom ADC ein momentaner Analogwert des Eingangssignals in ein Digitalwort umgesetzt.

Ein entweder von Kanal A, Kanal B, einem externen Eingang oder von der Netzfrequenz stammendes Triggersignal wird an den Triggerverzögerungs-Zähler geleitet. Nach einer gewissen Zeit, bestimmt von der Voreinstellung des Verzögerungzählers, wird ein Triggerimpuls erzeugt und an die ACL gelegt.

1.5.3. Das Speicherteil

Nach einer vollzogenen Analog/Digital Umsetzung erzeugt die ACL einen Taktimpuls für das Schieberegister. Bei jedem Taktimpuls wird ein digitales Wort des ADC-Ausgangs im Schieberegister gespeichert und alle vorhandene gespeicherte Information verschiebt um eine Stelle.

Die Kapazität des Schieberegisters beträgt 256 Digitalwerte und somit 256 umgesetzte momentane Analogwerte. Sobald vom Triggerverzögerungs Zähler der ACL ein Triggerimpuls übermittelt wird und die ACL hat dem Schieberegister mehr als 256 Impulse zugeführt, ist letzteres mit Informationen gefüllt und die ACL wird aufhören Taktimpulse zu erzeugen.

Das Schieberegisterinhalt ist nun bereit in dem RAM (Speicher wahlfreien Zugriffs) genannt ACCU kopiert zu werden. Die Übertragung der Information vom Schieberegister zum ACCU erfolgt im "handshake" Verfahren (Quittungsbetrieb, damit auf der Elektronenstrahlröhre ein flimmerfreies Bild erzielt wird. Sobald das Kopieren beendet ist, ist das Schieberegister "bereit" und der Vorgang beginnt von neuem.

Die im ACCU gespeicherte Information kann in einen der anderen Speicher (STO 1, STO 2, STO 3) kopiert werden. Jeder dies RAMs kann 256 Bytes digitaler Information aufnehmen. Mit beiden Kanalen auf ON ist die Speicherkapazität, mit 128 Bytes für jeden Kanal, gleichermassen verteilt.

1.5.4. Das Darstellungsteil

Die in den RAMs vorhandene Information kann nun dargestellt werden.
Der Inhalt jedes RAM ist 256 Wörter, jedes Wort bestehend aus 8 Bits. Jedes 8-Bit Wort kann 256 verschiedene Amplituden angeben (d.h. $2^8 = 256$) : Y-Parameter.
Jede Adresse des Speichers entspricht einer bestimmten vertikalen Linie entlang der X-Achse, das heisst die Darstellung von 10 Teilen wird in 256 Linien verteilt.

Da jeder 8-Bit Wert pro Adresse einen Momentanwert in Y-Richtung darstellt, wird eine Bildfläche von 2 vertikalen und 10 horizontalen Teilungen in 256 x 256 Punkte geteilt. Wenn Y x 5 gewählt ist, dann wird diese Fläche auf 256 x 256 Punkte über 10 x 10 Teilungen ausgedehnt.

Ein Adresszähler sendet der Reihe nach 256 verschiedene Adresse (beginnend mit Adresse 0 und endend mit Adresse 255) an die RAMs und zum Digital/Analog Umsetzer (DAC), des X-Systems. Am Ausgang des X-DACs steht eine lineaire Stufenspannung welche über die Dehnungsschaltung an den X-Verstärker zugeführt wird.

Der resultierende Ausgangs des X-Verstärkers gelangt an die Ablenkplatten der Elektronenstrahlröhre.

Auf gleiche Weise werden die 8-Bit Momentanwerte für jede Adresse (d.h. die Y-Information) mit Hilfe des Y-DAC in Analogsignale umgesetzt. Über die Y x 5 Dehnung wird das umgesetzte Signal an den Y-Verstärker gelegt und danach den Vertikalablenkplatten der Elektronenstrahlröhre zugeführt.

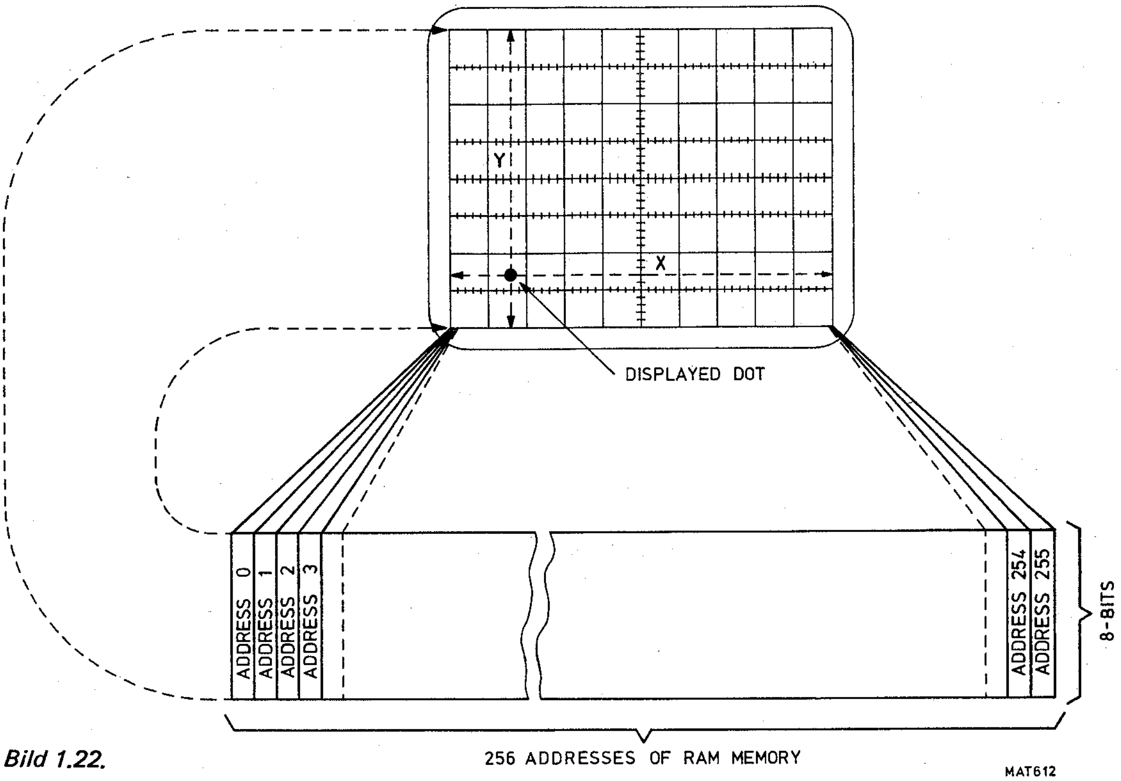


Bild 1.22.

1.5.5. Das Steuerteil

Das Steuerteil eines Mikroprozessors umfasst Speicher, Haltekreise Eingangs- und Ausgangstore und die entsprechenden Logikschaltungen.
Folgende Funktionen werden vom Mikroprozessor gesteuert.

– *Frontplattenschalter*

In einem bestimmten Zeitabstand tastet das Steuerteil alle Schalter (ausser die Triggerquellen- und Triggerartschalter) auf der Frontplatte ab. Die Einstellungen werden entschlüsselt und die entsprechenden Funktionen werden eingestellt.

Zur Vereinfachung des Betriebs werden unrichtige Einstellungen in sinnvolle Einstellungen übersetzt (z.B. würde beide Kanäle OFF in Kanal A ON übersetzt werden).

– *Nachberechnung*

Im Dehnungsbetrieb werden die AMPL/DIV Einstellungen nachberechnet und dargestellt.

– *Darstellungssteuerung*

Das Steuerteil sorgt für die Steuerung der gesamten Darstellung. Das Darstellungsteil besteht aus Elektronenstrahlröhre, Warnlampen, den alphanumerischen LED's und den zugehörigen Schaltungen für die Darstellungselemente.

Die Darstellung auf der Elektronenstrahlröhre wird Punkt für Punkt aufgebaut; das Steuerteil erzeugt die Steuersignale für das Punktverbindungssystem.

– *Handshake-Verfahren (Quittungsbetrieb)*

Eingangssystem (einschliesslich der Schieberegister) und Darstellungssystem besitzen unterschiedliche Betriebszyklen. Um eine flimmerfreie Darstellung zu erzielen bewirkt das Steuerteil Kopplung beider Systeme durch "handshake" Betrieb.

Ausser diesen Standardfunktionen des Oszilloskops überwacht das Steuerteil auch den Plotterausgang und den Betrieb der IEC-Bus Option.

2. INSTALLIERUNGSANLEITUNGEN

2.1. WICHTIGE SICHERHEITSBEDINGUNGEN (DEN IEC 348 VORSCHRIFTEN ENTSPRECHEND)

Vor Anschluss des Geräts an das Netz ist eine Sichtkontrolle vorzunehmen, um eine mögliche Beschädigung des Geräts während des Transports feststellen zu können. Wenn irgendwelche Defekte wahrgenommen werden, darf das Gerät **nicht** an das Netz angeschlossen werden.

REKLAMATIONEN: Im Falle offensichtlicher Beschädigungen oder Mängel oder wenn der sicherheitstechnische Zustand zweifelhaft erscheint, muss beim Überbringer sofort reklamiert werden. Eine Philips Verkaufs- oder Servicestelle muss ebenfalls verständigt werden um Reparatur des Geräts zu ermöglichen.

Vor dem Anschliessen muss der Erdschutzanschluss mit einem Schutzleiter verbunden werden (siehe 2.5. "Erdung").

WARNUNG: Beim Öffnen von Abdeckungen oder Entfernen von Teilen mit Werkzeug können spannungsführende Teile freigelegt werden. Auch können Anschlussstellen spannungsführend und somit Lebensgefährlich sein.

Vor dem Öffnen des Geräts muss das Gerät von allen Spannungsquellen getrennt sein.
Wenn danach eine Kalibrierung, Wartung oder Reparatur am geöffneten Gerät unter Spannung unvermeidlich ist, so darf das nur durch eine Fachkraft geschehen, welche die damit verbundene Gefahren kennt.
Kondensatoren im Gerät können noch geladen sein, selbst wenn das Gerät von allen Spannungsquellen getrennt wurde, die Schaltbilder sind zu beachten.

2.2. ABNEHMEN UND AUFSETZEN DER FRONT-ABDECKHAUBE

Abnehmen

- Den Knopf in der Mitte des Deckels eindrücken und eine viertel Umdrehung nach links drehen (Stellung UNLOCKED).
- Deckel abnehmen.

Aufsetzen

- Den Verriegelungsknopf eindrücken und in Stellung UNLOCKED drehen.
- Deckel an der Vorderseite des Oszillografen befestigen.
- Knopf eindrücken und eine viertel Umdrehung nach rechts drehen (Stellung LOCKED).

Der Raum in der Abdeckhaube dient zum Aufbewahren von Zubehören, wie Tastköpfe, faltbarer Lichtschuztubus, usw.

Zum öffnen der Front-Abdeckhaube die beiden Zungen der Verriegelung drücken und die Innenplatte abheben.

2.3. BETRIEBSLAGE DES GERÄTS

Das Gerät darf in beliebiger Lage betrieben werden. Mit dem Tragbügel nach unten geschwenkt kann das Gerät in Schrägstellung benutzt werden. Die elektrischen Kenndaten nach Abschnitt 1.2. sind für jede Betriebslage des Geräts garantiert. Es ist darauf zu achten, dass die Deckel- und Bodenabdeckung frei sind.
Das Gerät nie auf eine Wärmeerzeugende oder ausstrahlende Oberfläche stellen oder direkter Sonnenstrahlung aussetzen.
Der Tragbügel lässt sich drehen, wenn die Lagerzapfenknöpfe eingedrückt werden.

2.4. EINSTELLEN DER NETZSPANNUNG UND SICHERUNG

Vor Einführen des Netzsteckers in die Netzbuchse ist zu kontrollieren ob das Gerät für die örtliche Netzspannung eingestellt ist.

Die Einstellung erfolgt mit Hilfe des Netzspannungsumschalter (MAINS ADAPTOR SWITCH) an der Geräterückwand.

Der 2-Stellungs-Schalter gestattet Betrieb des Geräts an jeder Spannung zwischen 100 V und 120 V ±10 % (Im Fenster des Spannungsumschalters ist 115 V sichtbar) und zwischen 220 V und 240 V ±10 % (230 V sichtbar im Fenster).

Der an der Rückwand montierte Sicherungshalter enthält eine Sicherung von 2A, träge (4822 253 30025)

Es dürfen nur Sicherungen des vorgeschriebenen Wertes und Typs verwendet werden. Verwendung reparierter Sicherungen und Kurzschliessen des Sicherungshalters ist nicht zulässig. Beim Ersetzen von Sicherungen oder beim Umschalten auf eine andere Netzspannung muss das Gerät von allen Spannungsquellen getrennt sein.

Bemerkung: *Die gleiche 2 A, träge Sicherung ist für jede Stellung des Netzspannungsumschalters verwendbar.*

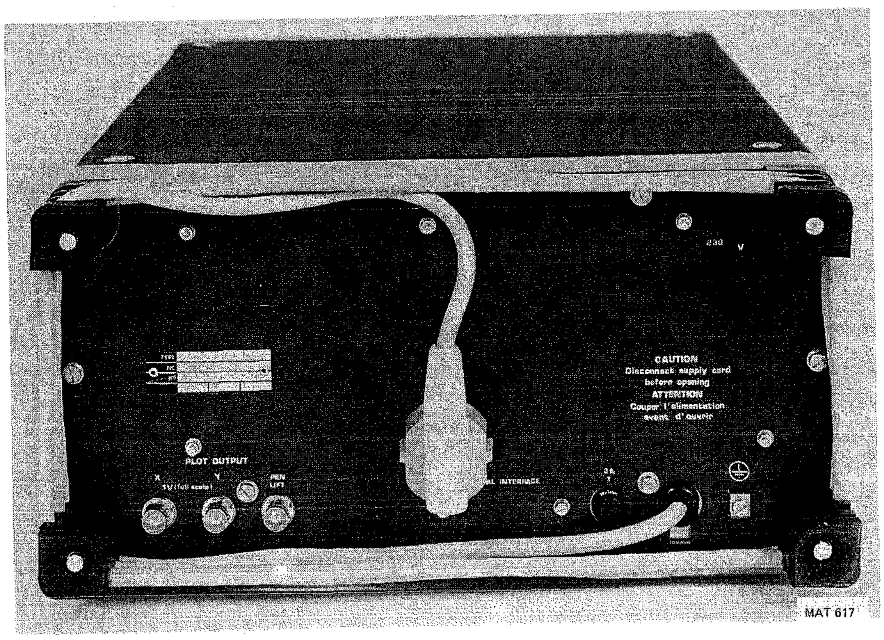


Bild 2.1. Rückanzicht des Oszilloskops mit Netzspannungsumschalter und Sicherung.

Wenn ausser Betrieb, kann das Netzkabel um die Füsse an der Rückseite gewickelt werden.

2.5. ERDUNG

Vor dem Einschalten muss das Gerät auf eine der folgenden Weisen mit einem Erdschutzleiter verbunden werden:

- über den Schutzerdeanschluss;
- über das dreiadrige Netzkabel. Der Netzstecker darf nur in eine Schutzkontaktdose eingeführt werden. Die Schutzmassnahme darf nicht unwirksam gemacht werden, z.B. durch eine Verlängerungsleitung ohne Schutzleiter.

WARNUNG: Jede Unterbrechung des Schutzleiters innerhalb oder ausserhalb des Geräts oder Trennung vom Schutzerdeanschluss ist gefährlich und deshalb unzulässig.

Wenn ein Gerät von kalter in warme Umgebung gebracht wird, kann durch Kondensation ein sicherheitstechnisch gefährlicher Zustand entstehen. Deshalb sind die Erdungsvorschriften genauestens zu beachten.

3. BETRIEBSANLEITUNG

3.1. ALLGEMEINES

Dieser Abschnitt gibt einen Überblick der für die Inbetriebnahme des Geräts erforderlichen Handlüngen und Vorsichtmassregeln. Er beschreibt und erläutert in Kürze die Funktion der Bedienungsorgane auf Frontplatte und Rückwand sowie der Anzeigen. Ausserdem sind hier die praktischen Gesichtspunkte der Bedienung erklärt, dies ermöglicht dem Bedienungsmann eine rasche Bewertung der Hauptfunktionen des Geräts.

3.2. EINSCHALTUNG UND POWER ON-TEST (EINSCHALTTEST)

Nach dem Anschluss des Oszilloskops an das Netz, gemäss Abschn. 2.4. und 2.5., kann es mit Schalter **POWER** eingeschaltet werden.

Der Schalter POWER (Netzschalter) ist gekoppelt an ILLUM auf der Frontplatte unter dem Bildröhrenrahmen. Die zugehörige POWER ON/OFF Anzeigelampe befindet sich neben dem ILLUM/POWER Schalter.

Das Oszilloskop ist sofort nach Einschaltung betriebsfähig. Bei normaler Installierung nach Abschnitt 2 und nach 30 Minuten Anwärmzeit gelten die Abschnitt 1.2. gegebenen Kenndaten.

WARNUNG: Das Oszilloskop darf niemals eingeschaltet werden, wenn eine Leiterplatte entfernt (ausser IEC und Ersatzplatine).
Eine Leiterplatte immer erst dann entfernen, wenn das Oszilloskop zumindest eine Minute ausgeschaltet ist.

3.2.2. POWER-UP Test

Es ist zu beachten, dass bei Einschaltung des Geräts der eingebaute Mikroprozessor automatisch einen Tester einer Anzahl interner Schaltungen auslöst:

- Start-Test.
- PROM-Test.
- LED-Anzeige-Test.
- RAM-Test.

Die Teste starten nach dem Einschalten automatisch. Wenn der Testzyklus beendet ist leuchten alle Warnlampen, Skalenlampen und alphanumerischen Anzeigen etwa drei Sekunden lang; danach schaltet das Oszilloskop auf normalen Betrieb.

Wenn sich beim Test ein Schaltkreis als fehlerhaft erweist, stoppt der Test. Dies zeigt sich wie folgt:

1. Das Gerät funktioniert nicht auf normale Weisse.
2. Einige (jedoch nicht alle) Warnlampen und Skalenlampen leuchten.

In einem solchen Falle empfiehlt es sich das Gerät auszuschalten und nach einigen Sekunden wieder einzuschalten. Falls nach Einschaltung die gleiche Fehlerbedingung erscheint, setzen Sie sich dann mit Ihrer PHILIPS Servicestelle in Verbindung oder überprüfen Sie das Gerät anhand Abschnitt 9.
dess Service-Handbuchs. Wenn eine oder mehrere Warnlampen und Skalenlampen nicht aufleuchten, das Gerät jedoch nach den Tests normal arbeitet, dann ist anzunehmen dass die betreffende Lampe defekt ist.

Wenn das System während des Betriebs blockiert, was durch extrem hohe statische Spannungen verursacht sein kann, dann wird Ausschaltung und Einschaltung automatisch Rückstellung des mikroprozessorgesteuerten Systems bewirken und ist das Oszilloskop wieder betriebsfähig.

3.3. ERKLÄRUNG DER BEDIENUNGSELELEMENTE UND BUCHSEN

Die Bedienungselemente sind teilgruppenweise angeführt und einzeln kurz beschrieben.

3.3.1. Elektronenstralröhrenteil

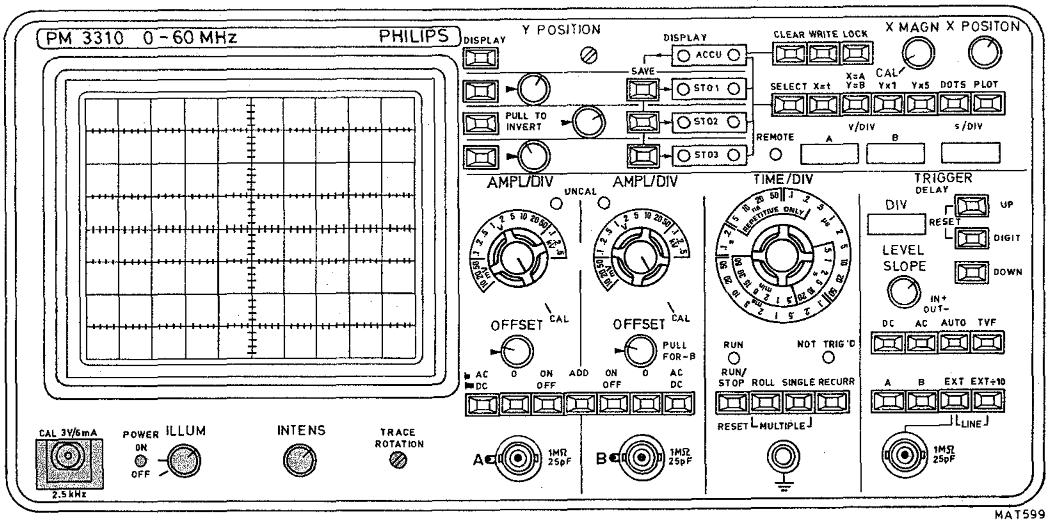
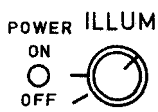


Bild 3.1.

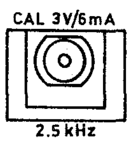


Stufenlos einstellbare Rasterbeleuchtung, zugleich Netzschalter POWER ON/OFF.
Warnlampe zeigt an, dass Netz eingeschaltet ist.

Stufenlose Einstellung der Bildhelligkeit

Bemerkung: Beim PM 3310 ist automatische Fokussierung des Elektronenstrahls vorgesehen, daher erübrigt sich externe Fokussierung.

Voreinstellung zur Ausrichtung der Schreibspur mit den horizontalen Rasterlinien (Schraubenziehereinstellung).



Ausgangsbuchse an der eine 3 V_{S-S}, 2,5 kHz Rechteckspannung zur Verfügung steht. Für Kalibrierung des Vertikalablenkung-Einsteller CAL oder für Frequenzkompensation von Spannungsteiler-Tastköpfen.
Stromschleife mit 6 mA_{S-S} für die Kalibrierung von Strommessköpfen.

3.3.2. Vertikalteil

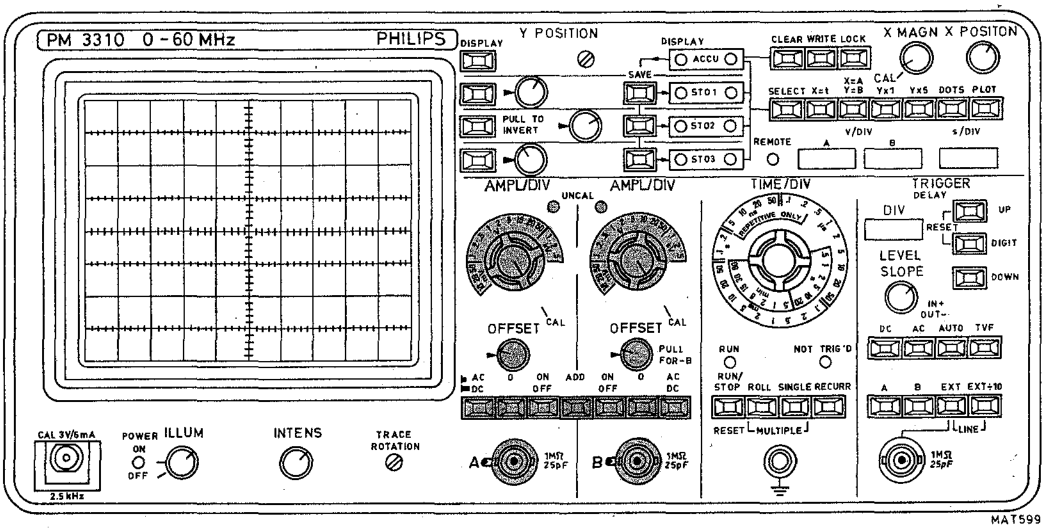
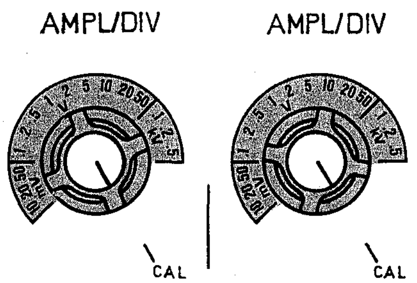


Bild 3.2.

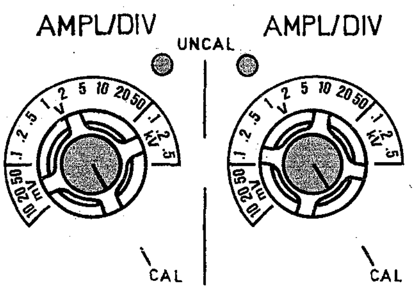


12-Stellungs stufenweise Einstellung der Vertikal-Ablenkkoeffizienten in 1-2-5 Folge.
Bei Einsatz eines 10:1 Tastkopfes mit Bereichsanzeige* erfolgt die Bereichseinstellung von 0,1 V/Teil bis 0,5 kV/Teil automatisch.

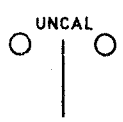
Mit einem 1:1 Tastkopf ist Bereichseinstellung von 10 mV/Teil bis 50 V/Teil möglich.

Unter der AMPL/DIV Aussenknopfskala befinden sich zwei Anzeigelampen. Normalerweise leuchtet die Lampe links, jedoch bei Anwendung eines 10:1 Tastkopfes mit Bereichsanzeige leuchtet die Lampe rechts.

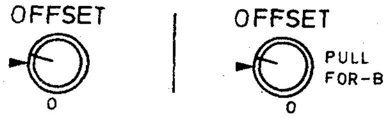
* Tastköpfe mit Bereichsanzeige sind im Lieferumfang des Geräts enthalten.



Stufenlose Einstellung der Vertikalablenkkoeffizienten.
In Stellung CAL ist der gewählte Ablenkkoeffizient kalibriert.

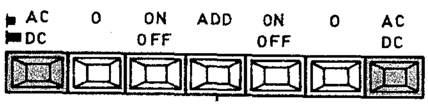


Warnlampe zeigt an dass sich der entsprechende AMP/DIV Schalter ausserhalb der CAL Position befindet.
Eine solche Situation wird in der alpha-numerischen Anzeige durch ein Sternchen (*) angegeben.



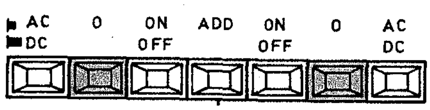
Stufenlose Einstellung zur Signalverschiebung innerhalb des dynamischen Bereichs des Speichers (2 Teile auf dem Bildschirm).
Wenn ein Teil des eingespeisten Signals aus dem dynamischen Bereich des Speichers geschoben wird, dann wird dieser Teil als eine gerade, blinkende Linie auf der Elektronenstrahlröhre dargestellt und zwar oben oder unten des Speicheranzeigeteil, je nachdem ob das Signal aus dem oberen oder dem unteren Teil des dynamischen Bereichs geschoben wurde. Falls das gesamte Signal aus dem dynamischen Bereich geschoben ist wird eine ununterbrochene gerade Linie abgebildet. Der Offsetbereich beträgt ± 4 mal die gewählte Abschwächereinstellung.

Ein Zweiweg Zug-Druckschalter ist gekoppelt an Kanal B OFFSET Einstellknopf zur Umkehrung der Signalpolarität PULL FOR – B (ziehen für – B).
Dieser Knopf wird eingedrückt für NORMAL und gezogen für –B.

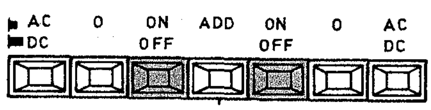


Mit eingedrückter Taste AC/DC wird die entsprechende Y-Eingangskopplung über einen Sperrkondensator bewirkt (AC).

Mit ausgelöster Taste AC/DC erfolgt direkte Kopplung (DC).



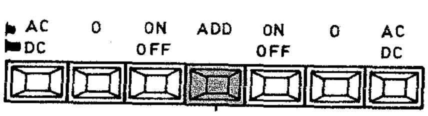
Mit Taste 0 eingedrückt ist die Verbindung zwischen Y-Eingangsbuchse und Eingangsschaltung unterbrochen und die Eingangsschaltung geerdet.



Mit eingedrückter ON/OFF Taste erfolgt die Vertikalablenkung durch das an die Eingangsbuchse des betreffenden Y-Kanals gelegte Signal.

Mit ausgelöster ON/OFF Taste wird die Schreibspur des betreffenden Y-Kanals nicht dargestellt.
Zur Vereinfachung des Betriebs wird Kanal A dargestellt wenn beide ON/OFF Tasten eingedrückt sind (d.h. die Schaltung hält Rechnung mit menschlichem Irrtum!).

Wenn sowohl Kanal A wie B eingeschaltet sind als Folge einer Einstellung von beiden ON/OFF Tasten auf ON dann werden beide Signale im Akkumulator gespeichert. Der ACCU Speicherinhalt wird normalerweise in den oberen zwei Teilen des Bildschirms dargestellt. (Siehe auch "Darstellungsteil").



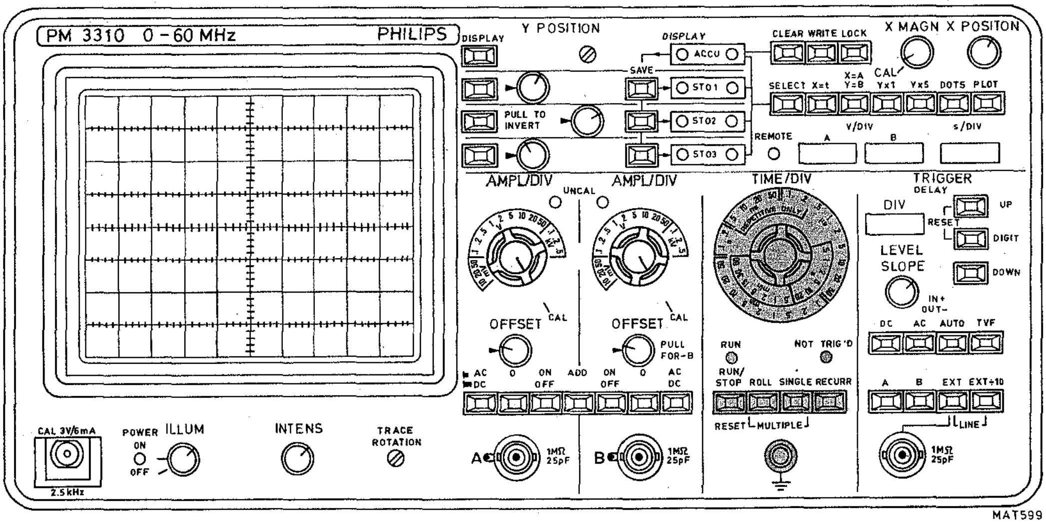
Mit eingedrückter Taste ADD wird die Summe der Signale A und B (A + B) dargestellt.

Kombiniert mit Einstellung PULL FOR – B wird A-B dargestellt. Betriebsart ADD ist unabhängig von ON/OFF Einstellungen wählbar. Das bedeutet dass wenn z.B. Kanal A auf OFF und Kanal B auf ON geschaltet sind, sowohl A wie B OFFSET-Einsteller wirksam sind.

Bemerkung: Wenn alle Tasten ausgelöst sind, wird automatisch Kanal A gewählt.

BNC-Eingangsbuchse, mit Bereichsanzeiger-Eingang.

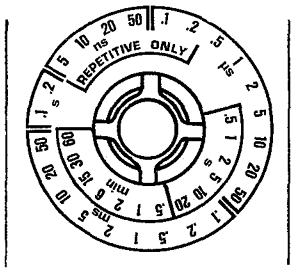
3.3.3. Horizontalteil



MAT599

Bild 3.3.

TIME/DIV



Zeitkoeffizient Stufeneinstellung der Zeitbasis: Drehschalter mit 24 Positionen (ohne Stopp).
Die gewählte Position wird von einer der Anzeigelampen, die sich unter der Skala dieses Knopfes befinden, angezeigt. Bei mit REPETITIVE ONLY gekennzeichneten Einstellungen dürfen nur Signale mit sich wiederholenden Charakters gemessen werden.

Der innere Skalenring ist nur für Betriebsart ROLL bestimmt und wird automatisch angezeigt wenn ROLL gewählt ist.
Die Suche der richtigen Darstellung des Eingangssignals auf dem Bildschirm erfolgt durch Drehen des TIME/DIV Schalters von schnell nach langsam (beginnend bei Position 0,5 ns/Teil) bis man die erste getriggerte Darstellung erhält.

RUN

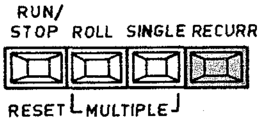
Warnlampe zeigt an dass Betriebsart ROLL wirksam ist und läuft.
Diese Lampe blinkt als Zeichen dass der ROLL-Vorgang beendet ist (siehe Beschreibung der Roll-funktion).

NOT TRIG'D

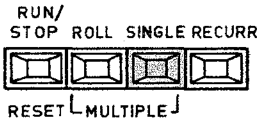
Warnlampe zeigt an dass kein Triggersignal zur Verfügung steht. Nicht leuchten bedeutet :

A). In Betriebsart ROLL/RECURR: Zeitbasis nicht getriggert.

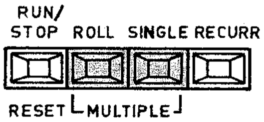
B). In Betriebsart SINGLE/MULTIPLE: Zeichen dass Signal(e) erfasst ist (sind).



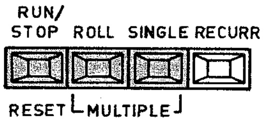
Mit eingedrückter RECURR-Taste wird der ACCU Speicher ständig mit neuen Daten überschrieben. Dieser Vorgang erfolgt in gewissen zeitlichen Abständen je nach Einstellung von TIME/DIV und Triggerverzögerung.



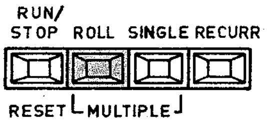
Mit eingedrückter Taste SINGLE wird der ACCU Speicherinhalt nur einmal aufgefrischt, wenn der Triggerpegel erreicht ist und die mit der Triggerverzögerung eingestellte Zeit verstrichen ist.
Diese Auffrischung erfolgt nur nach Eindrücken der RESET-Taste. Das Signal startet gemäss der Einstellung der Triggerverzögerung. Während der Wartezeit wird der Akkumulatorinhalt dargestellt und Lampe NOT TRIG'D ist ON.



Wenn sowohl Taste ROLL wie SINGLE eingedrückt ist, dann ist Betriebsart MULTIPLE gewählt.
Der SINGLE (einmalig) Vorgang erfolgt vier mal, nach einmaligem Eindrücken der RESET-Taste.
Das erste Ergebnis wird in STO 3 gespeichert, das zweite Ergebnis in STO 2, das dritte Ergebnis in STO 1 und das letzte Ergebnis im ACCU-Speicher.



Wenn SINGLE oder MULTIPLE gewählt ist, kann die Zeitbasis durch Eindrücken der RESET-Taste wieder gestartet werden.

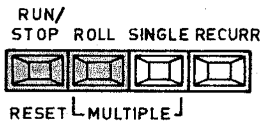


Mit eingedrückter Taste ROLL wird das Signal Punkt für Punkt auf der rechten Seite des Bildschirms aufgebaut und bewegt nach links nach drücken der RUN/STOP Taste. Lampe RUN zeigt an dass Betriebsart ROLL wirksam ist.

Wenn der Akkumulator vollständig gefüllt ist, wird die Information in Speicher STO 3 bewahrt, die nächste Information in Speicher STO 2, die nächste in Speicher STO 1 und die letzte Information im ACCU-Speicher (Lampe RUN bleibt dauernd ON).
Danach stoppt der ROLL Betrieb und Lampe RUN blinkt um dies anzuzeigen.

Betriebsart ROLL kann in den Positionen 0,5 sec/Teil bis 60 min/Teil, angezeigt von der Innenringlampe des TIME/DIV-Schalters, verwendet werden. Wenn der TIME/DIV–Schalter auf eine Position ausserhalb des Bereichs eingestellt ist, dann wird Blinken der Anzeigelampe im Aussenring des TIME/DIV-Schalters dies anzeigen. In diesen Positionen wird der ROLL-Betrieb fortgesetzt, jedoch in 0,5 s/Teil.

Die gesamte Information wird auf dem Bildschirm nur sichtbar, nachdem die vier Darstellungs-Drucktasten für ACCU, STO 1, STO 2 und STO 3 eingedrückt sind.



Eindrücken der CLEAR-Taste führt zu Löschung des ACCU Speicherinhalts und Betriebsart ROLL kann durch Drücken der Taste R/S von neuem gestartet werden. (Siehe auch "Darstellungsteil").

Während des ROLL-Vorgangs (d.h. Lampe RUN dauernd ON) lässt sich der Vorgang durch Drücken der RUN/STOP-Taste stoppen und/oder starten.

Wenn der ROLL-Betrieb durch Drücken der Taste RUN/STOP gestoppt wird, kann die Start/Stopp-Funktion dieser Taste von einem an den externen Triggereingang (TTL-Pegel) gelegtem Signal übernommen werden:
+5 V ($>$ +2,4 V) logisch "HOCH" bedeutet RUN.
0 V ($<$ 0,8 V) logisch "NIEDRIG" bedeutet STOP.

Bemerkung: Zur Vereinfachung des Betriebs wird, wenn alle Drucktasten ausgelöst sind, automatisch RECURR gewählt.

Messerde-Buchse.

3.3.4. Triggerung

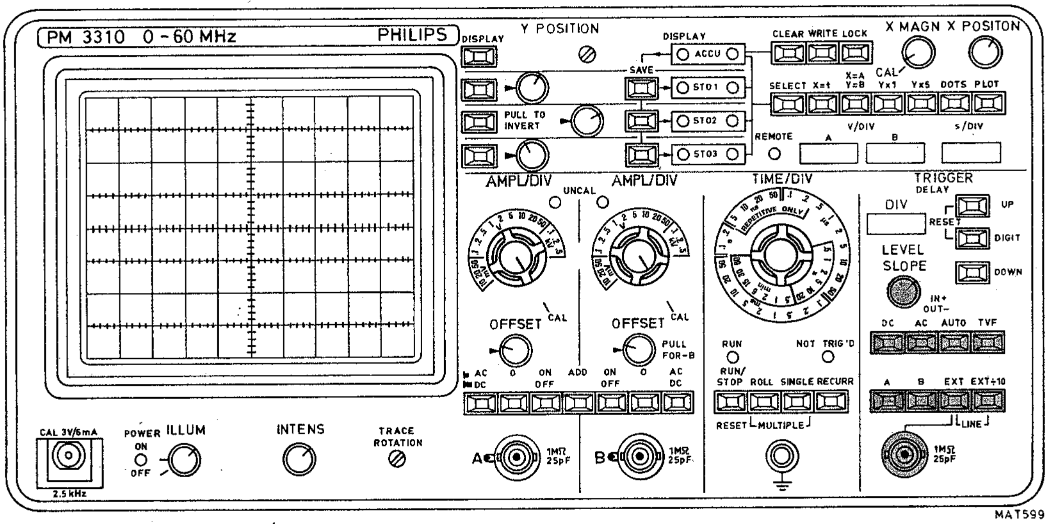
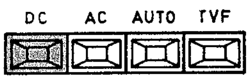


Bild 3.4.

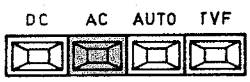
Stufenlose Einstellung des Triggerpunktpegels für das Eingangssignal.

Dieser Einsteller ist gekoppelt an einen Zug-Druckschalter zur Wahl der Triggerung auf der positiv oder negativ gerichteten Flanke des Triggersignals. (IN +, OUT –).

Triggerungsart-Einstellung

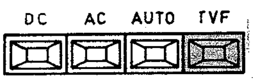


DC eingedrückt:
Der Zeitbasisgenerator wird von einem Triggersignal einschliesslich DC getriggert.
(Trigger Bandbreite DC ... 60 MHz).



AC eingedrückt:
Der Zeitbasisgenerator wird von einem Triggersignal, dessen Gleichspannungskomponente gesperrt ist, getriggert.
(Trigger-Bandbreite 10 Hz ... 60 MHz).

AUTO gewählt:
Die Zeitbasis ist freilaufend in Abwesenheit von Triggersignalen (in dieser Betriebsart ist die Gleichspannungskomponente gesperrt und ist die Trigger-Bandbreite 20 Hz ... 60 MHz).

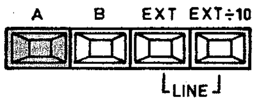


TVF gewählt:
Fernseh-Bild Synchronisation (für CCJR System 625 Zeilen).
*

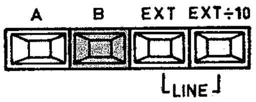
Bemerkung: Zur Vereinfachung des Betriebs wird, wenn alle Drucktasten ausgerastet sind Betriebsart AUTO gewählt.

* Kontrolliere die richtige Flankeneinstellung des Triggersignals (entsprechend dem Fernsehsystem unter Test).

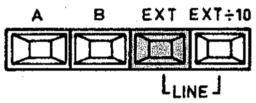
Wahl der Triggerquelle



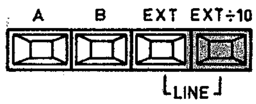
A eingedrückt: Triggerung auf ein internes Kanal A entnommenes Signal.



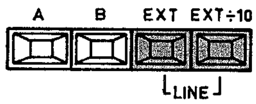
B eingedrückt: Triggerung auf ein internes Kanal B entnommenes Signal.



EXT eingedrückt: Triggerung auf ein externes über die angrenzende Buchse "1 MΩ // 25 pF" angelegtes Signal.

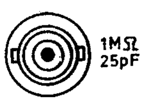


EXT ÷ 10 eingedrückt: Externe Triggerung bewirkt wie obige, jedoch über einen eingebauten 10:1 Spannungsteiler.



Wenn die beiden Tasten EXT und EXT ÷ 10 zugleich eingedrückt sind erfolgt Triggerung auf ein intern der Netzspannung entnommenes Signal (LINE).

Bemerkung: Zur Vereinfachung des Betriebs wird automatisch A gewählt wenn alle Drucktasten ausgerastet sind.



BNC-Eingangsbuchse für externe Triggerung oder für externes RUN/STOP Signal für ROLL-Betrieb.

3.3.5. Triggerverzögerung

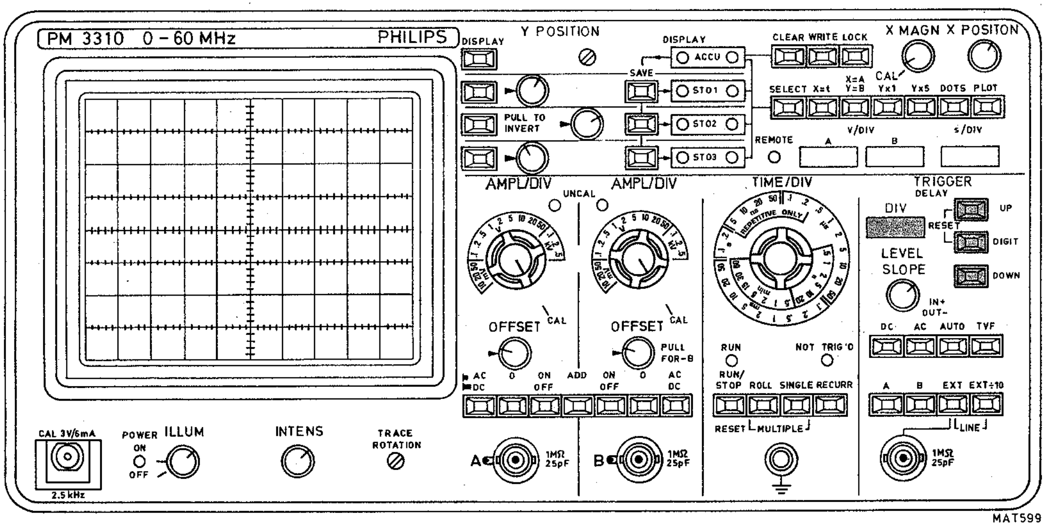
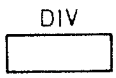


Bild 3.5.



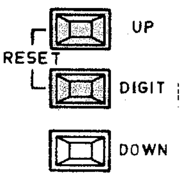
Eine vier-Dekaden Anzeige gibt die gewählte Zeit in Teilen, zwischen dem Triggerimpuls und dem Beginn des dargestellten Signals auf der Elektronenstahlröhre, an.

Diese Triggerverzögerungszeit ist zwischen –9 und +9999 Teilen variabel in den 0,2 s bis 0,5 µs/div Positionen des TIME/DIV Schalters.

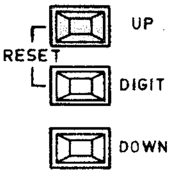
In den Positionen 0,2 µs bis 5 ns/div des TIME/DIV Schalters (nur für sich wiederholende Signale) ist der Verzögerungszeit-Bereich 0 ... 100 Teile.

Bei Einschaltung des Geräts wird die Anzeige automatisch nullgesetzt, ausser bei Anwendung der Speicher-Batterieunterstützung, wobei der vorige Wert angezeigt wird.

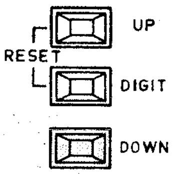
Bei Betriebsart ROLL wird der Text "OFF" angezeigt.



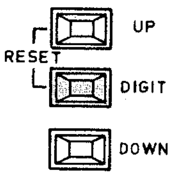
Wenn beide Tasten UP und DIGIT eingedrückt sind, wird die Verzögerungszeit auf Null rückgestellt.
Dies wird in der DIV-Anzeige angegeben.



Die Triggerverzögerungszeit lässt sich durch Eindrücken der Taste UP erhöhen.



Die Triggerverzögerungszeit lässt sich durch Eindrücken der Taste DOWN reduzieren.



Die Dekade in welcher gezählt wird, während die Drucktasten UP oder DOWN bestätigt werden, ist durch Eindrücken der Taste DIGIT wählbar.

Das gewählte Digit blinkt in der DIV-Anzeige.
Durch wiederholtes Drücken der Taste DIGIT werden die Dekaden hintereinander gewählt; das heisst die Ziffern laufen von der Dekade mit niedrigstem Stellenwert zur höchstwertigen und beginnen danach wieder bei der Dekade niedrigsten Stellenwertes.

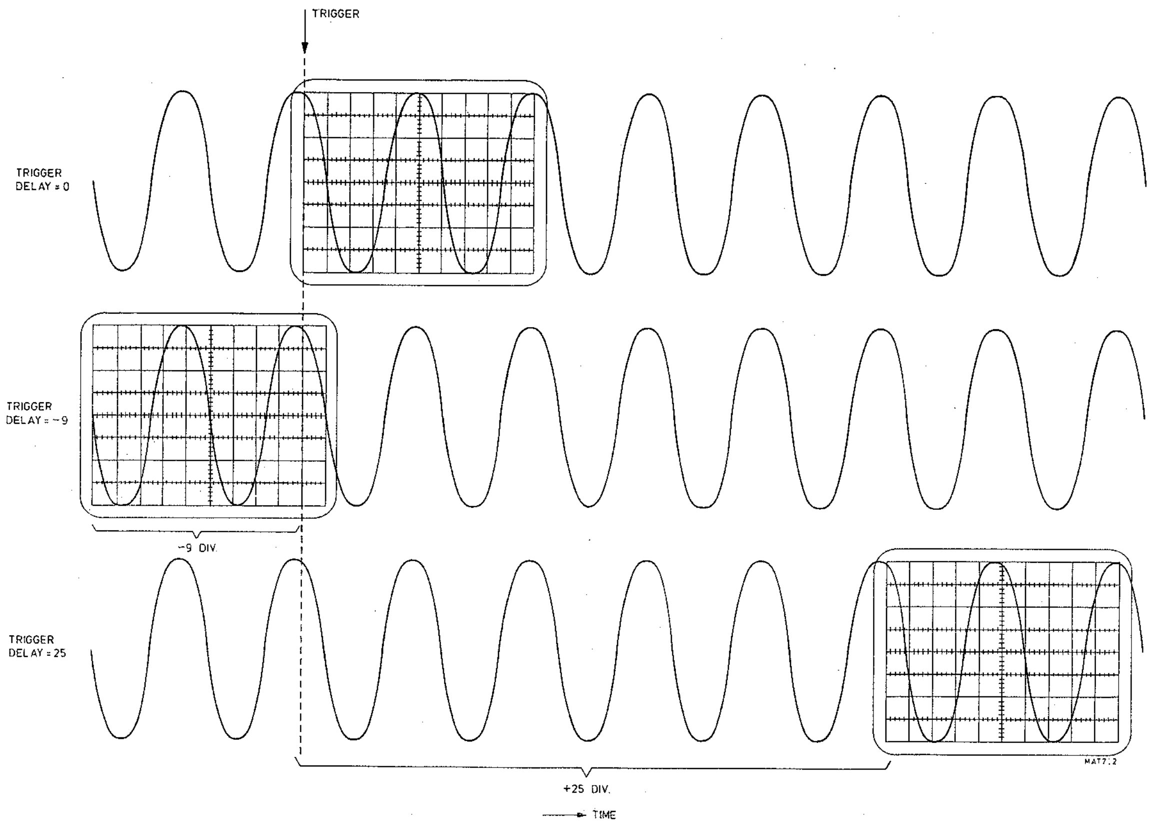


Bild 3.6.

3.3.6. Darstellungsteil

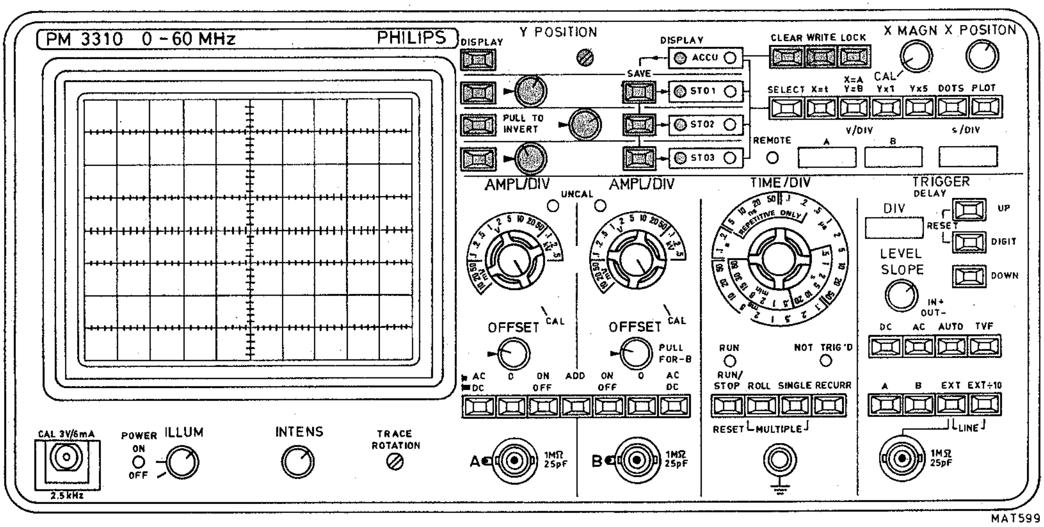
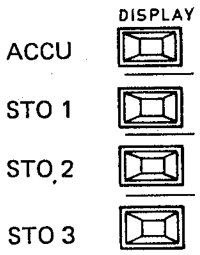
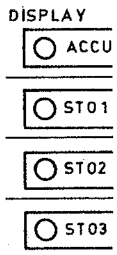


Bild 3.7.

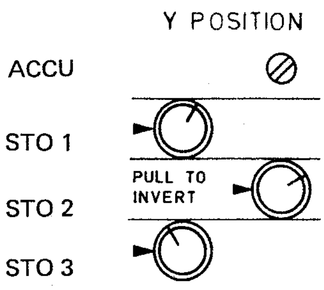


Je nach Einstellung der DISPLAY-Tasten, lässt sich der Inhalt eines oder mehrerer der vier Speicher ACCU, STO 1, STO 2 und STO 3 für Darstellung auf dem Bildschirm wählen.

Wenn keine der DISPLAY-Tasten gedrückt ist, wird von der ACCU LED angezeigt dass ACCU gewählt ist. Diese Einstellung lässt sich durch Eindrücken der SELECT-Taste beeinflussen. In einem solchen Fall und mit allen DISPLAY-Tasten ausgerastet, wird der zuletzt ausgeschaltete Speicher gewählt.



Diese Warnlampen zeigen an welche Speicher für Darstellung auf dem Bildschirm gewählt sind; entweder mit Hilfe der DISPLAY-Tasten oder mit der SELECT-Taste wenn alle DISPLAY-Tasten ausgerastet sind.



Stufenlose Einstellung der vertikalen Lage des Bildes
In der mit  gekennzeichneten Stellung werden die Kanäle gleichmässig über die gesamte Bildschirmfläche verteilt. Jeder Kanal belegt zwei Bildschirmteile. (Siehe Abbildung).
Für die Einstellung der ACCU Lage steht eine Schraubenziehereinstellung zur Verfügung.

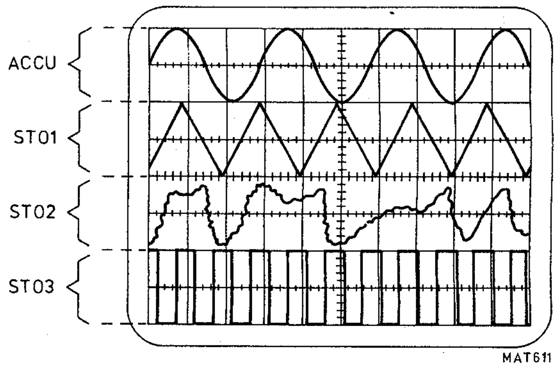


Bild 3.8.

PULL TO INVERT

(Ziehen für Umkehrung)

Ein an die STO 1, STO 2 und STO 3 POSITION Steller gekoppelter Zug-Druckschalter dient zur Umkerung der Signale auf dem Bildschirm.
Eindrücken für NORMAL und ziehen für INVERT.

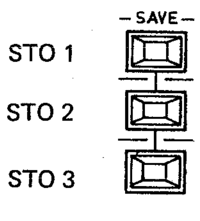
Durch Eindrücken der CLEAR-Taste wird der Inhalt des ACCU-Speichers gelöscht.
Die drei übrigen Speicher können nur gelöscht werden, wenn der gelöschte Speicherinhalt von ACCU in diese Speicher übertragen wird (siehe auch "Funktion der Tasten SAVE).

Der ROLL Vorgang lässt sich von neuem starten, wenn Taste CLEAR und danach RUN/STOP eingedrückt wird.

Mit eingedrückter WRITE-Taste wird das Eingangssignal, nach einem Triggersignal und nach Verstreichen der voreingestellten Verzögerungszeit, in den ACCU Speicher geschrieben. (Siehe Abschnitt 3.3. "Triggerung").

Mit eingedrückter LOCK—Taste ist das gesamte Speichersystem gesperrt, das heisst dass in dieser Betriebsart der Inhalt von ACCU, STO 1, STO 2, STO 3 nicht verändert werden kann.

Bemerkung: Zur Vereinfachung des Betriebs, wird automatisch WRITE gewählt, wenn alle Drucktasten ausgelöst sind.



Der Inhalt des ACCU Speichers wird nach Eindrücken der entsprechenden Taste im gewählten Register STO 1, STO 2 oder STO 3 aufbewahrt.
Zugleich wird die Information für die Einstellungen der Kanäle A und B AMPL/DIV, der TIME/DIV und der Triggerverzögerungs Steller im internen Speicher des Gerätes für alphanumerische.Darstellungszwecke gespeichert.
(Siehe auch V/DIV und s/DIV Darstellung).

3.3.7. Einstellungen der AMPL/DIV und TIME/DIV Schalter

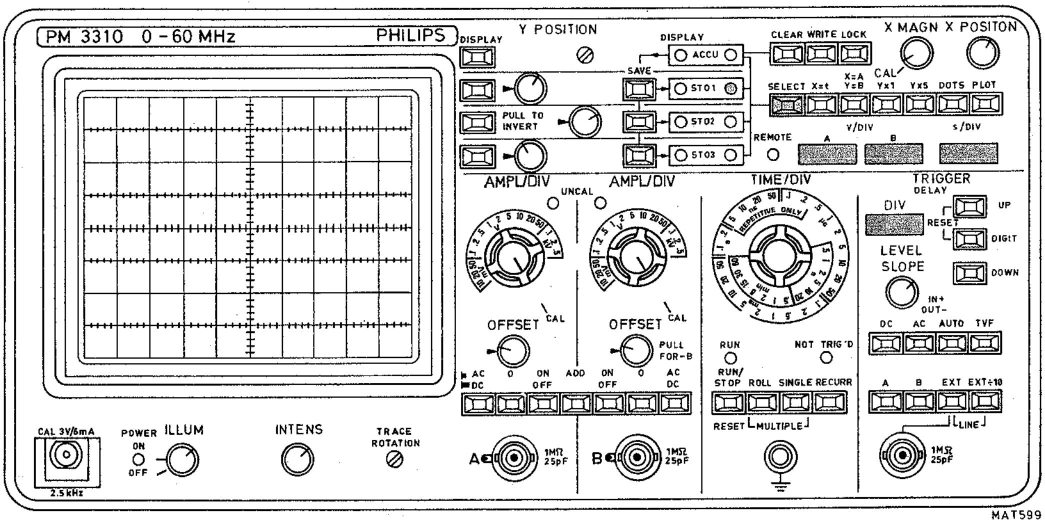
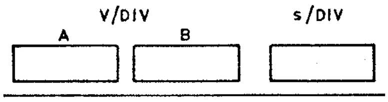
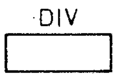
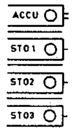


Bild 3.9.





In den Anzeigen werden die Einstellungen der AMPL/DIV und TIME/DIV Schalter und die Triggerverzögerungs Einstellungen für das entsprechende, von einer der Warnlampen angezeigte, Register ersichtlich.



Die Schaltereinstellungen, entsprechend einem der vier Speicher, werden dargestellt wenn Taste SELECT betätigt wird.

Nichtdargestellter Speicher werden übergeschlagen.

Angezeigt wird eine Mantisse (Dezimalteil) und ein Zehner-Exponent.

Dieser Exponent kann sein:

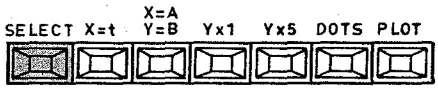
- Leer (0) zur Anzeige von Volt oder Sekunden
- –3 für mV oder ms
- –6 für µs
- –9 für ns

Ein * in der Anzeige gibt an, dass der stufenweise AMPL/DIV Steller während der Speicherung von Signalen in einen der Speicher nicht in CAL-Stellung war, somit wird ein Bereich höherer Empfindlichkeit angezeigt als während der Speicherung.

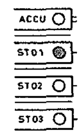
Weitere Anzeigemöglichkeiten sind:

ADD: Betriebsart ADD war wirksam.
SUB: Betriebsart SUB war wirksam (ADD mit Kanal B invertiert).
OFF: Der betreffende Kanal war nicht wirksam.
NOP: Die betreffende Einstellung ist ohne Belang (z.B. nach Einschaltung wenn keine Batterie-Unterstützung angewandt wird).

Bemerkung: Es empfiehlt sich bei Betriebsart SUB und ADD sowohl A wie B AMPL/DIV in die gleiche Stellung zu setzen um eine eindeutige Auswertung des gespeicherten Signals zu ermöglichen.



Betätigung der SELECT Taste ermöglicht die Wahl des Speichers, dessen Massstab-Faktoren dargestellt werden sollen.
In dieser Betriebsart durchläuft das System jene Speicher, die mit den DISPLAY Tasten gewählt wurden.
Der zu einer bestimmten Zeit gewählte Speicher wird von der entsprechenden Warnlampe angezeigt.



Wenn einer oder mehrere Speicherinhalte von STO 1 - STO 2 - STO 3 zusammen mit dem ACCU-Speicherinhalt auf dem Bildschirm dargestellt werden, dann wird die alphanumerische Anzeige durch Betätigung eines der in nachstehender Abbildung gezeigten Schalter automatisch auf ACCU-Einstellungen geschaltet.

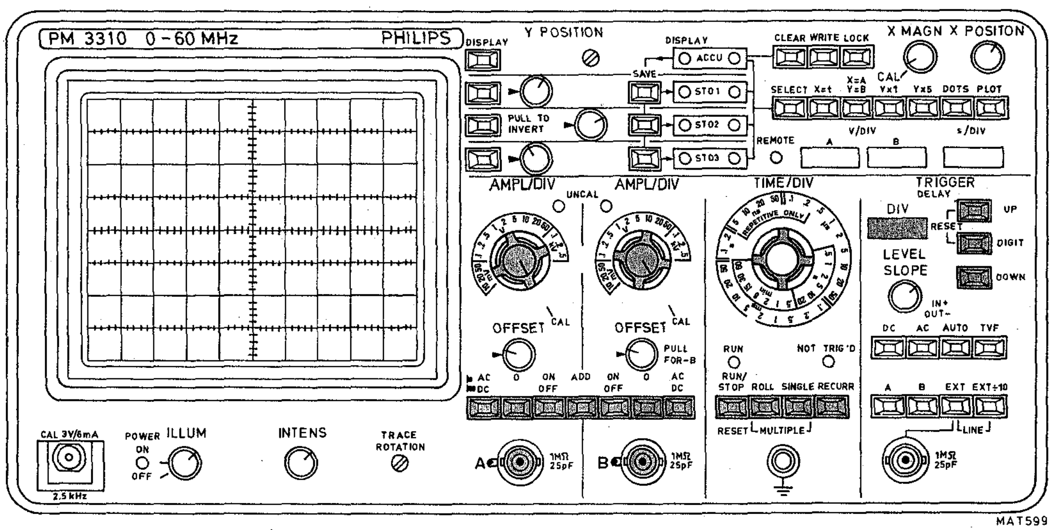
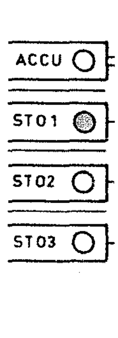


Bild 3.10

Wenn keine der DISPLAY-Tasten eingedrückt ist, dann bewirkt die Anwendung der SELECT-Taste das Durchlaufen ("scrolling") von
– Schirm-Leuchtspur
– Warnlampen
– Massstabfaktor Anzeigen

Die SELECT-Taste erfüllt auch eine Funktion im PLOT Betrieb (siehe Abschnitt 3.3.8. "Darstellungsarten").



Diese Warnlampen zeigen denjenigen Speicher an, auf welchen die Massstabfaktoren und Triggerverzögerungseinstellungen in den V/DIV, s/DIV und DIV Anzeigen bezogen sind.

Nur eine Warnlampe zugleich leuchtet.

3.3.8. Darstellungsarten

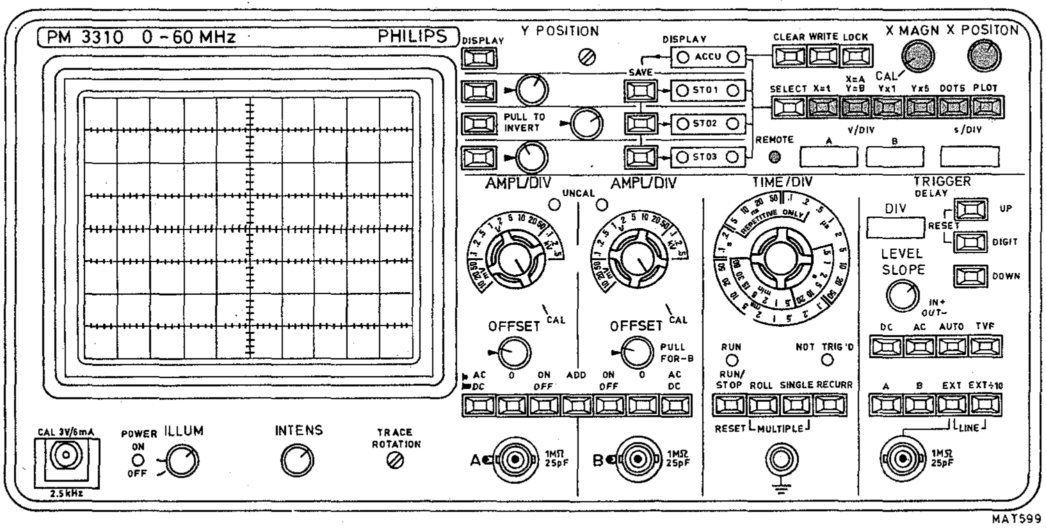
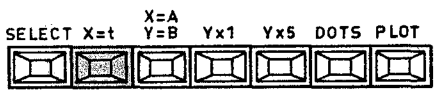
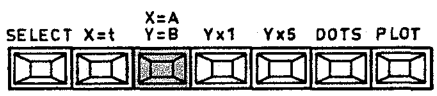


Bild 3.11

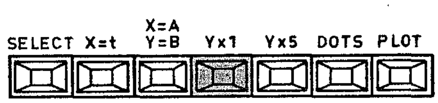


X = t Darstellung stammend von der ursprünglichen Zeitbasiseinstellung (Information vom Speicher).

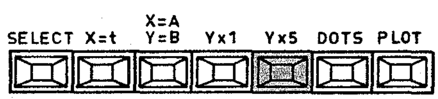


X/Y Darstellung von den A und B Eingängen.

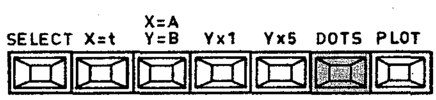
Die A und B Signale werden für Horizontal bzw. Vertikalablenkung verwendet.
Die Darstellung umfasst ein Bild von 10 x 2 Teilen.
Wenn Y x 5 Betrieb gewählt wird erhält man ein Bild von 10 x 10 Teilen, wovon 10 x 8 Teile auf dem Elektronenstrahlröhrenschirm dargestellt werden können.



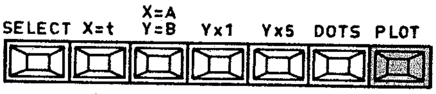
Vertikalablenk-Koeffizient x1.



Vertikalablenk-Koeffizient x5.
Bei dieser Betriebsart ändert sich auch der Massstabfaktor in der V/DIV Anzeige (geteilt durch Faktor 5). Die dargestellten Speicher werden nun auch über die 10 vertikalen Teile abgebildet.
Die Nullinien, falls korrekt justiert, liegen auf der gleichen Basislinie.



Durch Eindrücken dieser Taste (DOTS) verändert die normale Darstellung (Punktverbindung) in eine Darstellung einzelner Punkte.



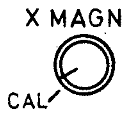
Mit eingedrückter PLOT-Taste stehen an der Geräterückwand Signale für Aufzeichnung mit einem XY Schreiber oder einem Xt Schreiber zur Verfügung.
Der Speicher, welcher die Information enthält die aufgezeichnet werden soll, ist mit Hilfe von Taste SELECT wählbar.

Bei Aufzeichnung A & B Betrieb, wird die B Aufzeichnung nach der A Aufzeichnung gestartet. Ein aufgehellter Punkt auf dem Schirm zeigt den Vortschritt der Registrierung an.

Betreffend Ausgangsspannung von X, Y und PEN LIFT siehe Abschnitt 3.3.9.
Um manuelle Positionierung der Schreibfeder zu ermöglichen ist eine Verzögerung von etwa drei Sekunden vor und sechs Sekunden nach der Aufzeichnungsfolge vorgesehen.
Die gesamte Aufzeichnungszeit beträgt etwa 100 s.

Nach nochmaligem Eindrücken der PLOT-Taste stoppt der PLOT Vorgang.

Bemerkung: Zur Vereinfachung des Betriebs wird automatisch X = t und Y x 1 gewählt, wenn alle Tasten ausgerastet sind.



Stufenlose horizontale Dehnung x 2,5.

Bemerkung: Keine Dehnung in Stellung CAL und keine Ablesung in der s/DIV Anzeige.

Stufenlose Einstellung der horizontalen Lage der Leuchtspur auf dem Schirm.

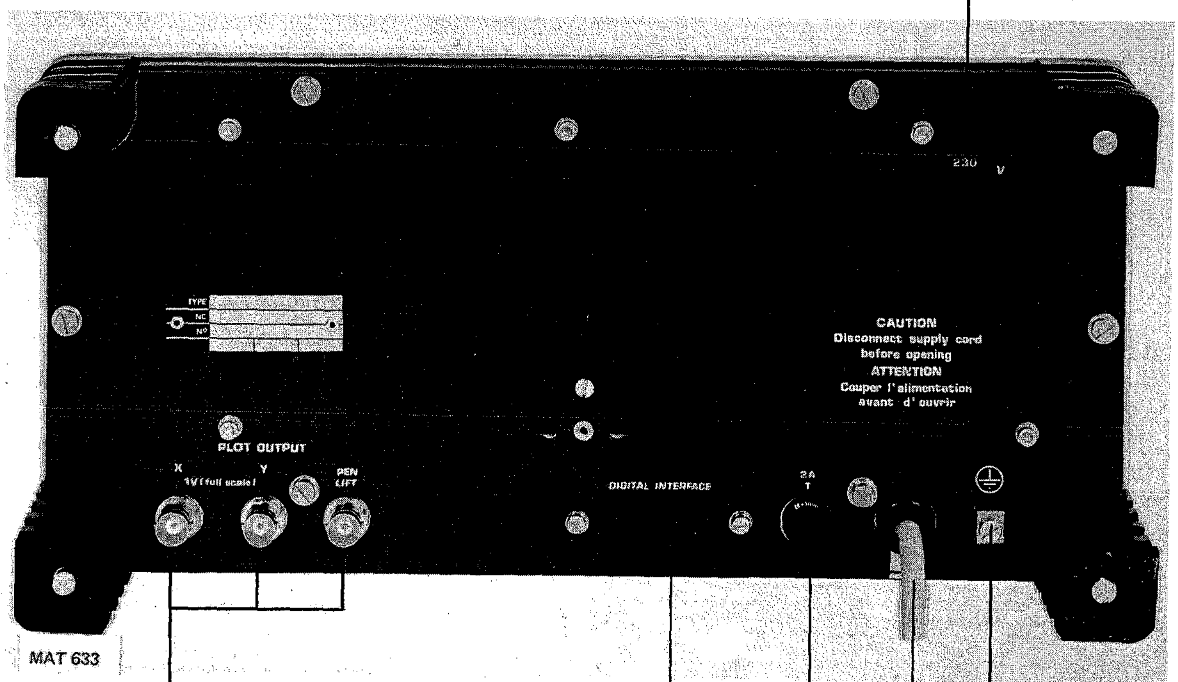
Warnlampe zeigt an dass das IEC-Bus allen Einstellungen der Frontplattenschalter übergeordnet ist.
Rückstellung auf "lokal" wird nur ermöglicht durch entweder die IEC-Bus Steuerung oder durch Aus- und Einschalten des Geräts.

Diese Einrichtung funktioniert nur bei Geräten die mit der Option IEC-Bus PM 3325 ausgerüstet sind. In einem solchen Fall lassen sich Einstellungen und Ausgängen von anderen Geräten ausserhalb des Oszilloskops steuern. (Siehe hierzu das Service Handbuch für Montageanleitung und Auflistung IEC-Bus Betrieb.).

3.3.9. Geräterückwand

Netzspannungs-Umschalter eingestellt für 115 V
(100 ... 120 V ± 10 %)

Netzspannungs-Umschalter eingestellt für 230 V
(220 ... 240 V ± 10 %)



Schutzerde Anschluss

Netzkabel

Netzsicherungshalter (Sicherung 2 A, träge)

Ausschnitt für eine IEC-Bus Buchse (Buchse geliefert mit IEC-Bus Option PM 3325).

X-Y und PEN LIFT Ausgänge für Anschluss eines Schreibers an das Oszilloskop.

- Der X-Ausgang stellt 1 V (Vollausschlag), d.h. 0,1 V pro Bildschirmteil, zur Verfügung.
- Der Y Ausgang stellt 1 V (Vollausschlag) d.h. 0,5 V pro Bildschirmteil, zur Verfügung.
- Der PEN LIFT Ausgang ist ein offener Kollektorausgang mit einer max. Belastung: U_{OL} 0,5 V bei 500 mA kontinuierlich und schaltet den Ausgang auf Null (TTL-kompatibel).

Bild 3.12

3.4. DETAILLIERTE BETRIEBSDATEN

3.4.1. Allgemeines

Vor dem Einschalten überzeuge man sich, dass das Gerät anhand der in Abschnitt 2 gegebenen Hinweise ordnungsgemäss installiert ist und dass die gegebenen Sicherheitsvorschriften inachtgenommen wurden.

Das nachstehend beschriebene Verfahren gibt einen allgemeinen Hinweis ob das Gerät einwandfrei funktioniert und ergibt ein geeignetes Anlaufverfahren bevor Messungen ausgeführt werden.

Es erweist sich als besonders wertvoll für Gebraucher die Oszilloskope dieses Typs nicht kennen.
Das Gerät gestattet die Speicherung eines Signals von Kanal A und eines Signals von Kanal B (einschliesslich der AMPL/DIV, TIME/DIV und Triggerverzögerungs Einstellungen bezogen auf diese Signale) in einem von vier internen Speichern: ACCU, STO 1, STO 2 und STO 3, je nach Wahl.

Bei Normalbetrieb (Y x 1), stehen, wie nebenstehend veranschaulicht, für jeden Speicher 2 Teile zur Verfügung. Mit Steller POSITION in Mittelstellung, sieht das Darstellungsformat wie abgebildet aus.

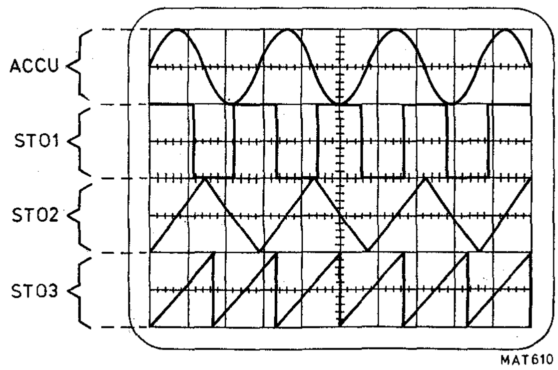


Bild 3.13.

3.4.2. Darstellung des ACCU Inhalts

Zur Darstellung des ACCU-Inhalts sind folgende Einstellungen erforderlich:

- **Keine** Signale angelegt.
- Alle Drucktasten ausgerastet und alle Schalter in CAL Stellung.

Folgende Funktionen sind nun wirksam (siehe Bild 3.14).

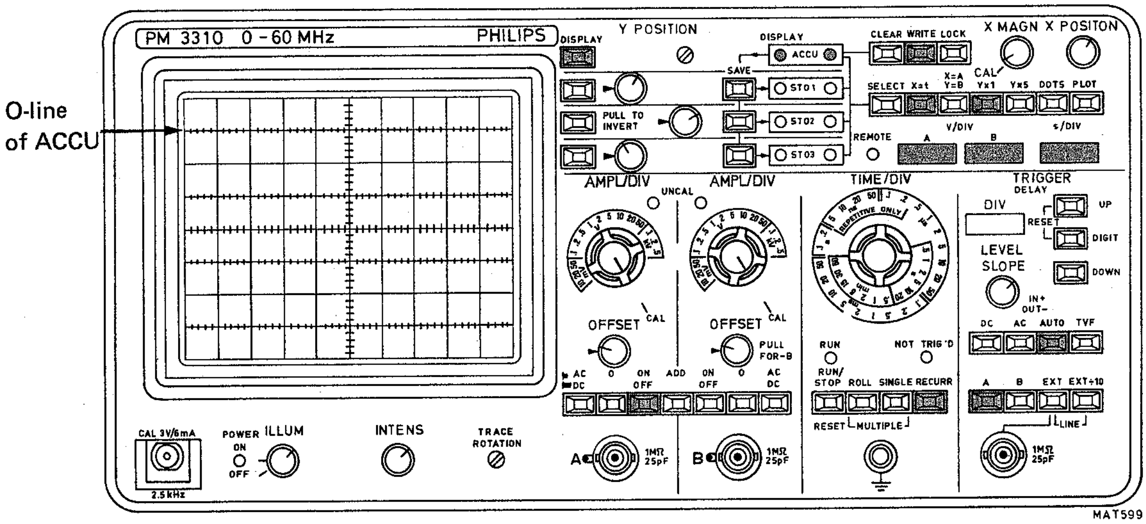


Bild 3.14.

- Schalter POWER auf ON. Sich überzeugen dass die Warnlampe leuchtet und der POWER-UP Test beginnt; siehe Abschnitt 3.2.2.
  Eine Leuchtspur wird nun in den beiden oberen Bildschirmteilen erscheinen.
- Mit Steller INTENS eine geeignete Leuchtstärke einstellen.
- Steller OFFSET von Kanal A derart einstellen, dass die abgebildete Basislinie mit 0-Line des ACCU Darstellungsteils übereinkommt.

Das Oszilloskop ist jetzt zum Empfang eines Eingangssignals bereit, vor weiteren Handlungen ist es jedoch ratsam die Drucktasten wie oben abgebildet ("Ansicht der Bedienungselemente") einzudrücken.

Ein sinusförmiges Signal an Eingang A legen und Schalter in eine geeignete Stellung bringen.

Die einwandfreie Darstellung des Eingangssignals auf dem Bildschirm lässt sich wie folgt er zielen. Schalter TIME/DIV von schnell nach langsam drehen (beginnend bei Position 0,5 ns/div.) bis man die erste getriggerte Darstellung erhält.

Bemerkung 1: Die Einstellung des AMPL/DIV Schalters von Kanal A muss so erfolgen, dass das Eingangssignal nicht mehr als Teile des Schirms bedeckt. Als Hinweis auf Überlauf oder unkorrekte OFFSET Einstellung, bleibt das Signal blinken bis eine einwandfreie Einstellung erreicht ist.

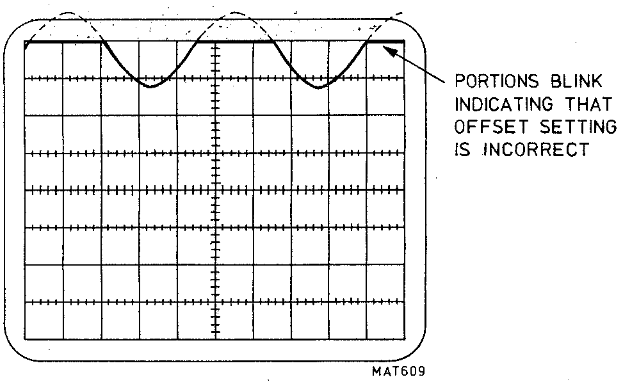


Bild 3.15.

Bemerkung 2: Für volle Bildschirmdarstellung Drucktaste Y x 5 eindrücken. Die Nullinie wird dann automatisch auf die Mittellinie des Schirms gelegt.

Bemerkung 3: Wenn sowohl Kanal A wie Kanal B auf ON stehen und an beide Kanäle Signale gelegt sind, überlagern sich die Signale.

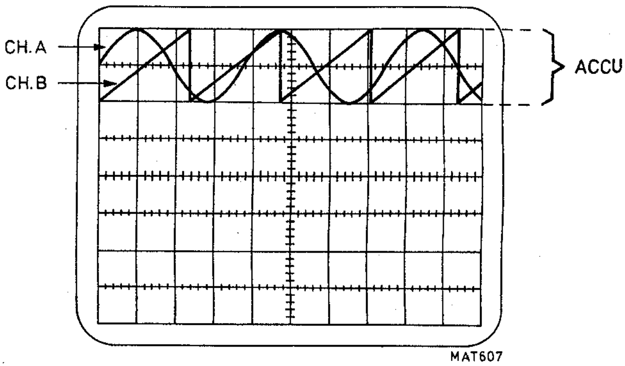


Bild 3.16.

In diesem Fall kann durch Einstellung von Schalter AMPL/DIV und der OFFSET-Steller der Kanäle A und B bewirkt werden dass bei Normalbetrieb (Y x 1) jede Leuchtspur nur ein Teil bedeckt.

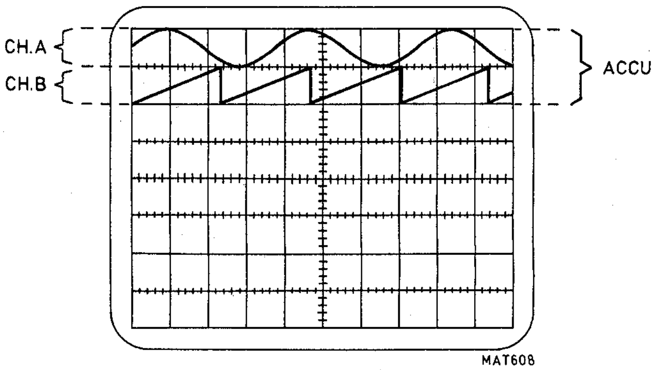


Bild 3.17

Bemerkung 4: Wenn eine oder mehr der übrigen DISPLAY Tasten eingedrückt sind, gibt es zwei mögliche Situationen.

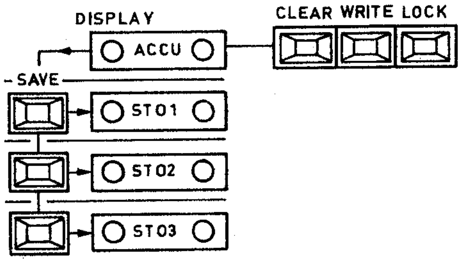
1. *Falls Speicher Batterie-Unterstützung verwendet wird, wird der Inhalt des (oder der) zugehörigen Speicher dargestellt; nämlich der Speicherinhalt von vor der Ausschaltung des Geräts.*
2. *Ohne Batterie-Unterstützung wird auf dem Bildschirm belanglose Information dargestellt und in der alphanumerischen Anzeige erscheint:*

V/DIV A	V/DIV B	s/DIV
NOP	NOP	NOP

DIV
NOP

3.4.3. Speicherung des ACCU Inhalts

Im folgenden wird die Speicherung des ACCU Inhalts in einem der Speicher STO 1, STO 2 oder STO 3 beschrieben.
STO 1, STO 2 und STO 3 sind zur Speicherung des ACCU Inhalts fähig.



– Taste SAVE des für Aufbewahrung der ACCU Information bestimmten Speichers.
– Sich überzeugen dass die Information in den Speicher geschrieben ist, durch die DISPLAY Taste dieses Speichers einzudrücken.

Der Inhalt wird nun auf dem Schirm dargestellt.

Ein Speicher kann gelöscht werden (nur in Betriebsart WRITE) durch Löschung des ACCU Inhalts mit Hilfe der CLEAR Taste und Übertragung des gelöschten ACCU Inhalts in den betreffenden Speicher durch Eindrücken der entsprechenden SAVE Taste. Mit anderen Worten, Löschung eines Speichers durch speichern des leeren ACCU Inhalts.

3.4.4. Anwendung der SELECT Taste

Die SELECT Taste hat folgende Funktionen:

a. Wahl des Speichers, der die V/DIV, s/DIV und DIV (Verzögerung) Einstellungen welche angezeigt werden sollen, enthält.
b. Wahl des Speichers dessen Inhalt aufgezeichnet (PLOT) werden soll.
c. Wenn **keine** DISPLAY Taste eingedrückt ist, wird mit SELECT der Durchlauf (scrolling) der dargestellten Speicher, der Warnlampen und der V/DIV, s/DIV und DIV (Verzögerung) Einstellungen ausgelöst.

Bemerkung: – *Wenn nur* **eine** *DISPLAY Taste eingedrückt ist, hat das Eindrücken der SELECT Taste keine sichtbare Wirkung.*
– *Wenn zwei oder mehr DISPLAY Tasten eingedrückt sind, dann bewirkt Eindrücken der SELECT Taste, dass das System die Warnlampen und die Information in der V/DIV, s/DIV und DIV (Verzögerung) Anzeige durchläuft.*

Mit Hilfe der Drucktaste LOCK können alle Speicherinhalte unverändert erhalten bleiben.

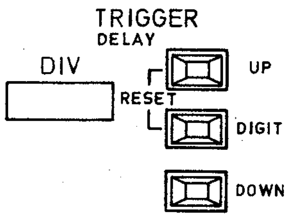
3.4.5. Triggerverzögerung

a. Positive Verzögerung

Die Triggerverzögerung ermöglicht die Wahl der Zeit (in Teilen) zwischen der Triggerung und dem Start der Elektronenstrahlröhren-Darstellung (linke Seite).

BEISPIEL: Angenommen, die sechste Zeile in einem Fernsehbildmuster ist erwünscht (Fernseh-Zeile = 64 µs)
Folglich ist die erforderliche Triggerverzögerung 5 x 64 µs = 320 µs, das heisst nachdem die fünfte Zeile vorbei ist.

Verfahren:



– TVF wählen.
– Schalter TIME/DIV auf 10 µs/DIV einstellen.
– UP eindrücken das Digit niedrigsten Stellenwertes, 2 anzeigt.
– DIGIT einmal eindrücken.
– UP eindrücken bis das zweite Digit 3 anzeigt.

Man erhält nun eine Verzögerung von 32 x 10 µs zwischen Bildimpuls und der Elektronenstrahlröhren-Darstellung auf der linken Seite.
Dies bewirkt die Darstellung der Information der sechsten Zeile.

b. Negative Verzögerung

Während das Oszilloskop dauernd im Schieberegister Information speichert, bietet es die Möglichkeit der Vortriggerung (pre-triggering).
Dies beinhaltet dass ein dem Triggerpunkt vorangehender Signalabschnitt auf dem Bildschirm dargestellt werden kann.
Der Triggerpunkt ist auf jedem beliebigen Teil des Bildschirms (0 bis 9 Teile) wählbar.
Wenn der TIME/DIV Schalter in eine andere Stellung versetzt wird, dann wird die Einstellung der Triggerverzögerung (in Teilen) automatisch geändert (nachberechnet) und dargestellt.
Das Ergebnis dieser Nachberechnung abwärts abgerundet auf ganze Teile (Integer).
Ausgangspunkt der Nachberechnung ist die im Moment dargestellte Anzahl Teile (Div.).

Bemerkung 1: Die Voreinstellung von TRIGGER DELAY bei einer bestimmten TIME/DIV Schalterstellung wird intern gespeichert und bleibt immer die gleiche Verzögerung, unabhängig von Abrundungsfehlern entstanden bei der Nachberechnung zufolge der Betätigung des TIME/DIV Schalters.

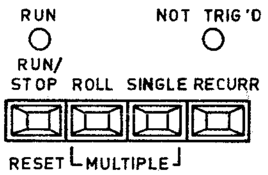
		erstes Beispiel				zweites Beispiel			
	TIME/DIV		DIV		DIV		DIV		DIV
Einstellung	5 µs	1	0095	12	0095	1	0095	10	0095
	10 µs	2	0047	11	0000	2	0047	9	0040
	20 µs	3	0023	10	0000	3	0023	8	0020
	50 µs	4	0009	9	0000	4	0009	7	0008
	. 1 ms	5	0004	8	0000	5	0004	6	0004
	. 2 ms	6	0002	7	0000		0002		0002
	. 5 ms		0000		0000				
			Bereich abwärts		Bereich aufwärts		Bereich abwärts		Bereich aufwärts

Bemerkung 2: Wenn durch Betätigung des TIME/DIV Schalters ein TRIGGER DELAY von "0" erreicht wird, dann werden alle langsameren Positionen ein TRIGGER DELAY von "0" aufweisen.

Bei Betriebsart ROLL wird die Triggerverzögerung ausgeschaltet und die Anzeige (DIV) wird OFF. angeben.

3.4.6. SINGLE (einmalig) und MULTIPLE (mehrfach) Betrieb

Wenn Taste SINGLE eingedrückt ist, wird ACCU nach einem Triggerimpuls und Verzögerung einmal aufgefrischt, ebenso die Elektronenstrahlröhrendarstellung, von ACCU.
Wenn das Gerät auf einen Triggerimpuls wartet, wird die Lampe NOT TRIG'D leuchten.



Wenn die beiden Taste SINGLE UND ROLL eingedrückt sind, wird der SINGLE Vorgang viermal wiederholt. Man nennt dies MULTIPLE Betrieb. Das Ergebnis des ersten Vorgangs wird in STO 3 gespeichert, das zweite Ergebnis in STO 2, das dritte in STO 1 und das vierte in ACCU.
Wenn entweder der SINGLE oder der MULTIPLE Vorgang beendet ist, lässt sich durch Eindrücken der Taste RESET die gleiche Betriebsart von neuem wählen.

3.4.7. ROLL Betrieb

Die Betriebsart ROLL wird für Signale sehr niedriger Frequenz angewandt.
Sie ist wirksam bei TIME/DIV Einstellungen von 0,5 s ... 60 min. Das Signal wird Punkt für Punkt aufgebaut und "schreibt" auf den Bildschirm von rechts nach links. Sobald im ACCU Speicher zehn Bildschirmteile aufgebaut sind, wird automatisch der SAVE Vorgang ausgelöst und wird der Inhalt im Speicher STO 3 aufbewahrt.
Wahl mit Taste ROLL und einmaliges Drücken von RUN/STOP startet den ROLL Betrieb.

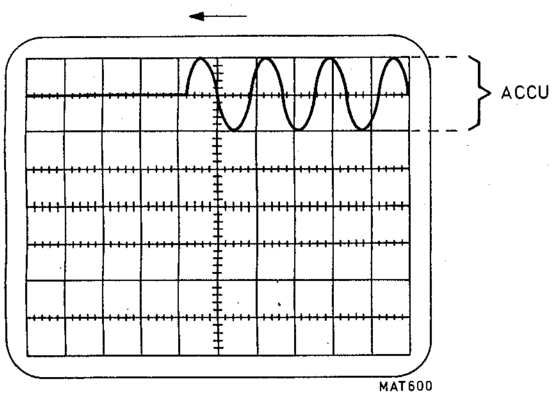


Bild 3.18. Aufbau der ersten Information im ACCU

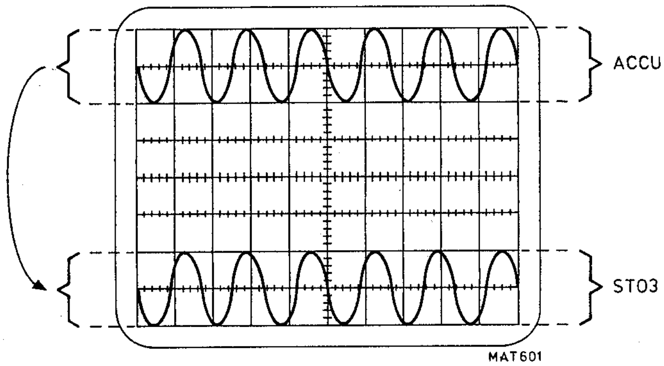


Bild 3.19. Erster SAVE Vorgang

Neue Information wird nun Punkt für Punkt im ACCU Speicher aufgebaut und nach Vollendung (zehn Teile) wird die neue Information in STO 2 gespeichert.

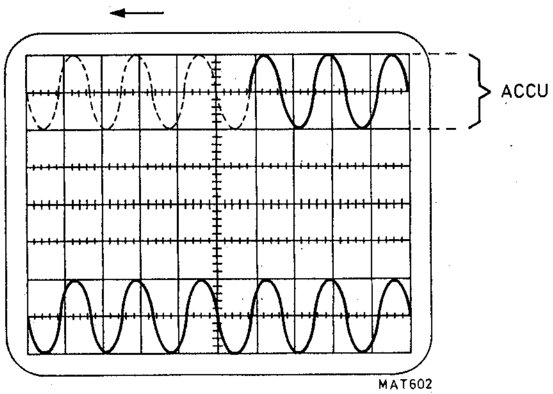


Bild 3.20. Aufbau der zweiten Leuchtspur Information im ACCU

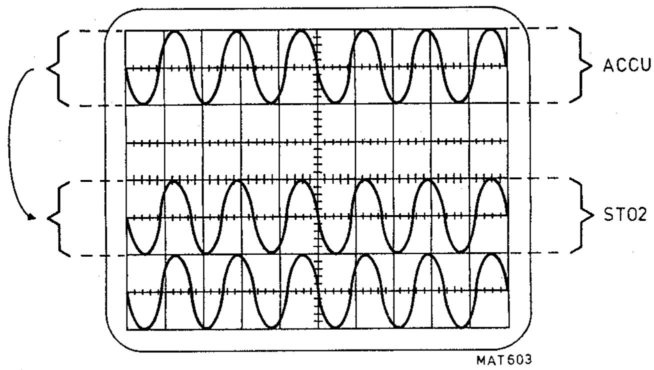


Bild 3.21. Zweiter SAVE Vorgang

Die dritte Information aufgebaut im ACCU wird in STO 1 gespeichert, wie nachstehend veranschaulicht.

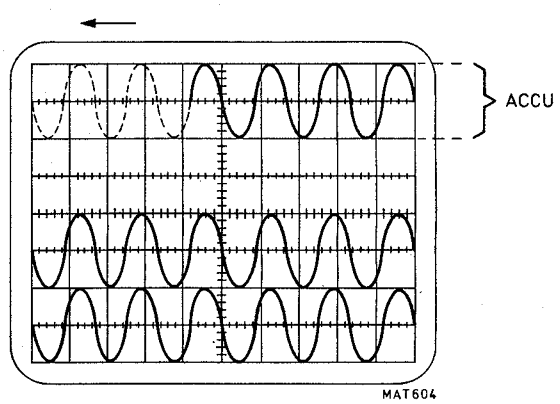


Bild 3.22. Aufbau der dritten Leuchtspur Information im ACCU

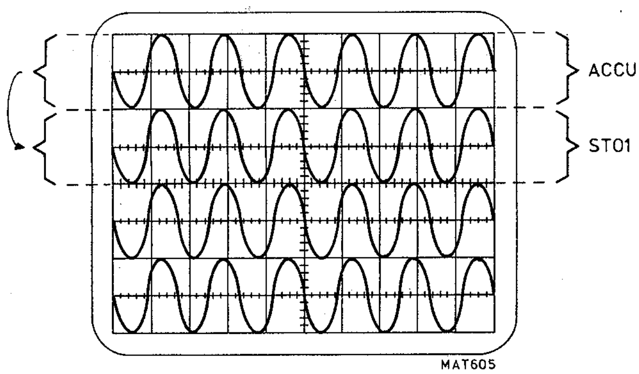


Bild 3.23. Dritter SAVE Vorgang

Die letzte Information wird im ACCU selbst gespeichert, wie unten ersichtlich.

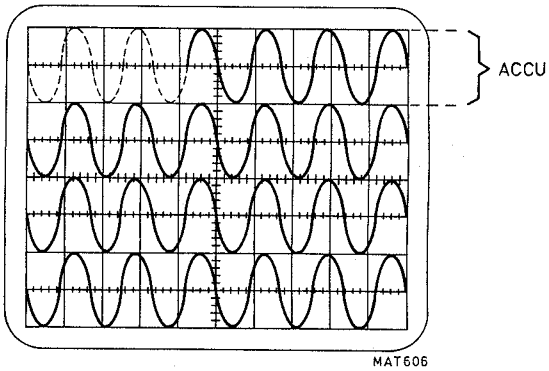


Bild 3.24

Während des ROLL Vorgangs wird Anzeigelampe RUN dauernd leuchten und am Ende des Vorgangs blinken. Falls während des ROLL Vorgangs eine Unterbrechung erforderlich ist, muss Taste RUN/STOP gedrückt werden. ROLL wird unterbrochen und Lampe RUN erlischt. Dieser Vorgang lässt sich auch mit Hilfe eines externen Gleichspannungssignals bei TTL-Pegel ausführen, doch nur wenn der ROLL Betrieb durch Betätigung der RUN/STOP Taste gestoppt wird.

TTL = 1 → RUN   TTL = 0 → STOP

Durch nochmaliges Eindrücken der RUN/STOP Taste wird der ROLL Vorgang fortgesetzt. Nach seiner Beendung (Lampe RUN blinkt) kann der Vorgang von neuem gestartet werden, indem man erst Taste CLEAR und danach RUN/STOP eindrückt.

3.4.8. Plotterbetrieb (Aufzeichnung)

Den X, Y und PEN LIFT Ausgang des Oszilloskops mit dem Schreiber verbinden.
Der X-Ausgang stellt 0,1 V pro Bildschirmteil zur Verfügung (1 V Vollausschlag).
Der Y-Ausgang stellt 0,5 V pro Bildschirmteil zur Verfügung (1 V Vollausschlag).
Der PEN LIFT-Ausgang ist ein offener Kollektorausgang mit einer max. Belastung von 500 mA, kontinuierlich und schaltet den Ausgang auf Null. Er ist TTL kompatibel.
Taste SELECT eindrücken zur Wahl des Speichers welcher die Information enthält die registriert werden soll.
Eindrücken der Taste PLOT startet den Registriervorgang, der auch auf dem Bildschirm durch einen von links nach rechts über die gewählte Schreibspur bewegenden Punkte sichtbar wird.
Der Registriervorgang (plotting) lässt sich durch nochmaliges Eindrücken der PLOT-Taste unterbrechen.
Falls keine automatische Federabhebung (pen-lift) vorhanden ist, kann manuelles Abheben und Aufsetzen der Schreibfeder auf folgende Weise vorgenommen werden:

- PLOT eindrücken.
- 2 Sekunden warten.
- Schreibfeder nach unten drücken (nach einer Sekunde beginnt die Registrierung).
- Nachdem das Signal registriert ist die Schreibfeder abheben.
- Im Zweikanalbetrieb bewegt die Schreibfeder nach sechs Sekunden zum Startpunkt des zweiten Kanals.
- Schreibfeder nach unten drücken (aufsetzen).
- Nach der Registrierung des zweiten Kanals die Schreibfeder abheben.

Bemerkung 1: Während des Registrierbetriebs (plotting) befindet sich das Oszilloskop in Betriebsart "LOCK" (gesperrt), das bedeutet dass der Inhalt der Speicher **nicht** *verändert werden kann.*

Bemerkung 2: Im Falle von Kanal A und B "plotting" wird erst Kanal A und danach Kanal B registriert.

Bemerkung 3: Im "PLOT" Betrieb ist zu Beginn und Ende 3 Sekunden Verzögerung vorgesehen um für Schreibfederbedienung von Hand genügend Zeit zu geben.

3.4.9. Einstellen der Abschwächer-Tastköpfe

- Die Kompensationsdose mit Buchse A verbinden und die Tastkopfspitze an Buchse CAL legen.
- Y x 5 eindrücken.
- Eine geeignete Einstellung des AMPL/DIV Schalter von Kanal A wählen.
- Mit einem kleinen Schraubenzieher durch das Loch in der Kompensationsdose den Trimmer einstellen um ein einwandfreies Bild zu erhalten.
  (siehe Bild 3.25)

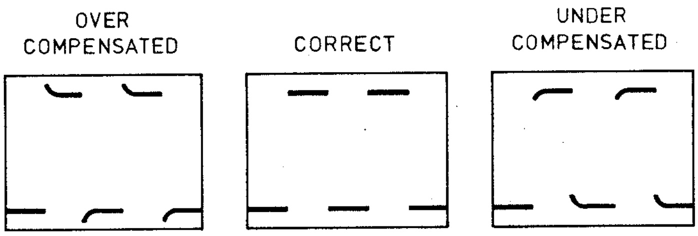


Bild 3.25 · MAT 635

3.4.10 Differenz Betriebsart

Betriebsart A minus B lässt sich durch Drücken von ADD und Ziehen des Knopfes B OFFSET einstellen.
Bei Messungen bei denen Signalleitungen bedeutende Gleichtaktsignale führen (z.B. Brumm) hebt die Differenz-Betriebsart diese Signale auf und lässt den Rest, der von Bedeutung ist, übrig (A-B).
Die Fähigkeit des Oszilloskops für die Unterdrückung von Gleichtaktsignalen, ist im CMR-Faktor gegeben (siehe Abb. 3.26)
Um den spezifizierten Grad der Gleichtaktunderdrückung zu erlangen, müssen erst die Kanal A und B Verstärkungen ausgeglichen werden. Dies wird durch Anschluss beider Kanäle an der CAL-Ausgang und durch Einstellung eines der stufenlosen Einstellelemente in dem Schalter AMPL/DIV auf Minimum Ablenkung auf dem Bildschirm erreicht.
Bei Verwendung von passiven 10:1 Messköpfen ist ein ähnliches Ausgleichsverfahren zu empfehlen. Es erfolgt durch die Kompensationseinstellung auf Minimum-Ablenkung.

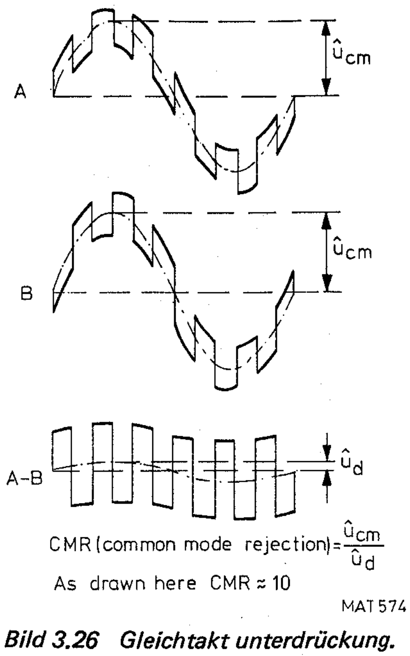


Bild 3.26 Gleichtakt unterdrückung.

3.4.11. X = A und Y = B

In dieser Betriebsart wird das Signal Punkt für Punkt aufgebaut.
Das heisst, dass die Punktverbindeschaltung automatisch ausgeschaltet wird.

Verfahren:

- Signale an die Kanal A und die Kanal B Eingangsbuchsen legen.
- Die AMPL/DIV Schalter entsprechend einstellen.
- X = t eindrücken und den TIME/DIV Schalter so stellen dass zumindest eine Periode auf dem Bildschirm dargestellt wird.
- Drücke X = A
  Y = B

  Horizontalablenkung wird nun vom Kanal A-Eingang bestimmt und Vertikalablenkung vom Kanal B-Eingang

TABLE DES MATIERES

1. GENERALITES

1.1. INTRODUCTION

L'oscilloscope à mémoire digitale PM 3310 est un appareil de mesure portatif à deux voies pour 60 MHz, pourvu de circuits électroniques commandées par microprocesseur.

Par sa conception ergonomique et compacte, le présent appareil offre une gamme étendue de réglages.
La disposition universelle des circuits combinée avec le logiciel du microprocesseur présente d'innombrables possibilités, y compris:

- trace à forte intensité
- la vue de pré-déclenchement
- le stockage de deux voies avec quatre signaux d'événements différents par voie
- IEC bus en option, par l'intermédiaire de PM 3325
- sortie pour table traçante
- retard de déclenchement
- alimentation d'assistance mémoire (batteries non comprises)

De plus, un écran de 8 cm x 10 cm avec lignes de graticules illuminées permet une visualisation facilitée: le potentiel d'accélération de 10 kV donne une trace à forte intensité et un point lumineux bien défini.

L'oscilloscope est pourvu de nombreux circuits intégrés, assurant le fonctionnement stable et réduisant le nombre des points de réglage.
La tension d'alimentation est réglable sur deux gammes: 100 à 120 V ± 10 % ou 220 à 240 V ± 10 %.

Toutes ces propriétés font du présent oscilloscope un instrument particulièrement utile dans une gamme étendue d'applications telles que la mesure et l'observation de:

- temps de montée (trace à forte intensité)
- signaux rapides à très faible taux de répétition
- signaux à très basse fréquence (jusqu'à une heure par division).

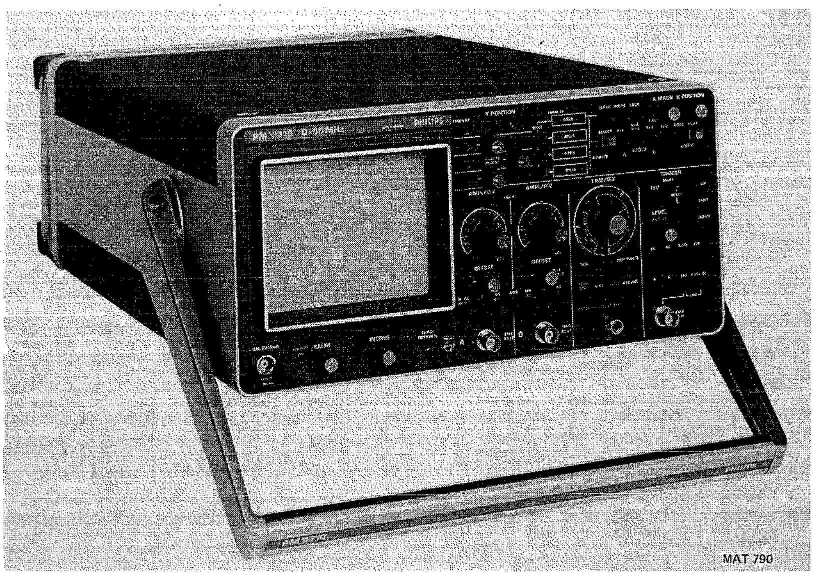


Fig. 1.1. Oscilloscope à mémoire digitale 60 MHz PM 3310

1.2. CARACTERISTIQUES TECHNIQUES

Cet instrument a été conçu conformément à la norme C.E.I. 348 pour les appareils de classe I . A la livraison, il répond aux règles de sécurité. La présente notice comporte des informations et les avertissements nécessaires à l'utilisateur afin d'assurer le fonctionnement de l'instrument dans les conditions de sécurité requises et de le maintenir dans un état conforme à la norme.

- Toutes les spécifications sont valables après un temps d'échauffement de 30 min. (température de référence 23 °C) et sans modifier la position de l'appareil).
- Seules les valeurs accompagnées d'une tolérance ou d'une limite sont garanties; les caractéristiques sans tolérance sont données à titre indicatif.
- Les précisions (absolue ou en %) se rapportent à la valeur de référence indiquée.

1.2.1. Tube à rayons cathodiques

Type	D14 - 292 GH/39	
Tension d'accélération	10 kV	
Aire de mesure	8 x 10 cm	Doublée de métal
Type de phosphore	P 31 (GH)	
Graticule	Interne	Divisions centimétriques avec subdivisions de 2 mm
Illumination de graticule	Bien visible sous des conditions d'éclairage normal et variable de façon continue	
Rotation de trace	Réglage tournevis au panneau avant	
Focalisation	Réglée automatiquement	

1.2.2. Axe vertical d'entrée

Gamme de fréquence	Continu à 60 MHz Alternatif: 10 Hz à 60 MHz	
Temps de montée	< 6 ns	
Aberrations d'impulsion	± 3 %	Mesurées en mode "Y x 5" avec une impulsion d'essai de 8 div temps de montée 1 ns; fréquence 1 MHz (à l'exception des premiers 0.2 cm mesurés à partir de l'impulsion centrale)
Déviation verticale		
Coefficient de déviation	10 mV/div à 50 V/div	12 positions étalonnées en progression 1-2-5
Erreur limite	± 3 %	± 5 % en mode "Y x 5"
Commande continue	1 : > 2.5	
Impédance d'entrée	1 MΩ // 25pF	
Couplage	Capacitif-0-Continu	
Tension d'entrée maximale	± 400 V	Continu + crête en alternatif
Sélection d'entrée	A seule B seule A et B additionnées	La voie B peut être inversée

Facteur de réjection en mode commun	100 : 1	A 2 MHz, signal maxi en mode commun: 8 divisions
Gamme dynamique	2 x gamme de tension	
Offset en continu	± 4 x gamme de tension	
Taux d'échantillonnage maxi	50 MHz	
Retard de signal visible	> 10 ns	Voir également "retard"

1.2.3. **Base de temps**

Coefficients de temps		
Répétitif seulement	5 ns à 0.2 μs/div	
Direct	0.5 μs à 0.2 s/div	
Exploration verticale (roll)	0.5 s à 60 min/div	
Erreur de coefficient	< 2 %	4 % combinée avec retard dans "REPETITIVE ONLY"
Résolution	25 échantillons/div	

1.2.4. **Déclenchement**

Source	A B EXT EXT : 10 Secteur	
Sensibilité		
Interne	0,3 div 0,15 div	à 60 MHz à 40 MHz
Externe	0,3 V 0,15 V	à 60 MHz à 40 MHz
Externe : 10	3 V 1,5 V	à 60 MHz à 40 MHz
Pente	+/–	
Modes	Auto Continu Alternatif Trame de télévision (image 1/1)	20 Hz à 60 MHz Continu à 60 MHz 10 Hz à 60 MHz Conforme à CCIR (625 lignes)
Niveau		
Auto	Proportionnel à la valeur crête-à-crête du signal de déclenchement	
Alternatif/continu	± 3 div	
Retard		
Gamme	–9 à +9999 div 0 à 100 div	0.2 s à 0.5 μs/div 0.2 μs à 5 ns/div
Précision	± 2 mm ou 0.01 % ± 2 div + retard visible	0.2 s à 0.5 μs 0.2 μs à 5 ns/div
Impédance d'entrée	1Ω // 25pF	
Tension d'entrée maxi	± 400 V	Continu + crête en alternatif

1.2.5.	**Mémoire**		
	Nombre de mémoires	4	1 mémoire accumulateur et 3 mémoires d'emmagasinage
	Résolution horizontale	1 : 250	En mode de traçage simple
	Résolution verticale	1 : 250	
1.2.6.	**Modes de fonctionnement**		
	Simple	Rafraîchissement de mémoire accumulateur lorsque le niveau de déclenchement est atteint et que le temps réglé avec retard de déclenchement est écoulé. Le signal est stocké en fonction de la position du retard de déclenchement. Pendant l'attente, l'accumulateur est affiché et la diode LED "NOT TRIG'D" est allumée.	
	Rafraîchissement de mémoire ("recurrent")	Le signal dans la mémoire accumulateur est affiché sur l'écran. A écoulement de ce temps-réglé avec retard de déclenchement- la mémoire emmagasine de nouvelles informations.	5 ns à 0.2 s/div
	Exploration horizontale (roll)	Le signal est formé point par point à droite de l'écran et déplacé vers la gauche. Lorsque l'accumulateur est plein, l'information est placée dans le registre 3, puis dans le registre 2, le registre 1 et finalement dans l'accumulateur. Ensuite, l'exploration est arrêtée, ce qu'indique le témoin "RUN" clignotant.	0.5 s à 60 min/div
	Multiple	4 fois "simple" avec maintien en mémoires	0,5 μs à 0.2 s/div
1.2.7.	**Modes d'affichage**		
	Mémoire	Couvre 2 centimètres de hauteur d'écran	
	Combinaisons d'affichage des voies		
	Accumulateur	En fonction de la sélection d'entrée	
	Registre	Information telle que stockée dans l'accumulateur peut être sélectionnée pour le stockage dans chacune des trois mémoires registres et est affichée lorsque le bouton d'affichage est enfoncé	Total, information stockée en STORE 1, 2 ou 3 peut être inversée
	Gamme de positionnement	± 8 div	

Vertical Loupe d'axe vertical	5 fois	La mémoire couvre 10 cm de hauteur d'écran. Indiqué par la diode LED dans la section affichage.
Loupe d'axe horizontal	1 : > 2,5	Continu
Sélection X-Y	Déviation en sens X peut être dérivée de la base de temps ou du contenu mémoire dérivé de l'entrée A.	
Modes de mémoire	"CLEAR" (effacer)	La mémoire accumulateur est effacée.
	"SAVE" (3x) (stocker)	Le contenu de mémoire accumulateur est stocké dans le registre sélection
	"WRITE" (écrire)	Le signal d'entrée peut être écrit dans la mémoire accumulateur
	"LOCK" (bloquer)	Le système de mémoire est fermé
"DOTS"	Bouton poussoir	On passe du mode d'affichage normal (points reliés) en affichage en pointillé

1.2.8. Sortie pour l'enregistreur X/Y ou X(t)

Horizontale	1 V/pleine déviation d'échelle	
Verticale	1 V/pleine déviation d'échelle	
Levage de style	Compatible TTL "0" = style rabaissé "1" = style levé	Sortie collecteur ouverte Charge maxi: 0,5V : 500 mA.
Temps de traçage	environ 100 s	
Séquence de traçage	Le traçage B a lieu après le traçage A	

1.2.9. Interfaces

IEC-bus	En option à l'aide d'un circuit imprimé enfichable	
IEC-bus	Réglages et sortie à commander à partir du contrôleur ligne bus	
Local/A distance	Avec connecteur IEC	

1.2.10. Affichage X-Y

X = t	A partir de la base de temps	
X = A Y = B	A partir de l'entrée YA	"Points reliés" n'est pas fonctionnel
Largeur de bande	voir YA	
Précision	5 %	
Différence de phase	Distance entre signal dérivé de A et signe dérivé de B: 1/25 div.	
Position	0 du signal A stocké sera au centre de l'écran.	

1.2.11. Sortie d'étalonnage

Fréquence	2,5 kHz	
Tension	3 V	
Courant	6 mA	

1.2.12. Alimentation

Tension secteur	100 à 120 V ± 10 % 220 à 240 V ± 10 %	
Fréquence secteur	50 à 400 Hz ± 10 %	
Consommation	< 65 W	
Batterie		
Fonction	Seulement pour assistance mémoire	
Type	2 batteries "pen light" de 1.5 V	par exemple 2x 1.5 V lithium SAFT 2x 1.5 V Duracell
Isolation	L'isolation de l'alimentation répond aux conditions de sécurité de CEI 348 classe I pour appareils à enveloppe métallique	

1.2.13. Conditions d'ambiance

Remarque: Les données d'environnement ne sont valables que si l'instrument est contrôlé conformément aux méthodes officielles. Des renseignements relatifs à ces méthodes et aux critères employés sont fournis sur demande par l'organisation PHILIPS de votre pays ou par le TEST AND MEASURING DEPARTMENT de la N.V. PHILIPS' GLOEILAMPENFABRIEKEN a EINDHOVEN, PAYS-BAS.

Température ambiante	+5 à +40 °C −10 à +40 °C −55 à + 75°C	Gamme de référence d'utilisation Gamme limite d'utilisation Conditions de stockage conformément à MIL 28800 et un maximum de 24 heures à haute et/ou à basse température
Altitude		
Limite opérationnelle	5000 m	
Limite de transport	15000 m	Conforme à CEI 68-2-13, test M
Humidité	Suivant CEI 68 Db	L'appareil résiste à une humidité relative de 95 % pour un cycle de température de 25 °C à 40 °C (hors service)
Chocs	30 m/s^2	En service; chocs d'1/2 sinus durée 11 ms; 3 chocs par direction pour un total de 18 chocs.

Vibrations	3 m/s²	En service; vibrations dans trois directions avec un maximum de 20 min. par direction; 10 minutes avec fréquence de 5-25 Hz et amplitude de 1,016 mm crête-à-crête; 10 minutes avec fréquence de 25-55 Hz et amplitude 0.5 mm crête-à-crête. 10 minutes supplémentaires sur la résonance de fréquence et avec hausse maximale d'amplitude. L'unité est montée sur une table de vibration sans matériel amortisseur.
Dimensions	longueur 460 mm	Poignée et commandes non comprises. Voir également figure 1.2.
	largeur 316 mm	Poignée non comprise
	hauteur 154 mm	Pieds non compris
Poids	environ 12 kg	

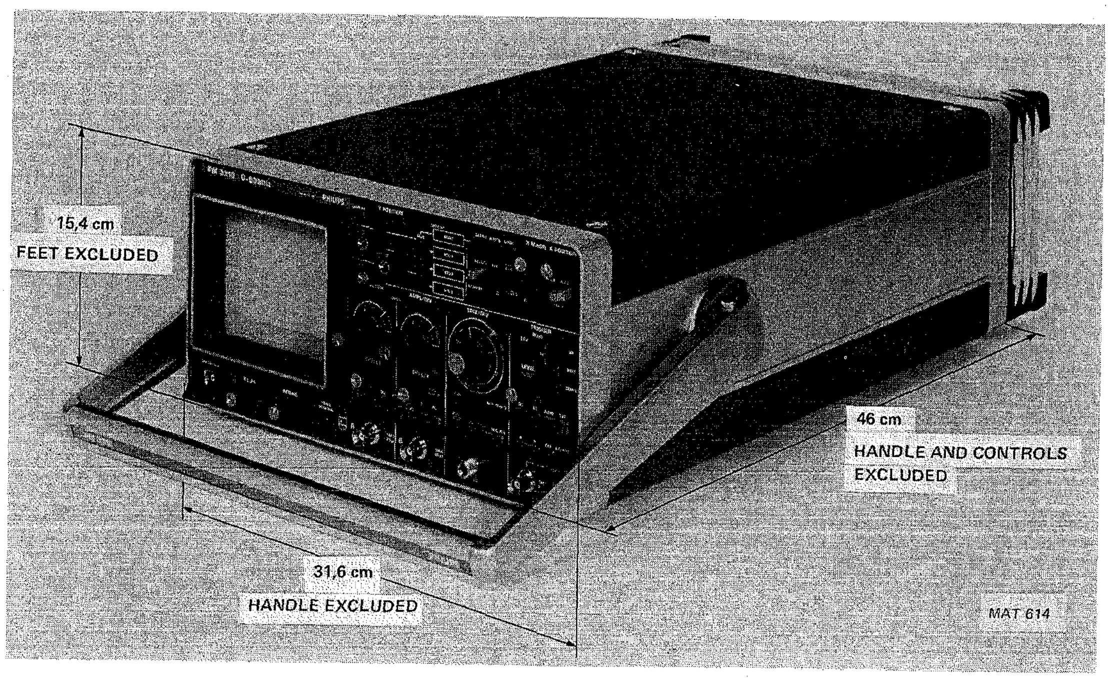


Fig. 1.2. Dimensions

1.3. ACCESSOIRES

1.3.1. Accessoires compris à la livraison

- 2x sonde 10 : 1; 1,5 m avec indication de gamme
- 1x borne d'étalonnage – adaptateur BNC
- 1x filtre de contraste bleu
- 1x visière repliable PM 9366
- 1x couvercle frontal avec emplacement pour 3 sondes
- 1x notice d'emploi
- 2x adaptateur BNC banane 4 mm PM 9051

1.3.2. Accessoires en option

- Batteries pour alimentation d'assistance mémoire
- PM 3325, circuit imprimé avec connecteur et matériel de montage pour fonctionnement IEC-bus (IEC 625)
- PM 8960, jeu pour montage en rack 19"

1.4. INFORMATION SUR LES ACCESSOIRES

1.4.1. Sonde 10 : 1 (1,5 m) avec indication de gamme

La sonde fournie avec l'oscilloscope PM 3310 est comparable à la sonde PM 8927S. Il s'agit d'une sonde 10x pour oscilloscopes allant jusqu'à 80 MHz à douille d'entrée BNC et capacité d'entrée de 14 à 40 pF mis en parallèle par 1 MΩ. A la livraison la réponse d'échelon HF est réglée sur la capacité d'entrée de PM 3310.
La sonde est pourvue d'une douille BNC spéciale permettant d'obtenir l'indication de la gamme. Ceci veut dire que l'échelle d'atténuateur de l'oscilloscope est adaptée automatiquement à l'atténuation de sonde.

Caractéristiques techniques

Caractéristique électriques

Atténuation	10 x ± 2 % (entrée d'oscilloscope 1 MΩ)
Résistance d'entrée en continu	10 MΩ ± 2 % (entrée d'oscilloscope 1 MΩ)
en alternatif	Voir courbe Fig. 1.3.
Capacitance d'entrée en continu et basse fréquence	11 pF ± 1 pF (entrée d'oscilloscope 1 MΩ ± 5 % mis en parallèle par 13 pF ± 3 pF)
Réactance d'entrée HF	Voir courbe Fig. 1.3.
Largeur de bande utile	Voir courbe Fig. 1.4.a.
Tension maximale d'entrée	500 V continu + alternatif (crête), décroissant avec la fréquence. Voir Fig. 1.4. Entrée d'oscilloscope 1 MΩ et tension appliquée entre pointe de sonde et la partie du corps de sonde mise à la terre. Tension d'essai 1500 V continu pendant 1 s à une température entre 15 et 25 °C, humidité relative de 80 % maximum et au niveau de la mer.
Contrôle du zéro sur boîtier de sonde	Fonction identique à la position 0 du commutateur de couplage d'entrée sur l'oscilloscope.
Gamme de compensation	14 à 40 pF

Conditions d'ambiance

La sonde fonctionne conformément aux spécifications dans les conditions suivantes:

Température	–25 à +70 °C
Altitude	Jusqu'à 5000 mètres
Autres conditions d'ambiance	Identiques à celles d'application pour l'oscilloscope utilisé avec la sonde.

Caractéristiques mécaniques

Dimensions	Corps de sonde 103 mm x 11 m dia (max.) Longueur de câble 1500 ou 2500 mm Boîte de correction 55 x 30 x 15 mm y compris BNC
Masse	140 g, y compris les accessoires standard.

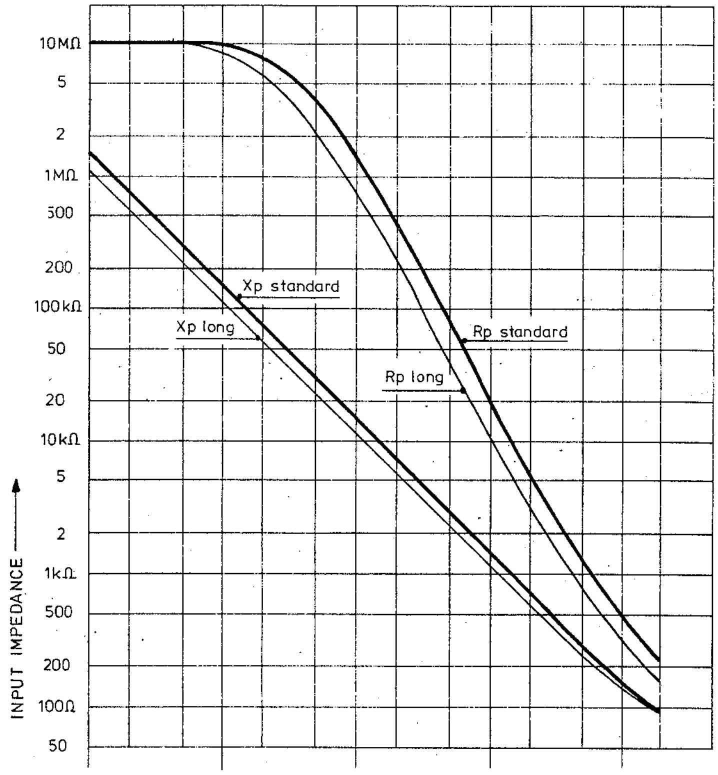


Fig. 1.3.

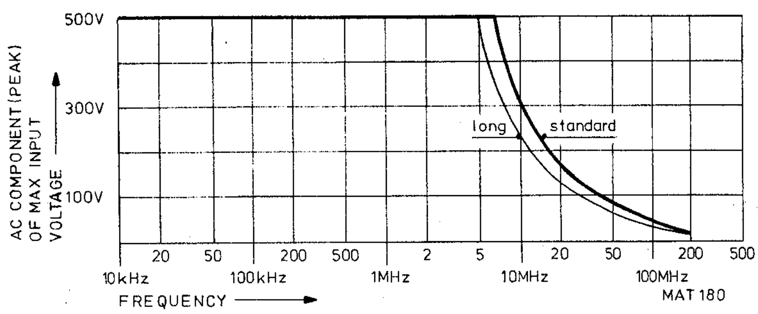


Fig. 1.4.

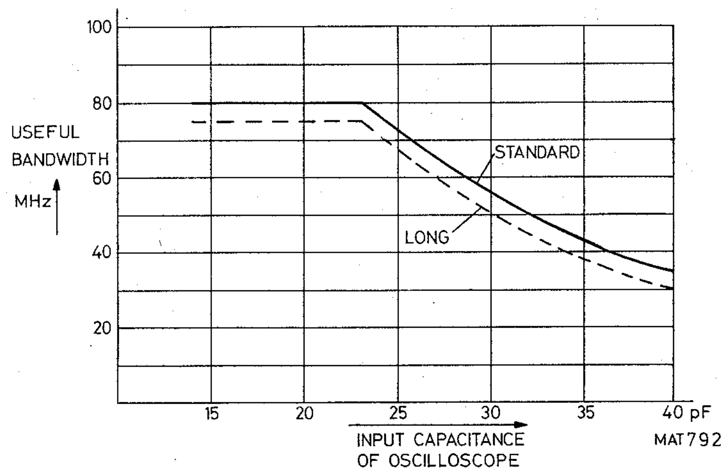


Fig. 1.4.a.

Réglages

Adaptation de la sonde à l'oscilloscope

La sonde de mesure est réglée et contrôlée par le fabricant. Cependant, pour adapter la sonde à l'oscilloscope, le procédé suivant est requis.
Connecter la pointe de mesure à la prise CAL d'oscilloscope.
Un trimmer (C2, Fig. 1.11) est réglable à travers une ouverture dans la boîte de compensation pour obtenir une réponse rectangulaire optimale. Voir Fig. 1.5, 1.6 et 1.7.

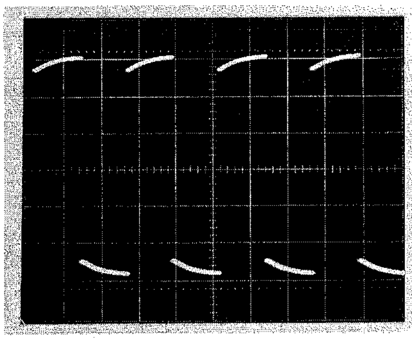


Fig. 1.5. Surcompensation (réglage C2)

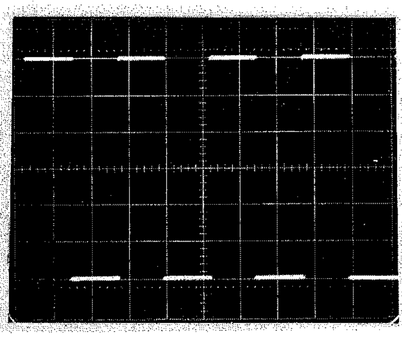


Fig. 1.6. Compensation exacte (réglage C2)

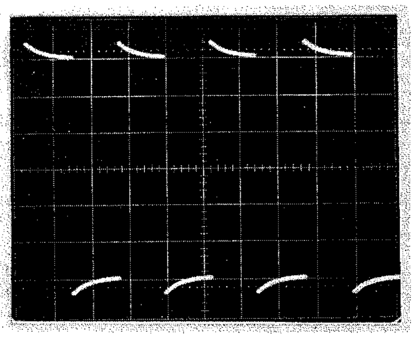


Fig. 1.7. Sous-compensation (réglage C2)

Réglage de la réponse haute fréquence

Le réseau de correction pour réponse haute fréquence est réglé par le fabricant afin d'être adapté à l'entrée d'oscilloscope. Pour obtenir une réponse optimale, avec des sondes livrées séparément, la sonde peut être ajustée à l'oscilloscope en question.
Un rajustage ultérieur ne sera nécessaire que si la sonde doit être appliquée à un oscilloscope de type différent ou après le remplacement d'un composant électrique.
Pour le réglage, procéder comme suit:
Connecter la sonde à un générateur rapide (temps de montée n'excédant pas 1 ns) terminé par son impédance caractéristiques.
Démonter la boîte de compensation. Régler le générateur sur 100 Hz. Ajuster alternativement R2 et R3 afin d'obtenir l'affichage comme illustré en figure 1.8.
Il est important que le front d'onde soit aussi escarpé que possible et le sommet aussi plat que possible. Des réglages incorrects de R2 et R3 causent des distorsions d'impulsion telles qu'illustrées aux figures 1.9 et 1.10.

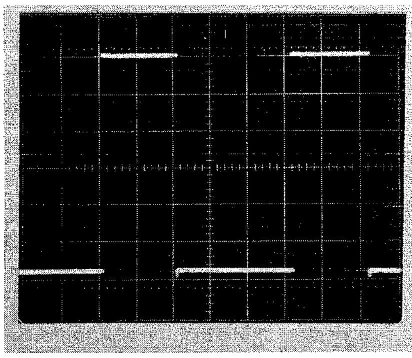


Fig. 1.8. Potentiomètres de pré règlage ajustés correctement

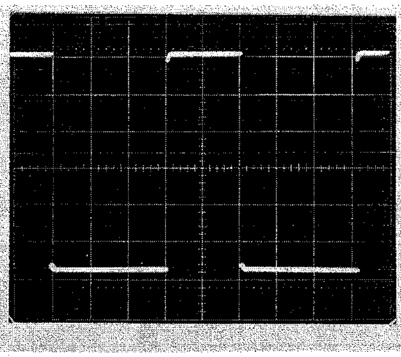


Fig. 1.9. Arondissement dû au réglage incorrect des potentiomètres

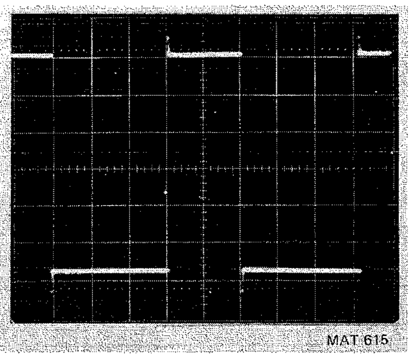


Fig. 1.10. Dépassement dû au réglage incorrect des potentiomètres

Démontage

Démontage de la sonde (voir Fig. 1.11)

La partie avant 11 de la sonde peut être dévissée de la partie arrière 13. Le poste 11 peut dès lors être glissé de 12 et 13.
La combinaison RC 12 est soudée à 13. Pour le remplacement de 12, se référer à la section "Remplacement des composants".

Démontage de la boîte de compensation (Fig. 1.12)

Dévisser le collier strié de la boîte de compensation au câble.
Le boîtier 14 peut être glissé latéralement de la boîte de compensation. Les composants électriques sur le circuit imprimé sont alors accessibles.

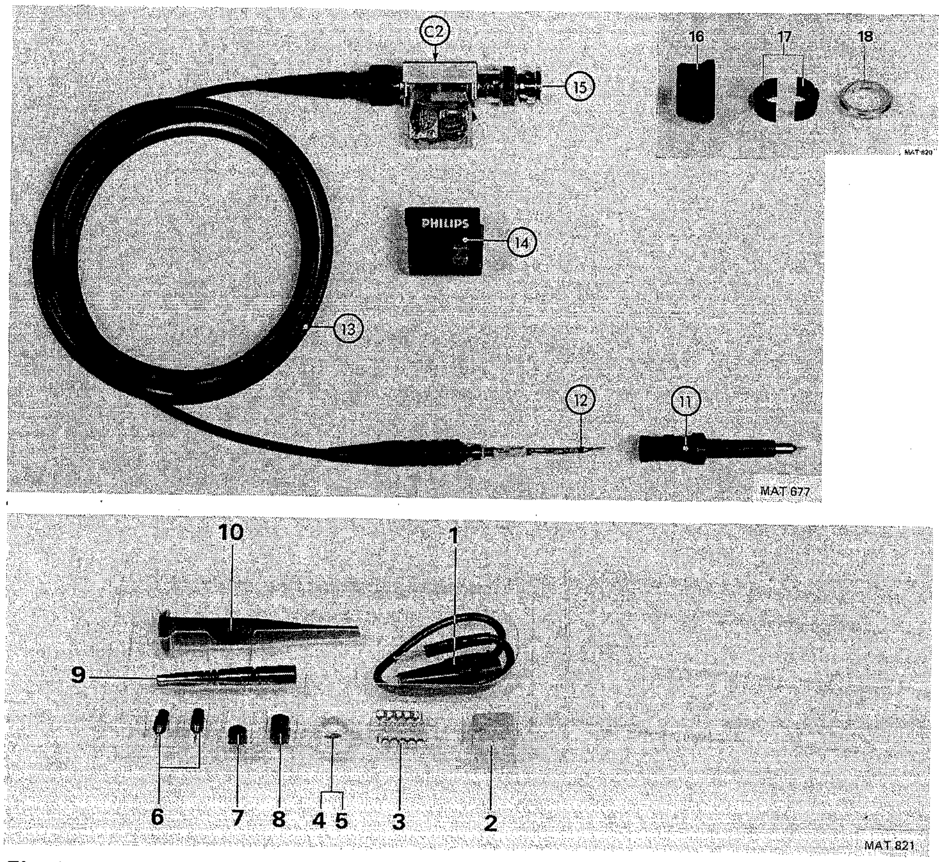


Fig. 1.11. Démontage + accessoires

Remplacement des composants

Assemblage de la sonde

Un nouveau réseau RC est coulissé sur le raccord de câble après quoi le conducteur de câble est soudé au fil de la résistance.
Lorsque la sonde est assemblée, le réseau RC doit se trouver au centre dans la pointe de sonde.

Remplacement du câble

Démonter la boîte de compensation.
Dessouder la connexion entre le conducteur interne et le circuit imprimé. Bien tenir le châssis de la boîte de compensation et desserrer le raccord de câble à l'aide d'une clé hexagonale de 5 mm. Pour l'assemblage, procéder en ordre inverse du démontage.

Remplacement de la pointe de sonde

La pointe endommagé peut être tirée hors de la sonde à l'aide d'un pince. Une nouvelle pointe doit être poussée fermement en place.

Nomenclature des composants

Composants mécaniques (Fig. 1.11. et 1.12.)

Les postes 1 à 10 sont des accessoires standard livrés avec la sonde.

Pos.	Numéro de commande	Qté	Description
1	5322 321 20223	1	Câble de terre
2	5322 256 94136	1	Porte-fusible
3	5322 255 44026	10	Bornes à souder pouvant être incorporés dans les circuits comme points de test de routine
4	5322 532 64223	2	Bague rouge
5	5322 532 74224	2	Bague blanche
	5322 532 64225	2	Bague bleue (pas illustrée)
6	5322 268 14017	2	Pointe de sonde
7	5322 462 44319	1	Capuchon isolant couvrant la partie métallique de la sonde pendant les mesures sur des circuits à câblage dense
8	5322 462 44318	2	Capuchon facilitant la mesure sur des circuits intégrés "dual-in-line"
9	5322 264 24018	1	Adaptateur enroulé
10	5322 264 24019	1	Grippe-fil à ressort
11	5322 264 24012	1	Coquille de sonde avec bouton de test zéro
12	5322 216 54152		Réseau RC
13	5322 320 14063		Ensemble de câbles
14	5322 447 64016	1	Capuchon
15	5322 268 44019	1	Connecteur BNC
16	5322 532 64277	1	Porte
17	5322 532 64278	2	Baqué
18	5322 532 14696	1	Baque de contacte
—	5322 492 64765	1	Grippe-fil de contacte
R	5322 116 55552	1	Résistance 2K32

Composants électriques

Pos.	Numéro de commande	Description
C1	–	Partie du réseau RC (pas fournie séparément)
C2	5322 125 54003	Trimmer 60 pF, 300 V
R1	–	Partie de réseau RC (pas fournie séparément)
R2	5322 101 14047	Potentiomètre 470 Ω, 20 %, 0,5 W
R3	5322 100 10112	Potentiomètre 1 kΩ, 20 %, 0,5 W

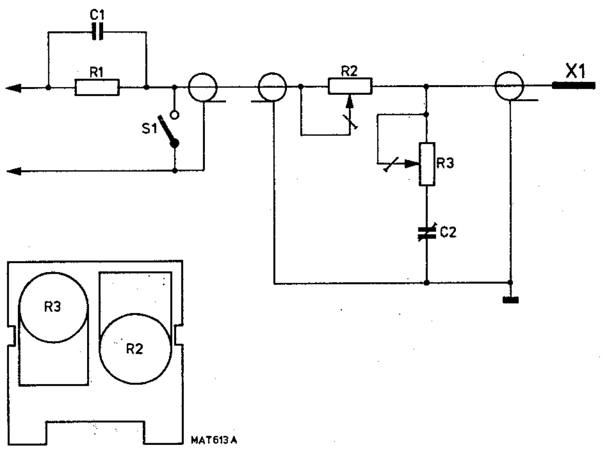


Fig. 1.12. Circuit imprimé illustrant les éléments de réglage et le circuit électrique

1.4.1.1. BORNE CAL-ADAPTATEUR BNC

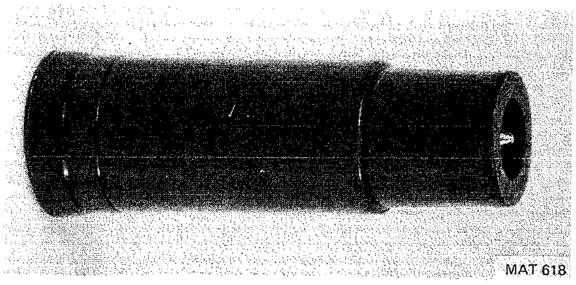


Fig. 1.13.

1.4.1.2. FILTRE DE CONTRASTE BLEU

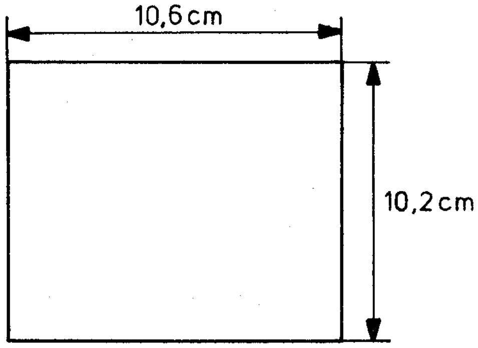


Fig. 1.14.

1.4.1.3. VISIÈRE REPLIABLE PM 9366

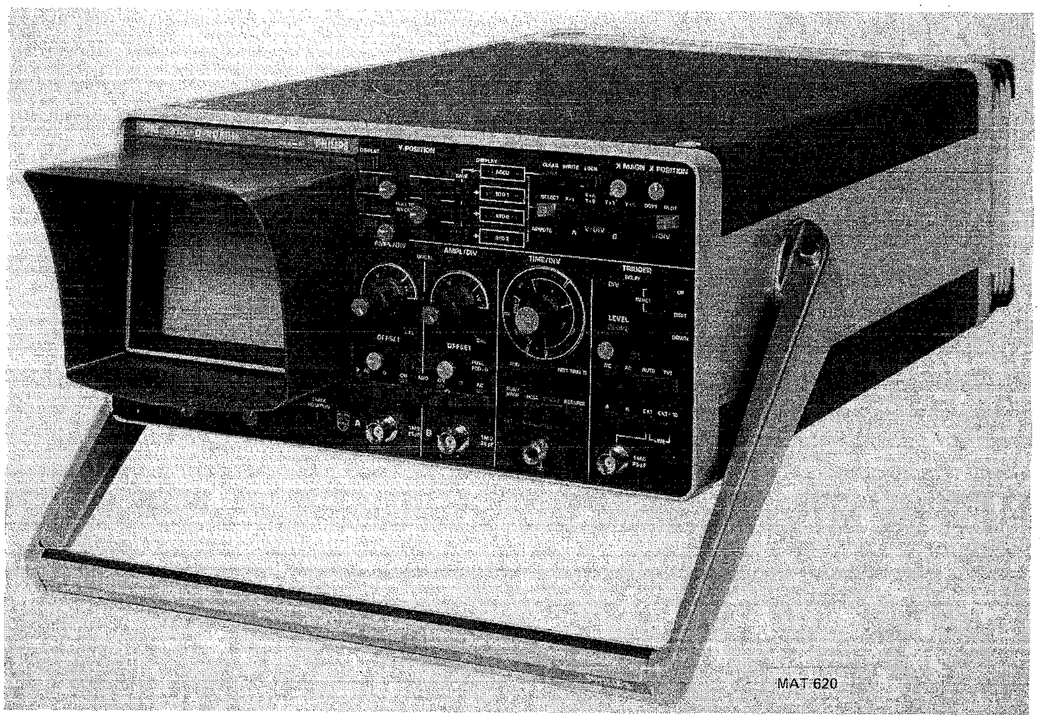


Fig. 1.15.

1.4.1.4. PANNEAU AVANT

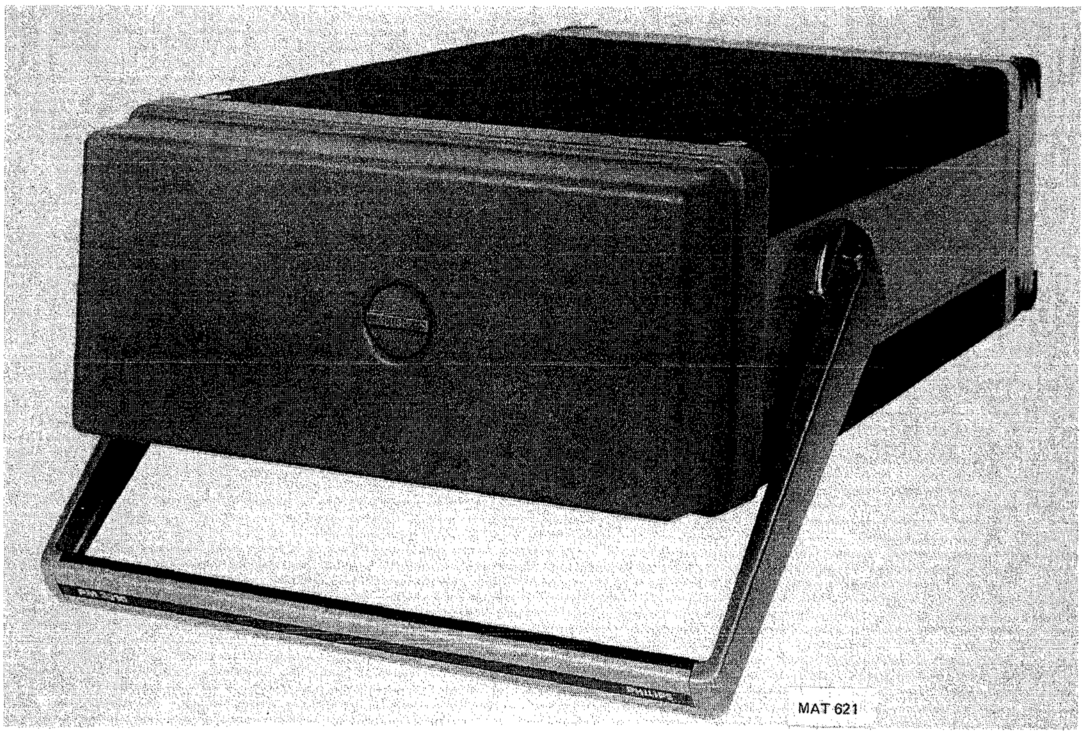


Fig. 1.16.

1.4.1.5. BORNE BNC-ADAPTATEUR 4mm PM9051

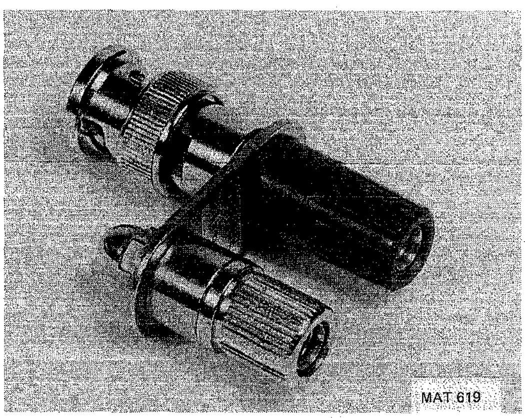


Fig. 1.17.

1.4.2. Information sur les accessoires en option

1.4.2.1. BATTERIES POUR ALIMENTATION D 'ASSISTANCE BATTERIE

L'appareil est équipé d'une unité d'assistance permettant de conserver le contenu de mémoire et les réglages des commutateurs après la mise hors service du commutateur POWER.
Lorsque l'alimentation d'assistance batterie est utilisée l'information stockée dans les mémoires à accès libre (RAM) avant la mise hors service est affichée à nouveau lorsque l'appareil est mis en service au bout d'un certain temps.

L'affichage automatique indique la dernière information contenue en mémoire et les réglages de commutateur correspondants.
Le fonctionnement incorrect ou avec batterie faible n'est pas indiqué par l'oscilloscope. Dans ce cas l'appareil fonctionnera comme s'il n'y avait pas d'alimentation pour assistance de mémoire. Pour des raisons techniques les batteries ne sont pas comprises. Si l'alimentation d'assistance mémoire est requise, installer les batteries comme décrit ci-avant.

Remplacement des batteries

ATTENTION: Toujours s'assurer que l'alimentation secteur est entièrement déconnectée de toute tension avant de déposer un seul couvercle de l'appareil.
L'appareil est protégé par quatre couvercles: un couvercle avant, une tôle arrière, une tôle supérieure et une tôle de fond.

Les batteries sont accessibles après dépose de la tôle supérieure.
Pour déposer les couvercles, procéder comme suit:

- Relâcher les attaches aux quatre coins de la tôle supérieure. Ne pas relâcher plus de deux tours, afin d'éviter que les attaches ne se perdent.

Fig. 1.18. Depose de couvercle d'appareil

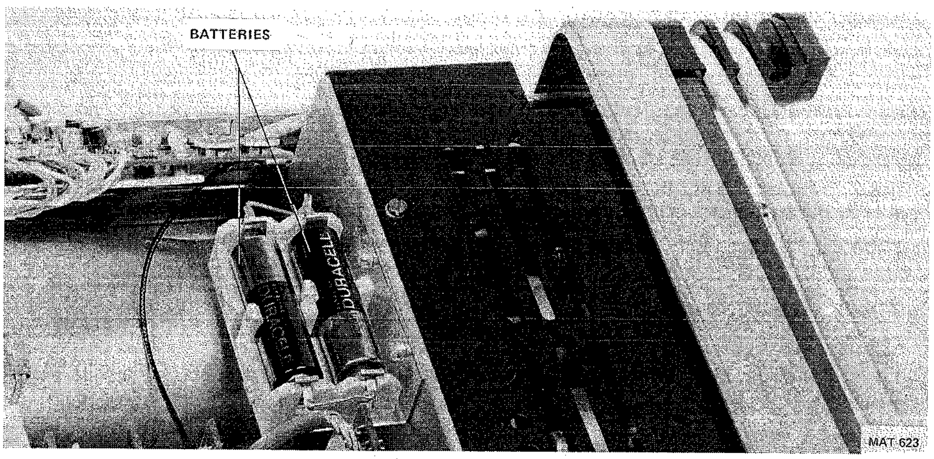


Fig. 1.19. Emplacement des batteries internes

Types de batteries recommandés: 2 x 1,5 V lithium SAFT ou
2 x 1,5 V duracell

1.4.2.2. Instructions d'assemblage pour jeu d'adaptation en rack 19" PM 8960

Introduction

Le PM 8960 est un jeu d'adaptation permettant d'adapter l'oscilloscope PM 3310 au montage en rack ou en coffret 19".
L'appareil peut alors être facilement glissé hors du rack ou du coffret, permettant son inspection aisée.

Contenu d'un jeu PM 8960

Repère sur figure 2	Description	Quantité
1	Poignée	2
2	Panneau avant	1
3	Support, côté droit	1
4	Vis à tête ronde M4x12	4
5	Rondelle à ressort 4,1	10
6	Etrier de verrouillage	2
7	Support, côté gauche	1
8	Etrier	2
9	Rail téléscopique	2
10	Vis noyée M4x10	6
11	Ecrou hexagonal M4	6
12	Etrier	2
13	Vis à tête ronde M5x10	8
14	Rondelle à ressort 5,1	8
15	Rondelle 5,3x10	8
16	Rondelle enjoliveuse 5,3x12	4
17	Vis noyée M5x12	4

Instructions d'assemblage

Montage des rails téléscopiques

- Visser les étriers rep. 8 sur les rails téléscopiques (rep. 9) à l'aide des vis à tête noyée (rep. 10), des rondelles à ressort (rep. 5) et des écrous hexagonaux (rep. 11). Les trous de montage sont accessibles par une ouverture dans le guide central des rails téléscopiques.
- Visser les étriers (rep. 12) sur l'extrémité arrière des rails téléscopiques à l'aide d'un même nombre de postes 5, 10 et 11.
- Visser l'ensemble entre les supports de montage du rack ou coffret 19" à l'aide des vis à tête ronde (rep. 13) des rondelles (rep. 14) et des rondelles à ressort (rep. 15).

Poignée

Pour déposer la poignée procéder comme suit:

- Déposer les couvercles supérieur et inférieur de l'appareil.
- Déposer le profilé en matière plastique (montage déclic) en le faisant légèrement pivoter sous un seul angle.
- Déposer les quatre vis fixant la poignée aux étriers.
- Enfoncer les boutons-poussoirs dans les étriers et tourner la poignée en position horizontale au-delà de l'arête supérieure de l'oscilloscope.
- Maintenir enfoncé le bouton-poussoir droit et tirer l'étrier hors du pivotement.
- Déposer la poignée de l'autre étrier.
- Enfoncer le bouton-poussoir de l'étrier gauche et tourner en position horizontale, sous la base de l'appareil.
- Maintenir le bouton-poussoir enfoncé et tirer l'étrier hors du pivotement.

Fixation des poignées et supports au panneau avant

Visser les supports (rep. 3 et 7) par les trous (rep. 2) du panneau avant sur les poignées à l'aide des vis à tête ronde (rep. 4) et de la rondelle à ressort (rep. 5).

Fixation du panneau avant sur l'oscilloscope

Tirer les supports (rep. 3 et 7) légèrement vers l'extérieur et faire coulisser le panneau avant sur le front d'oscilloscope.
S'assurer que les parties étroites des ouvertures pointent vers le sommet de l'oscilloscope. Si elles pointent vers le bas, tourner l'ensemble panneau avant/support 180^o et le fixer à nouveau sur l'oscilloscope. Faire coulisser les ouvertures dans les supports au-delà des pivotements de poignée.
Fixer les supports sur l'oscilloscope en introduisant les étriers de verrouillage (rep. 6) dans les encoches des pivotements.

Montage de l'oscilloscope sur les rails téléscopique

Tirer les rails téléscopiques entièrement hors de l'armoire.
Faire coulisser les ouvertures dans les supports (rep. 3 et 7) au-delà des écrous à tête ronde à l'avant des rails.
Veiller à ce que l'oscilloscope coulisse jusqu'à la partie étroite des ouvertures reposent sur les écrous à tête ronde.
Faire coulisser l'ensemble dans le rack ou l'armoire et fixer le panneau à l'aide des vis à tête noyée (rep. 17) et des rondelles enjoliveuses (rep. 16).

Extraction de l'oscilloscope permettant l'inspection aisée

Tirer l'oscilloscope entièrement hors du rack ou de l'armoire.
Désengager les trous clés des vis à tête ronde et faire culbuter l'oscilloscope jusqu'à ce que l'avant repose sur le rack ou l'armoire. Pour fixer à nouveau l'oscilloscope en position normale, procéder en ordre inverse.

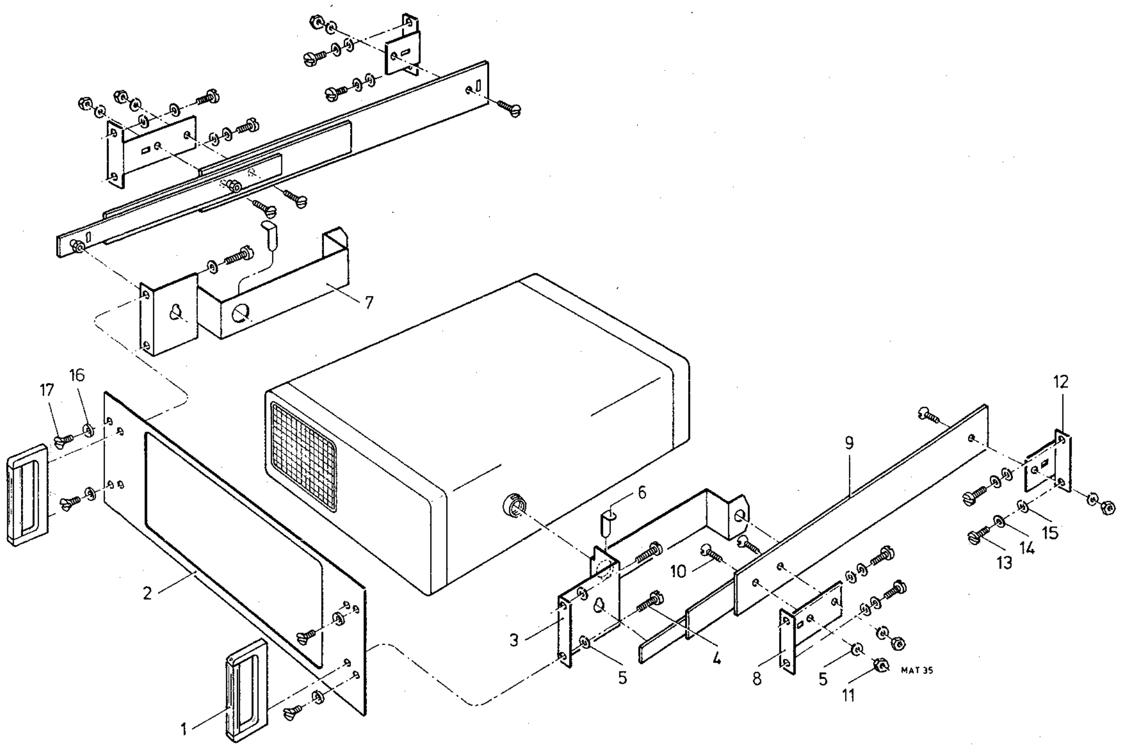


Fig. 1.20.

1.4.2.3. Interface IEC-bus PM 3325

Généralités

Le PM 3325 est un interface bus à buts multiples comforme à CEI - TC 66, auto-contrôle inclus.
La sélection d'adresse se fait à l'aide de 5 commutateurs (5 bits les moins significatifs des caractères ASCII).
Une indication de fonction de carte est également comprise.

Ensemble des fonctions d'interface pour PM 8210

Fonction d'interface	*Symbole*	*Identification*	*Remarque*
Handshake source	SH	SH1	
Handshake accepteur	AH	AH1	
Fonction orateur	T	T6	
Fonction auditeur	L	L4	
Demande service	SR	SR1	Le PM 3310 est capable d'envoyer une demande service
Distance/local	RL	RL2	Ne s'applique pas
Remise de l'unité	DC	DC1	
Interrogation parallèle	PP	PP0	Ne s'applique pas
Déclenchement de l'unité	DT	DT1	
Fonction contrôleur	C	C0	Ne s'applique pas

Demande service (SRQ)
Le PM 3310 est capable d'envoyer une SRQ pour indiquer une condition spéciale de l'appareil
Une demande de service est donnée:
- Lorsque le measurement est achevée.
- Aprés la mise en serivce ou la remise à zéro, si le procédé de départ est terminé.
- Si un code de programmation incorrect a été reçu.

Après une SRQ le contrôleur peut adresser le PM 3310 en tant que "orateur interrogation série", le mot de statut étant alors réglé sur bus (DI08 ... DI07).

Un mot de statut est constitué comme suit:

bit 8	Pas employée
bit 7 . . . "1"	Une SRQ a été donnée par le PM 3310
"0"	Aucune SRQ n'est donnée
bit 6 . . . "1"	Si une erreur est indiquée.
"0"	Condition normal
bit 5 . . . "1"	Occupé
"0"	Prêt
bit 4 . . .	
bit 3 . . .	Pas employée
bit 2 . . .	
bit 1 . . .	

1.5. PRINCIPES DE FONCTIONNEMENT (voir Fig. 1.21)

Dans la présente section, les principes de fonctionnement du PM 3310 sont discutés à partir du schéma synoptique et plus spécialement les points qui diffèrent de l'oscilloscope normal (par ex. les possibilités de stockage digital et de commande).

1.5.1. Généralités

L'oscilloscope à mémoire digitale PM 3310 comprend quatre sections:
- un système d'acquisition des signaux
- une section mémoire
- une section affichage
- une section commande

Ces quatre sections sont détaillées ci-après.

1.5.2. Système d'acquisition des signaux

Le signal d'entrée à afficher est appliqué au sélecteur de voies par un atténuateur et un amplificateur. Les réglages sur panneau avant sont balayés par la section commande (système microprocesseur).
Après le décodage, cette information est appliquée à l'atténuateur, l'amplificateur et le sélecteur de voies pour déterminer les caractéristiques correctes.
La sortie du sélecteur de voies est alimentée au convertisseur analogique-digital (ADC) afin de convertir le signal analogique sous forme digitale. Une conversion est démarrée lorsque le convertisseur reçoit une impulsion de commande à partir de la logique de commande d'acquisition (ACL). A la réception d'une impulsion de commande, une valeur analogique instantanée du signal d'entrée est convertie en mot digital par le convertisseur.
Un signal de déclenchement dérivé de la voie A, de la voie B d'une entrée externe ou de la fréquence secteur est appliqué au compteur de retard de déclenchement. Après un certain temps déterminé par le préréglage du compteur de retard une impulsion de déclenchement est produite et appliquée à la logique de commande d'acquisition.

1.5.3. Section mémoire

Après une conversion analogique-digital, la logique de commande d'acquisition (ACL) fournit une impulsion d'horloge pour le registre à décalage. A chaque impulsion d'horloge un mot digital de la sortie ADC est mémorisée dans le registre à décalage et toutes les informations mémorisées sont décalées d'une position.
La capacité du registre à décalage est de 256 mots digitaux et donc 256 valeurs analogiques instantanées converties.
Dès que le compteur de retard de déclenchement émet une impulsion de déclenchement à la logique ACL et que ACL a fourni plus de 256 impulsions au registre à décalage, ce dernier est rempli d'informations et ACL arrête de produire des impulsions d'horloge.
Le contenu du registre à décalage est prêt à être copié dans la mémoire RAM "ACCU". Le transfert d'informations du registre à décalage à ACCU est réglé par un procédé "handshake" afin d'obtenir un affichage sans clignotement sur le TRC. Lorsque le copiage est terminé, le registre à décalage est "prêt" (ready) et l'action redémarrée.
L'information mémorisée dans ACCU peut être copiée dans une des autres mémoires (STO 1, STO 2, STO 3). Chacune de ces mémoires RAM peut contenir 256 bytes d'information digitale. Avec les deux voies en service ("ON"), la capacité de mémoire est divisée également en 128 bytes par voie.

1.5.4. Section affichage

L'information dans les mémoires RAM peut alors être affichée.
Le contenu de chaque RAM est de 256 mots, composé chacun de 8 bits. Chaque mot de 8 bits est capable d'indiquer 256 amplitudes différentes (par ex. $2^8 = 256$): paramètres Y.
Chaque addresse de la mémoire correspond à une ligne verticale de l'affichage le long de l'axe X; par ex. l'affichage de 10 divisions est divisé en 256 lignes.
Comme chaque valeur de 8 bits par adresse constitue une valeur instantanée dans le sens Y, une aire d'affichage de 2 divisions verticales et 10 horizontales est divisées en 256 x 256 points. Lorsque Y x 5 est sélectionné, cette aire est agrandie à 256 x 256 points sur 10 x 10 divisions.
Un compteur d'adresse émet 256 addresses différentes en ordre (en commençant par l'adresse 0 et finissant par l'adresse 255) aux mémoires RAM et au convertisseur digital-analogique (DAC) du système X.
Pour produire les échelons discrets pour l'affichage de base de temps horizontale, la sortie de X-DAC est une

tension linéaire en escalier, laquelle est appliquée à l'amplificateur X par l'agrandisseur. La sortie résultante de l'amplificateur X passe par les plaques de déflexion horizontale du TRC.
De même, les valeurs instantanées à 8 bits pour chaque adresse (par ex. l'information Y) sont converties en signaux analogiques à l'aide de Y-DAC. Grâce à l'agrandisseur Y x 5, le signal converti est appliqué à l'amplificateur Y et ensuite aux plaques de déflexion verticale du TRC.

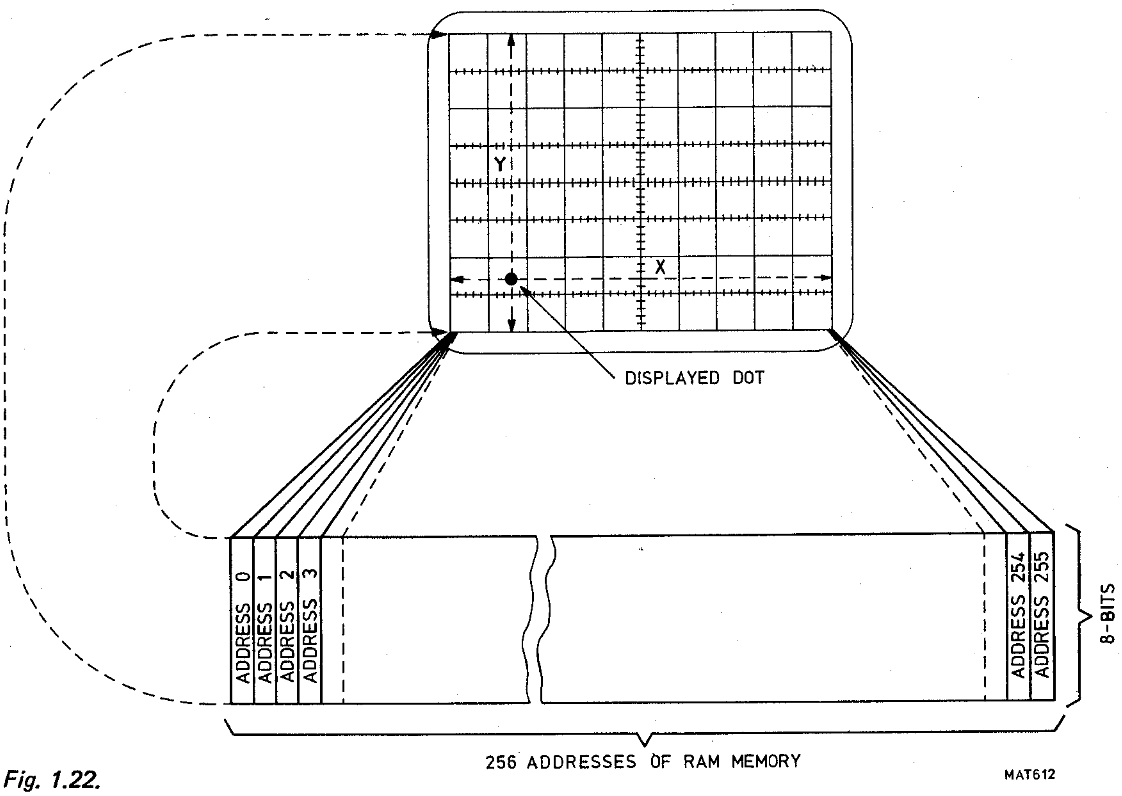


Fig. 1.22.

1.5.5. Section commande

La section commande consiste en un microprocesseur, des mémoires, des verrouillages, des portes (d'entrée et de sortie) et des circuits logiques correspondants.

– *Commutateurs sur panneau avant*

A un intervalle de temps défini, la section commande balaye tous les commutateurs du panneau avant, à l'exception des commutateurs de source de déclenchement et de mode de déclenchement.
Pour simplifier le fonctionnement, des réglages incorrects sont traduits en réglages significatifs (par ex. deux voies OFF seraient traduits en voie A ON).

– *Recalcul*

En mode Y x 5, les réglages de AMPL/DIV sont recalculés et affichés.

– *Commande d'affichage*

La commande de l'affichage complet a lieu à partir de la section commande. La section affichage comprend le TRC, les témoins, les diodes LED alphanumériques et les circuits correspondants.
L'affichage TRC est composé point par point. Pour obtenir une représentation de ligne la section commande fournit les signaux de liaison des points.

– *Procédé "handshake"*

Le système d'entrée (registre à décalage inclus) et le système d'affichage ont différents cycles de fonctionnement. Pour obtenir un affichage stable, les deux systèmes doivent être couplés par un procédé "handshake" dirigé par la section commande.
En plus de ces fonctions standard d'oscilloscope, la section commande supervise également la sortie pour table traçante et le traitement de l'option IEC-bus.

2. INSTALLATION

2.1. REGLEMENTS DE SECURITE (CONFORMES A LA CEI 348)

Avant de brancher l'instrument sur le secteur, examiner le boîtier, les commandes, les connecteurs, etc. afin de s'assurer qu'il n'y a pas eu de dommages en cours de transport. En cas de défauts, ne pas brancher l'instrument.

RECLAMATIONS: En cas de dommages ou d'insuffisances, ou si la sécurité de l'appareil est mise en doute, une réclamation doit être adressée directement au transporteur. De plus, il faudra également avertir une organisation de vente ou de service Philips afin de faciliter le procédé de réparation.

Avant de procéder à toute autre connection, la borne de terre de l'instrument doit être reliée à la ligne de terre du réseau (voir 2.5 mise à la terre).

REMARQUE: L'ouverture des capots ou l'enlèvement d'organes à l'exception de ceux directement accessibles à la main, sont susceptibles de découvrir des composants et des connecteurs sous tension.

L'instrument doit être débranché de toute source de tension avant de procéder à un réglage, un remplacement, une opération d'entretien ou une réparation nécessitant l'ouverture de l'instrument.
Si le réglage, l'entretien ou la réparation de l'instrument ouvert sous tension sont inévitables, seule une personne qualifiée peut se charger de cette tâche.
Ne pas oublier que les condensateurs à l'intérieur de l'instrument peuvent être chargés, même si l'instrument est déconnecté de toute source de tension.

2.2. DEMONTAGE ET MONTAGE DU COUVERCLE AVANT

Démontage:

- Tourner le bouton au centre du couvercle d'un quart de tour vers la gauche (position UNLOCKED).
- Enlever le couvercle.

Montage:

- Tourner le bouton de verrouillage vers position UNLOCKED.
- Fixer le couvercle sur la partie avant de l'oscilloscope.
- Enfoncer le bouton et le tourner d'un quart de tour vers la droite (position LOCKED).

L'espace creux dans le couvercle avant permet d'y placer des accessoires tels que sondes, visière, etc.
Pour ouvrir le couvercle, presser les langues de verrouillage et soulever le panneau intérieur.

2.3. POSITION DE L'APPAREIL

L'instrument peut être utilisé en toute position. A poignée rabattue, l'instrument peut être utilisé en position inclinée. Les spécifications conformément aux paragraphe 1.2. ne sont garanties qu'en position normale ou avec poignée rabattue (s'assurer que la grille de ventilation au-dessus et en-dessous du boîtier n'est pas obturée).
Il n'est pas recommandé de placer l'instrument en plein soleil ou sur une surface produisant de la chaleur.
La poignée peut être tournée en appuyant sur les boutons-poussoirs aux étriers.

2.4. ADAPTATION A LA TENSION SECTEUR ET FUSIBLE

Avant de raccorder le secteur, s'assurer que l'instrument est réglé sur la tension secteur locale.
Pour ce faire, utiliser le commutateur MAINS ADAPTOR SWITCH à 2 positions à l'arrière. Ces deux positions permettent d'utiliser l'appareil sur toute tension secteur entre 100 et 120 V ± 10 % (115 V affiché dans la fenêtre de MAINS ADAPTER SWITCH) d'une part, et entre 220 et 240 V ± 10 % (230 V affiché dans la fenêtre). Le porte-fusible monté sur le panneau arrière porte un fusible lent de 2 A (4822 253 30025).

En cas de remplacement, les fusibles de rechange seront correctement calibrés et d'un modèle adéquat.
Il faut éviter d'utiliser des fusibles réparés ou de court-circuiter des porte-fusibles. En cas de remplacement d'un fusible ou d'adaptation à une autre tension secteur, l'instrument sera débranché de toute source de tension.

Remarque: Le même fusible lent 2 A est applicable pour tous les réglages de l'adaptateur secteur.

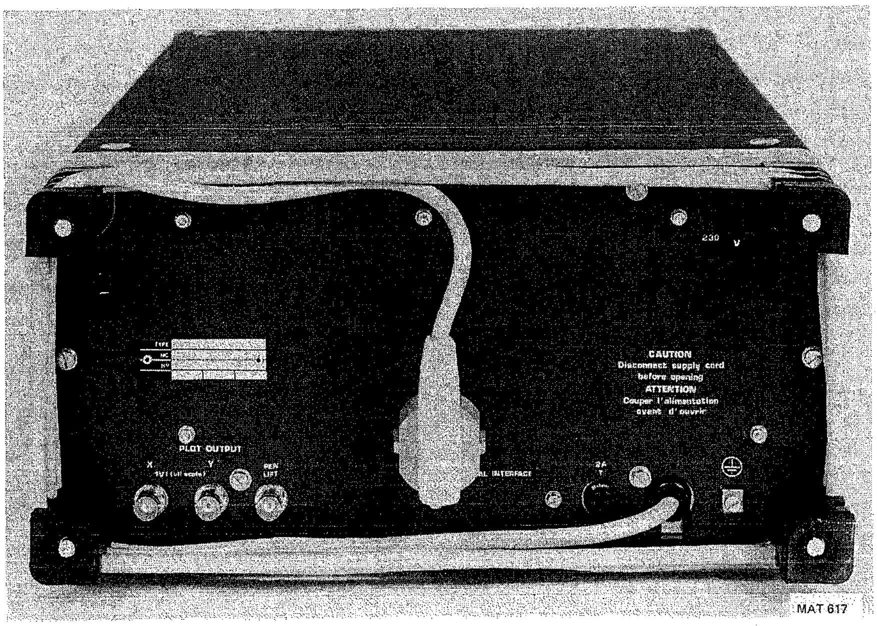


Fig. 2.1. Vue arrière illustrant adaptateur secteur et fusible.

En cas de non-emploi, le cordon secteur peut être enroulé autour des pieds disponibles sur le panneau arrière.

2.5. MISE A LA TERRE

Avant toute mise sous tension, l'instrument doit être connecté à la terre.

- Par la borne de terre de l'appareil.
- Par le cordon secteur à trois conducteurs. La fiche secteur ne sera introduite que dans une prise possédant un contact de terre. La mise à la terre ne doit pas être éliminée par l'emploi d'un câble prolongateur sans conducteur de terre.

ATTENTION: Toute interruption de la ligne de terre, à l'intérieur ou à l'extérieur de l'instrument, tout débranchement de la borne de terre peut rendre l'instrument dangereux. L'interruption intentionnelle de la ligne de terre est formellement interdite.

Lorsqu'un instrument passe d'un endroit froid à un endroit chaud, la condensation peut provoquer un certain risque. En conséquence, il faut appliquer strictement les prescriptions de mise à la terre.

3. INSTRUCTIONS D'UTILISATION

3.1. GENERALITES

La présente section décrit les travaux et précautions requises à l'utilisation. En outre, elle décrit sommairement les fonctions des commandes et des indicateurs et met en évidence les aspects pratiques du fonctionnement. De la sorte, un opérateur peut rapidement se familiariser avec les fonctions principales de l'instrument.

3.2. ENCLENCHEMENT ET TEST D'ALIMENTATION

3.2.1. Enclenchement

Lorsque l'instrument est branché au secteur comme indiqué aux paragraphes 2.4 et 2.5, il peut être enclenché à l'aide du bouton poussoir POWER. Le commutateur POWER est incorporé dans la commande d'illumination de graticule ILLUM (panneau avant), immédiatement sous le bord de l'écran. Le témoin POWER ON/OFF est proche de la commande ILLUM.
L'instrument est immédiatement en état de fonctionner, après enclenchement. Les caractéristiques techniques selon le paragraphe 1.2 ne sont valables que dans une situation normale — conforme à la section 2 — et après un temps d'échauffement de 30 min.

ATTENTION: L'instrument ne doit jamais être enclenché lorsqu'une platine ou un bloc a été enlevé (à l'exception des circuits IEC et SPARE). Ne déposer de platine ou de bloc qu'une minute au moins après la mise hors service de l'instrument.

3.2.2. Test d'alimentation

A l'enclenchement de l'appareil, le microprocesseur incorporé démarre un test automatique de plusieurs circuits internes:

- Test de démarrage
- Test PROM
- Test d'affichage LED
- Test RAM

Le test est automatiquement démarré après l'enclenchement. A la fin du cycle de test, tous les témoins, indicateurs et l'affichage alphanumérique s'allument pendant environ 3 secondes et ensuite l'oscilloscope passe en mode de fonctionnement normal. Si, pendant le test, un circuit défectueux est trouvé, le test est arrêté.

Ceci est visible:

1. l'appareil ne passe pas en mode de fonctionnement normal
2. un certain nombre de témoins et d'indicateurs (pas tous) sont allumés

Dans ce cas, il est recommandé de mettre l'appareil hors service et après quelques secondes à nouveau en service. Si, après l'enclenchement, la même condition fautive est enregistrée, contacter votre département de service Philips ou vérifier conformément au chapitre 9 de la notice d'entretien. Si un témoin et un indicateur ou plus ne s'allument pas et que l'appareil passe en mode fonctionnel après les tests, ce témoin (indicateur) peut être défectueux.

Si, pendant le fonctionnement, le système est bloqué — dû par exemple à de très hautes tensions statiques — un déclenchement/enclenchement remet automatiquement le système à microprocesseur et l'oscilloscope redevient fonctionnel.

3.3. COMMANDES ET PRISES

Les commandes et les prices sont toutes reprises dans les sections correspondantes et accompagnées d'une brève description.

3.3.1. Section TRC

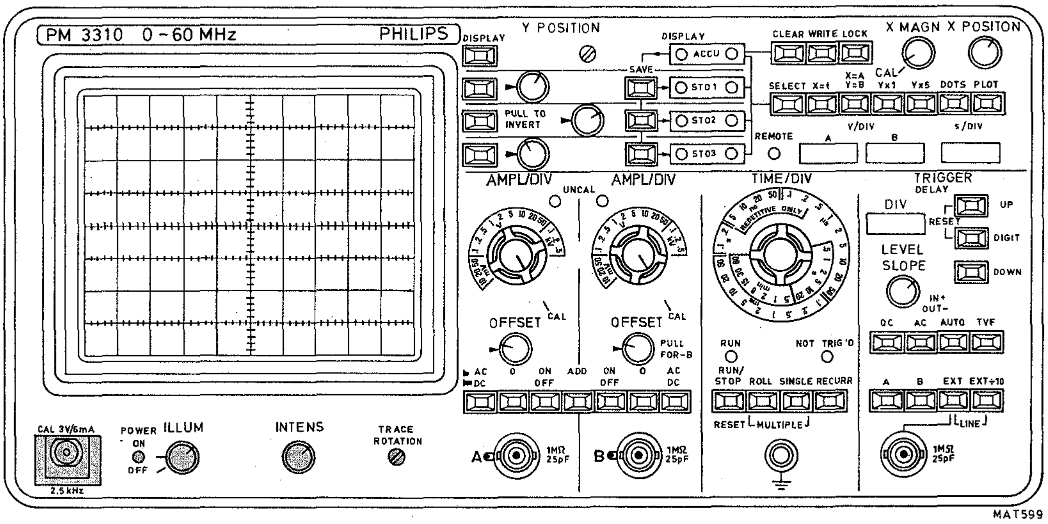
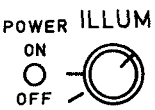


Fig. 3.1.

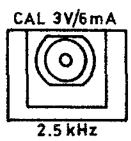


Commande continûment variable de l'illumination de graticule incorporant le commutateur POWER ON/OFF (en service/hors service).
Témoin indiquant la mise en service.

Commande continûment variable de l'intensité de trace.

Remarque: Le PM 3310 est équipé d'une commande de focalisation automatique, de sorte que le réglage de foyer est superflu.

Commande de préréglage pour alignement de la trace sur les lignes de graticule horizontales (réglage par tournevis).



Sortie 3 V_{CC} (tension rectangulaire 2,5 kHz) permettant de calibrer la commande AMPL de déflexion verticale ou de compenser la fréquence des sondes pour diviseur de tension.
Boucle de courant avec 6 mA_{CC} pour étalonnage des sondes de courant.

3.3.2. Section verticale

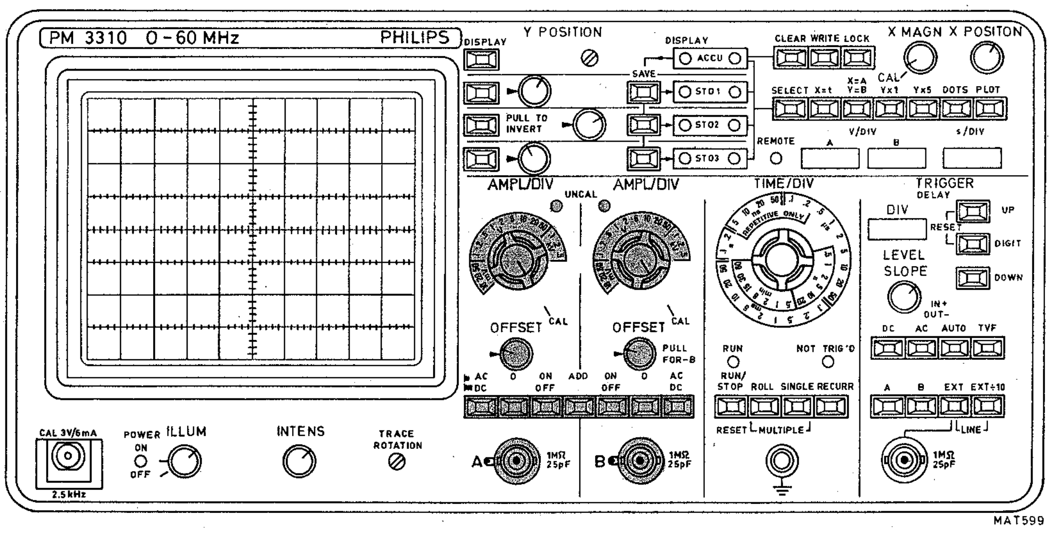
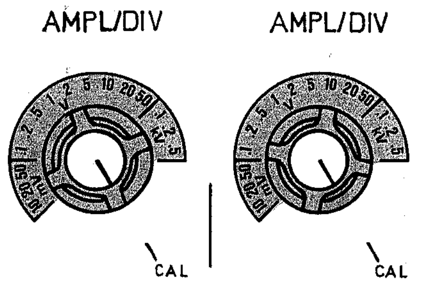


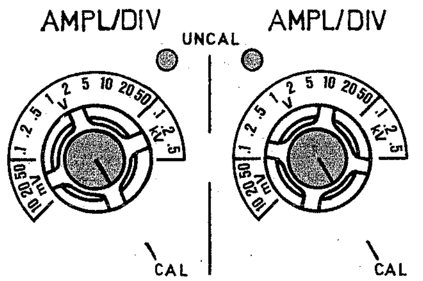
Fig. 3.2.



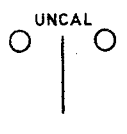
Commande à 12 échelons des coefficients de déflexion verticale en progression 1-2-5.
Avec une sonde 10:1 munie d'une indication de gamme* le réglage a lieu automatiquement de 0,1 V/div à 0,5 kV/div.
Avec une sonde 1:1 le réglage est possible de 10 mV/div à 50 V/div.

Deux témoins sont situés sous l'échelle extérieure du bouton AMPL/DIV. Normalement un des témoins (gauche) est allumé; mais si une sonde 10:1 avec indicateur est appliquée, le témoin de droite est allumé.

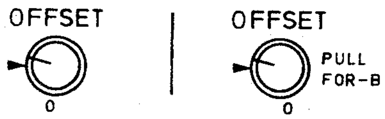
* Des sondes avec indication de gamme sont livrées avec l'appareil.



Commande continûment variable des coefficients de déflexion verticale. En position CAL le coefficient de déflexion sélectionné est étalonné.



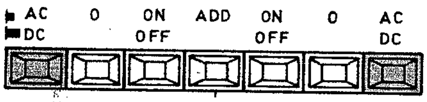
Témoin indiquant que le commutateur AMPL/DIV correspondant n'est pas en position CAL. Ceci est indiqué par un astérisque dans l'affichage alphanumérique.



Commande continue pour décalage du signal dans la gamme dynamique de la mémoire (2 divisions sur l'écran).

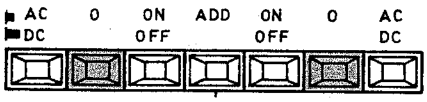
Si une partie du signal pénétrant est décalé hors de la gamme dynamique de mémoire cette partie est affichée sur le TRC comme une ligne droite clignotante dans la partie supérieure ou inférieure de la section affichage mémoire; ceci est en fonction du fait que le signal est décalé hors de la gamme dynamique supérieure ou inférieure.

Si le signal complet est décalé hors de la gamme dynamique, une ligne droite clignotante complète sera affichée. La gamme offset est de ± 4 fois de réglage d'atténuateur sélectionné.
Un commutateur push-pull (deux positions) est incorporé dans la commande OFFSET de la voie B, lequel permet d'inverser la polarité (PULL FOR –B). Le mode normal est obtenu en position enfoncée de cette commande et le mode –B en position tirée.

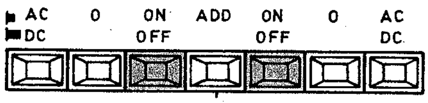


Lorsque AC/DC est enfoncé le couplage d'entrée Y correspondant est obtenu par l'intermédiaire du condensateur de blocage (AC).

En position relâchée de AC/DC le couplage d'entrée est direct (DC).



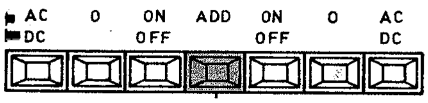
En position enfoncée de 0, la connexion entre la douille d'entrée Y et son circuit d'entrée est interrompue et le circuit d'entrée mis à la terre.



En position enfoncée de ON/OFF, la déflexion verticale est obtenue par le signal connecté à la douille d'entrée de la voie Y correspondante.

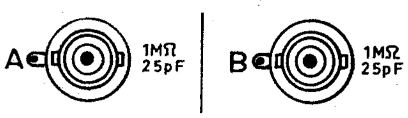
En position relâchée de ON/OFF, la trace de la voie Y correspondante n'est pas affichée.
Pour simplifier le fonctionnement avec les deux boutons ON/OFF relâchés, la voie A sera affichée (par ex. le circuit tolère l'erreur humaine!).

Si les deux voies A et B sont enclenchées par l'enclenchement (ON) des boutons-poussoirs ON/OFF, les deux signaux sont stockés dans la mémoire accumulateur. Le contenu de cette mémoire ACCU est généralement affiché dans les deux divisions supérieures de l'écran TRC (voir également section affichage).



En position enfoncée de ADD, le signal de somme (A + B) des voies A et B est affiché.
Combiné avec l'action de PULL FOR –B, A-B sera affiché.
Le mode ADD peut être sélectionné indépendamment des réglages de commutateur ON/OFF. Par exemple, si la voie A est commutée sur OFF et la voie B sur ON, les commandes A et B OFFSET sont fonctionnelles.

Remarque: Lorsque tous les boutons-poussoirs sont relâchés, la voie A est automatiquement sélectionnée.



Prise d'entrée BNC comprenant une entrée pour indication de gamme.

3.3.3. Section horizontale

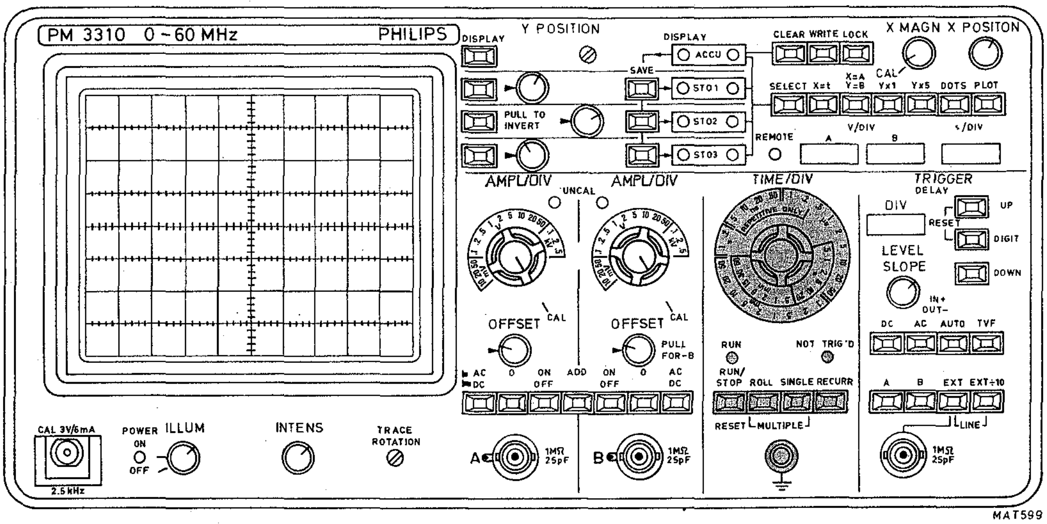
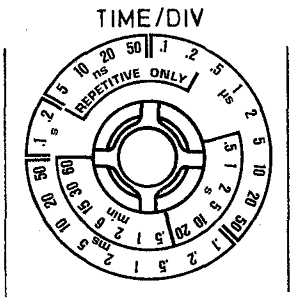


Fig. 3.3.



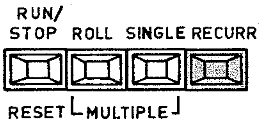
Commande échelonnée du coefficient de temps de la base de temps: commutateur rotatif à 24 positions (sans arrêt). La position sélectionnée est indiquée par un des témoins situés sous l'échelle de ce bouton. Dans les positions marquées REPETITIVE ONLY, seuls des signaux de caractère répétitif peuvent être mesurés.

La bague intérieure sert uniquement en mode ROLL et est indiquée automatiquement en cas de sélection du mode ROLL. L'affichage correct du signal d'entrée sur l'écran TRC peut être trouvé en tournant le bouton TIME/DIV de rapide à lent (en portant de la position 0,5 ns/div) jusqu'à ce que le premier affichage déclenché soit obtenu.

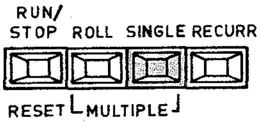
Témoin indiquant que le mode ROLL est fonctionnel et actif. Ce témoin clignote pour indiquer que le travail en mode ROLL est achevé (voir également la description de la fonction "ROLL").

Témoin indiquant qu'il n'y a pas de signal de déclenchement Si le témoin reste éteint, cela veut dire:

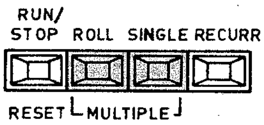
A. que la base de temps est déclenchée en mode ROLL/ RECURR
B. que le signal est capturé en mode SINGLE/MULTIPLE.



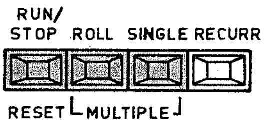
Lorsque RECURR est enfoncé, la mémoire ACCU est constamment alimentée par des informations nouvelles. Ceci a lieu à des intervalles de temps fonction de la position TIME/ DIV et du réglage du retard de déclenchement.



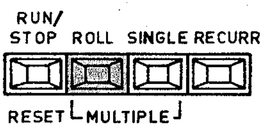
Lorsque SINGLE est enfoncé, le rafraîchissement de la mémoire ACCU a lieu une seule fois au moment où le niveau de déclenchement est atteint et que le temps réglé avec retard est écoulé.
Ce rafraîchissement a uniquement lieu en appuyant sur le bouton RESET. Le signal est démarré en fonction de la position du retard de déclenchement. Pendant l'attente, le contenu d'accumulateur est affiché et la lampe NOT TRIG'D allumée.



Lorsque les boutons ROLL et SINGLE sont enfoncés, le mode MULTIPLE est sélectionné.
L'action SINGLE a lieu 4 fois après avoir appuyé une fois le bouton RESET.
Le premier résultat est emmagasiné dans la mémoire STO 3, le second dans la mémoire STO 2, le troisième dans la mémoire STO 1 et le dernier dans la mémoire ACCU.



Si le mode SINGLE ou MULTIPLE est sélectionné, la base de temps peut être démarrée à nouveau en enfonçant le bouton RESET.

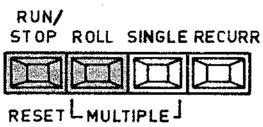


Lorsque ROLL est enfoncé, le signal est établi point par point sur la partie droite de l'écran et se déplace vers la gauche après avoir enfoncé le bouton R/S.
Le témoin RUN indique que le mode ROLL est fonctionnel.

Lorsque l'accumulateur est entièrement repli, l'information est conservée dans la mémoire STO 3, la suivante dans la mémoire STO 2, la suivante dans la mémoire STO 1 et la dernière dans la mémoire ACCU (le témoin RUN est continûment allumé).
Ensuite le mode ROLL est arrêté et le témoin RUN clignote pour indiquer cette condition.

Le mode ROLL peut être utilisé dans les positions 0,5 sec./div à 60 min/div indiquées par l'indicateur intérieur du commutateur TIME/DIV. Si le commutateur TIME/DIV est réglé hors de la gamme, l'indicateur dans la bague extérieure du commutateur TIME/DIV clignote.
Dans ces positions le mode ROLL est continué, mais en échelons de 0,5 sec/div.

L'information totale ne sera visible sur le TRC après avoir enfoncé les quatre boutons d'affichage pour ACCU, STO 1, STO 2 et STO 3.



Lorsqu'on enfonce le bouton CLEAR, le contenu de la mémoire ACCU est effacé et le mode ROLL peut être redémarré en enfonçant le bouton R/S (voir également section affichage).

Pendant le mode ROLL (par exemple témoin RUN allumé continûment) l'action peut être arrêtée et/ou démarrée en enfonçant le bouton RUN/STOP.

Lorsque le mode ROLL est arrêté par le bouton RUN/STOP, la fonction marche/arrêt de ce bouton peut être reprise par un signal appliqué à l'entrée de déclenchement EXT (niveau TTL):
+5 V ($>$ +2,4 V) logique HIGH signifie RUN (marche)
0 V ($<$ 0,8 V) logique LOW signifie STOP (arrêt).

Remarque: Pour simplifier l'opération, RECURR est automatiquement sélectionné lorsque tous les boutons sont relâchés.

Prise de terre de mesure.

3.3.4. Déclenchement

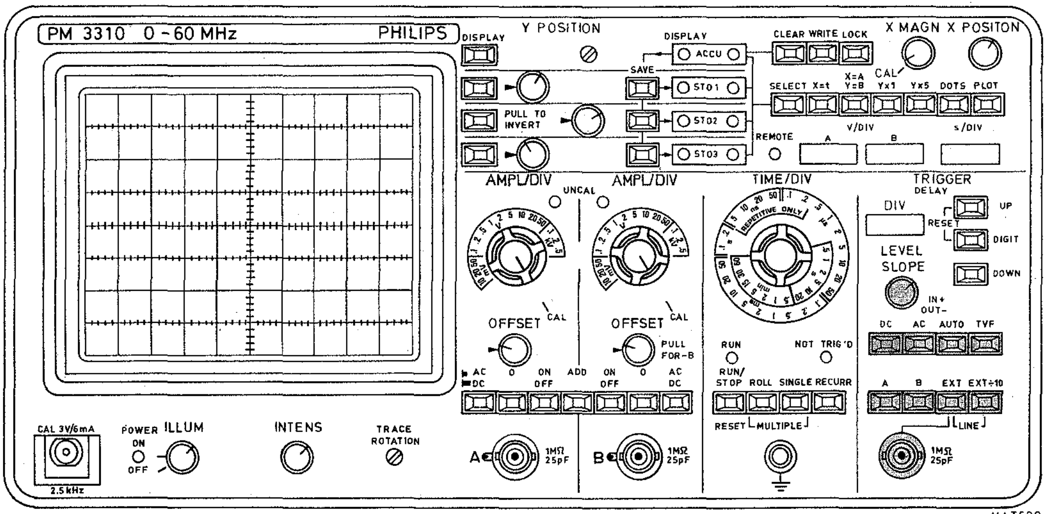
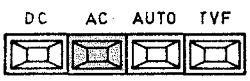


Fig. 3.4.

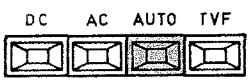
Commande continûment pour sélectionner le niveau du point de déclenchement sur le signal d'entrée.
Cette commande comprend un commutateur push-pull qui permet de choisir le déclenchement soit sur le flanc positif, soit le flanc négatif (IN +, OUT –).

Sélection du mode de déclenchement

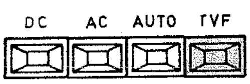
Avec DC enfoncé le générateur de base de temps est déclenché par un signal de déclenchement comprenant DC (largeur de bande de déclenchement: continu à 60 MHz).



Avec AC enfoncé le générateur de base de temps est déclenché par un signal dont la composante continue est bloquée (largeur de bande de déclenchement: 10 Hz à 60 MHz).



Avec AUTO sélectionné la base de temps est en fonctionnement libre en l'absence de signaux de déclenchement (la composante continue est bloquée dans ce mode et la largeur de bande de déclenchement se situe entre 20 Hz et 60 MHz).

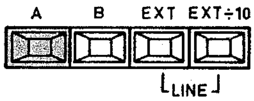


Avec TVF sélectionné on obtient la synchronisation du signal de trame pour télévision. (Pour le système CCIR 625 lignes.)

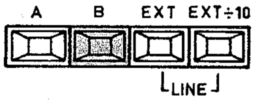
Remarque: Pour simplifier l'opération, le mode AUTO est sélectionné lorsque tous les boutons sont relâchés.*

* Vérifier le réglage correct de la pente de déclenchement (en fonction du système de télévision testé).

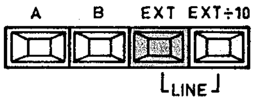
Sélection de la source de déclenchement



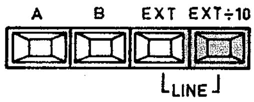
Avec A enfoncé, le déclenchement se fait sur un signal interne dérivé de la voie A.



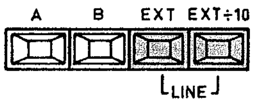
Avec B enfoncé le déclenchement se fait sur un signal interne dérivé de la voie B.



Avec EXT enfoncé le déclenchement provient d'un signal externe par la prise d'entrée de déclenchement EXT adjacente (1 MΩ//25 pF).

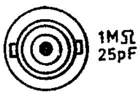


Avec EXT ÷ 10 enfoncé, un déclenchement externe est obtenu, lequel a lieu par l'intermédiaire d'un diviseur de tension incorporé 10 : 1.



Avec les boutons EXT et EXT ÷ 10 enfoncés, le déclenchement se fait par un signal interne dérivé de la tension secteur. (LINE)

Remarque: Pour simplifier l'opération, A est automatiquement sélectionné lorsque tous les boutons sont relâchés.



Prise d'entrée BNC pour déclenchement externe et signal RUN/STOP externe pour mode ROLL.

3.3.5. Retard de déclenchement

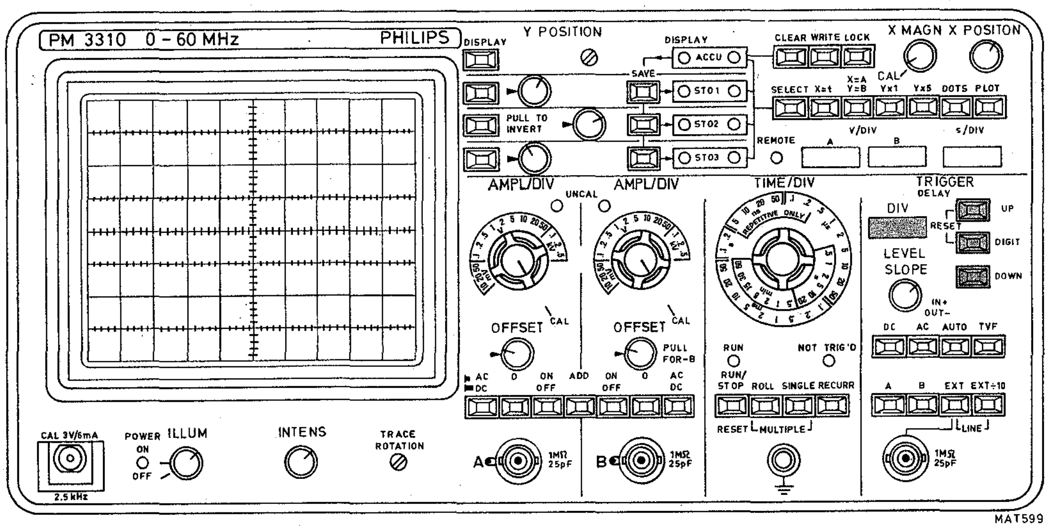
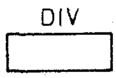


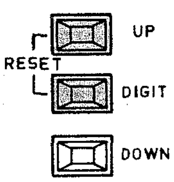
Fig. 3.5.



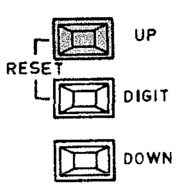
Affichage à 4 décades indiquant le temps sélectionné en divisions entre l'impulsion déclenchement et le début du signal affiché sur TRC. Ce retard de déclenchement peut durer entre –9 et +9999 en positions 0,2 s à 0,5 μs/div du commutateur TIME/DIV.
En positions 0,2 s à 5 ns/div du commutateur TIME/DIV (uniquement pour signaux répétés), la gamme de temps de retard est de 0 à 100 divisions.

Lorsque l'appareil est mis en circuit, l'affichage est automatiquement remis à zéro, sauf en cas d'assistance mémoire, car dans ce cas la valeur emmagasinée en dernier lieu est affichée.

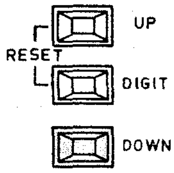
En mode ROLL le texte OFF sera affiché.



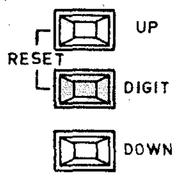
Lorsque les deux boutons-poussoirs UP et DIGIT sont enfoncés, le temps de retard de déclenchement est remis à zéro. Ceci est indiqué dans l'affichage DIV.



Le temps de retard de déclenchement peut être accord en appuyant sur le bouton UP.



Le temps de retard de déclenchement peut être réduit en appuyant sur le bouton DOWN.



La décade dans laquelle le comptage sera effectué, peut être sélectionné en appuyant sur le bouton DIGIT, le bouton UP ou DOWN étant également actionné.
Le chiffre sélectionné clignote dans l'affichage.

Si l'on appuie plusieurs fois sur DIGIT, les décades sont sélectionnées à tour de rôle (scrolling).
On passe de la décade la moins significative à la décade la plus significative pour repasser ensuite la décade la moins significative.

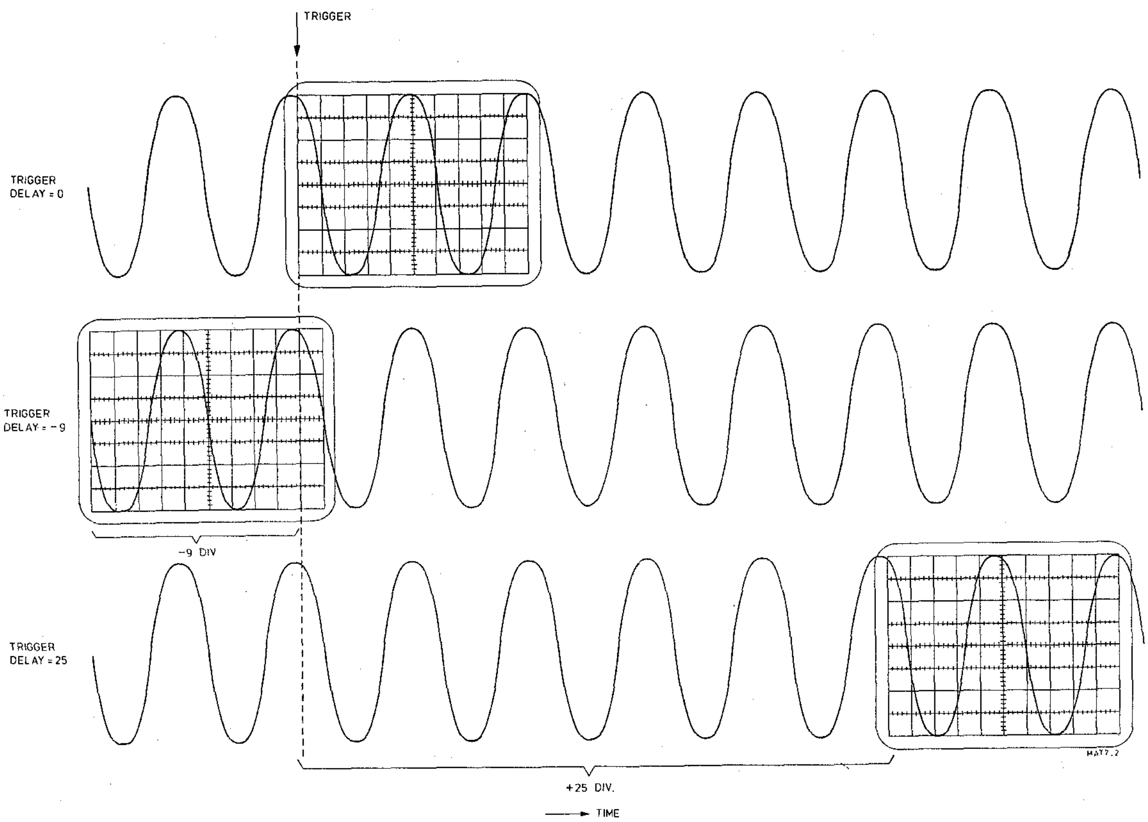


Fig. 3.6.

3.3.6. Section affichage

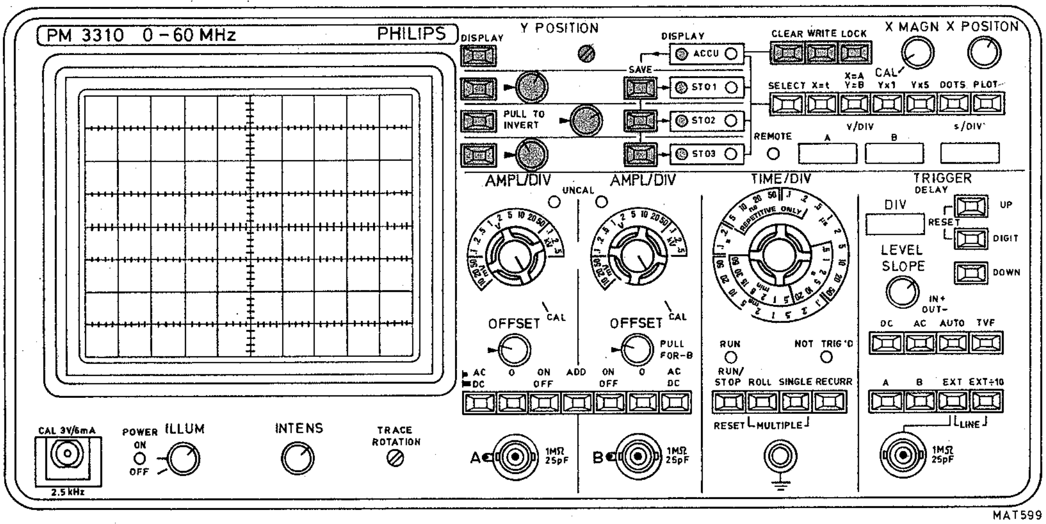


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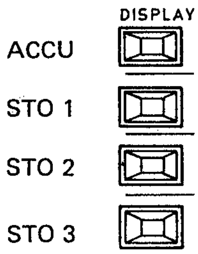
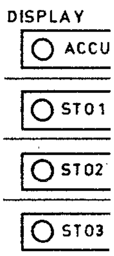
Fig. 3.7.

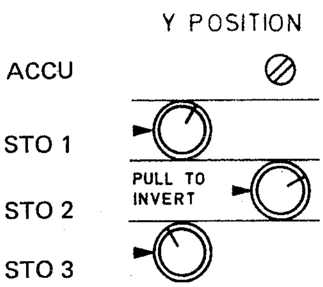


En fonction des réglages des boutons-poussoirs DISPLAY, le contenu d'une mémoire ou plus (ACCU, STO 1, STO 2 et STO 3) peut être sélectionné pour l'affichage sur l'écran TRC.

Si aucun bouton DISPLAY n'est enfoncé, la diode LED ACCU indique que la mémoire ACCU est sélectionnée. Ceci peut être influencé en appuyant sur le bouton SELECT. Dans le cas où tous les boutons-poussoirs sont relâchés, la dernière mémoire mise hors circuit est sélectionnée.



Ces voyants indiquent que les mémoires sont sélectionnées pour affichage sur l'écran TRC à l'aide des boutons DISPLAY ou du bouton SELECT, lorsque tous les boutons DISPLAY sont relâchés.



Commandes continûment variables pour décalage vertical de l'affichage.
Dans la position , les voies sont disposées de façon égale sur l'aire utile de l'écran. Chaque voie occupe deux divisions sur l'écran (voir figure).
La position ACCU est réglée par tournevis.

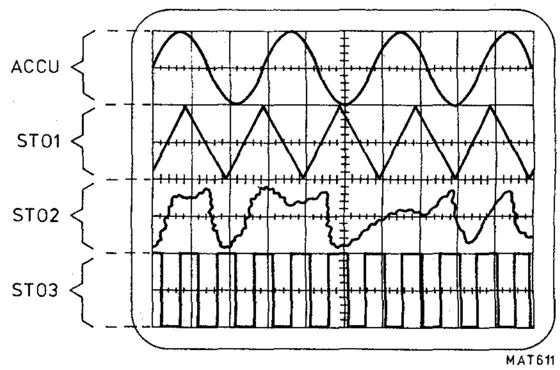


Fig. 3.8.

PULL TO INVERT
(Tirer en mode inversé)

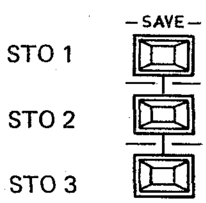
Commutateur push-pull intégré aux commandes STO 1, STO 2 et STO 3 POSITION pour l'inversion des signaux sur l'écran TRC. Enfoncées, ces commandes sont en mode normal et tirées en mode inversé (PULL TO INVERT).

En enfonçant le bouton CLEAR le contenu de la mémoire ACCU est effacé.
Les trois autres mémoires peuvent seulement être effacées en tranférant le contenu de mémoire effacée de ACCU dans ces mémoires (voir également la fonction des boutons SAVE).
Le mode ROLL peut être redémarré en enfonçant le bouton-poussoir CLEAR et ensuite le bouton RUN/STOP.

Lorsqu'on enfonce le bouton WRITE, le signal d'entrée est écrit dans la mémoire ACCU après une impulsion de déclenchement et après le retard préréglé (voir également section 3.3.4. Déclenchement).

Lorsqu'on enfonce le bouton LOCK, le système de mémoire est entièrement bloqué, ce qui signifie que le contenu de ACCU, STO 1, STO 2 et STO 3 ne peut être modifié dans ce mode.

Remarque: Pour faciliter le fonctionnement, le mode WRITE est automatiquement sélectionné lorsque tous les boutons-poussoirs sont relâchés.



Le contenu de la mémoire ACCU est retenu dans le registre sélectionné STO 1, STO 2 ou STO 3 en enfonçant le bouton-poussoir correspondant.
Au même moment, l'information indiquant les réglages des commandes AMPL/DIV (voies A et B), TIME/DIV et retard de déclenchement est stockée dans la mémoire interne de l'appareil, à des fins d'affichage alphanumérique (voir également V/DIV et s/DIV).

3.3.7. Réglages AMPL/DIV et TIME/DIV

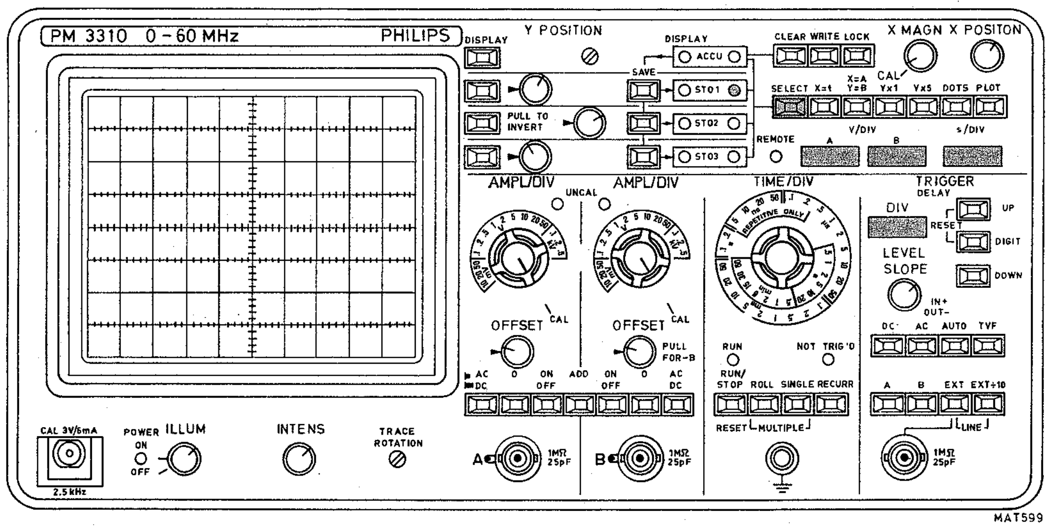
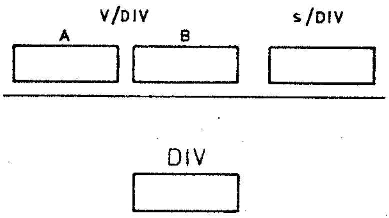
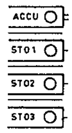


Fig. 3.9.



Les affichages indiquent les réglages AMPL/DIV et TIME/DIV et ceux du retard de déclenchement pour le registre dont le voyant est allumé:



Pour afficher les réglages de commutateur d'une des quatre mémoires, actionner le bouton SELECT.
Les mémoires non-affichées sont sautées.
L'affichage indique une mantisse (partie décimale) et un exposant.

Cet exposant peut être:

- Nul (0) pour indiquer volts ou secondes
- –3 pour mV ou ms
- –6 pour µs
- –9 pour ns

Un astérisque dans l'affichage indique aue la commande continue AMPL/DIV n'était pas en position CAL pendant le stockage des signaux dans une des mémoires; l'affichage indique alors une gamme plus sensible que pendant l'affichage.

Autres affichages possibles sont:

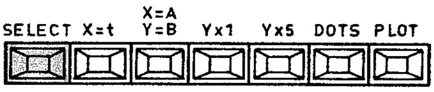
ADD : le mode ADD était fonctionnel

SUB : le mode SUB était fonctionnel (ADD avec voie B inversée)

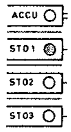
OFF : la voie correspondante n'était pas fonctionnelle

NOP : le réglage correspondant est sans intérêt (par ex. après la mise en service lorsque d'alimentation pour assistance de memoire n'est pas utilisée).

Remarque: En modes ADD et SUB, il est recommandé de régler les commutateurs A et B AMPL/DIV dans la même position afin de bien pouvoir interpréter le signal stocké.



En enfonçant le bouton-poussoir SELECT, la mémoire dont les facteurs d'échelle doivent être affichés, peut être sélectionnée. Dans ce mode, le système explore les mémoires sélectionnées à l'aide des boutons-poussoirs DISPLAY.
La mémoire sélectionnée à un certain moment est indiquée par le voyant correspondant.



Si le contenu d'une mémoire ou plus STO 1, STO 2 et STO 3 est affiché sur TRC de concert avec le contenu de mémoire ACCU, l'affichage alphanumérique est automatiquement commuté sur les réglages ACCU, en actionnant une des commandes illustrées ci-dessous.

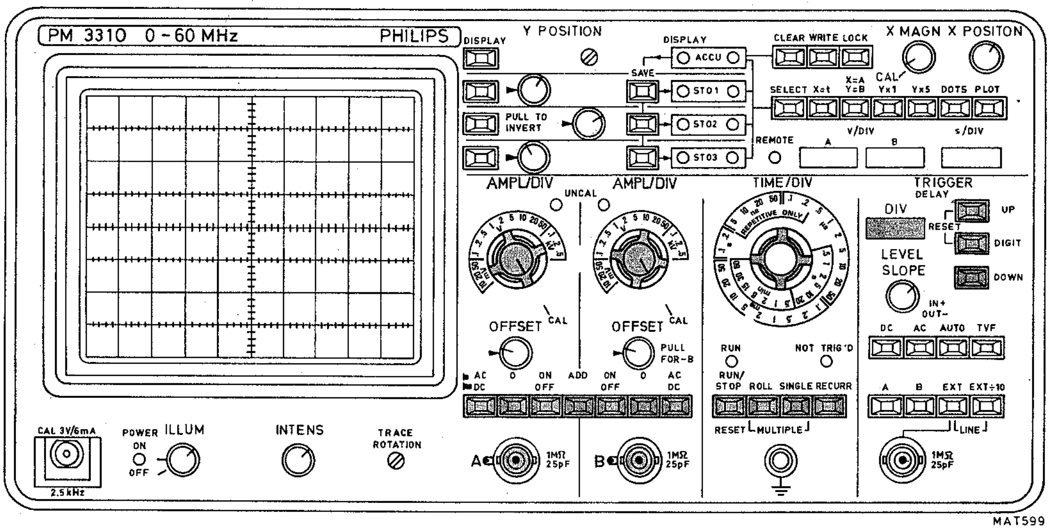
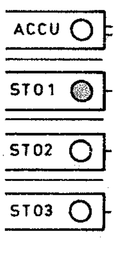


Fig. 3.10.

Si aucun des boutons-poussoirs DISPLAY n'est enfoncé, utiliser le bouton SELECT pour explorer:

- la trace d'écran
- les voyants
- les affichages de facteur d'échelle

le bouton-poussoir SELECT est également fonctionnel en mode PLOT (voir section 3.2.8. Modes d'affichage).



Ces voyants indiquent la mémoire spécifique à laquelle se rapportent les facteurs d'échelle et les réglages du retard de déclenchement en affichages V/DIV, s/DIV et DIV.

Un seul voyant est allumé au même moment.

3.3.8. Modes d'affichage

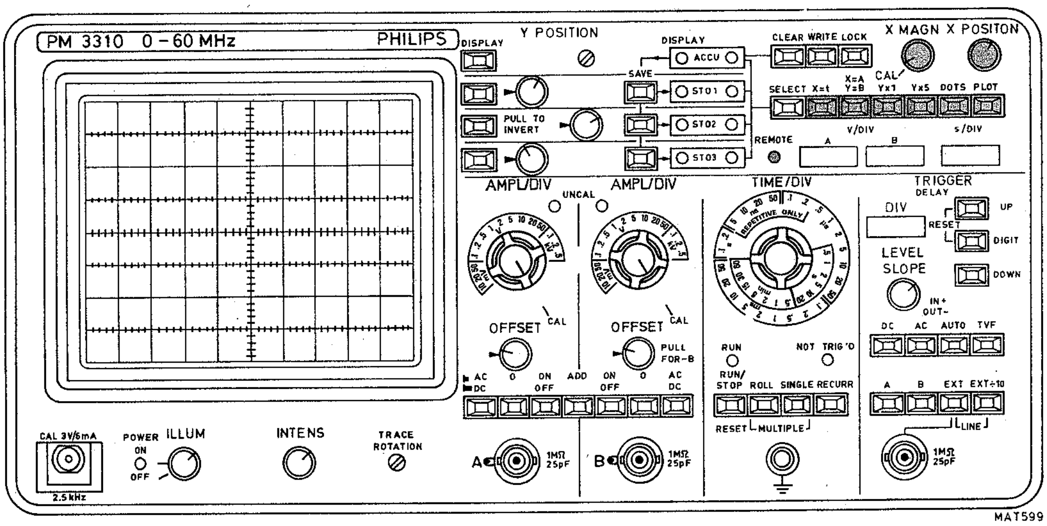
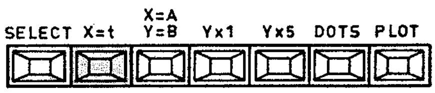
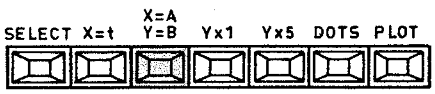


Fig. 3.11.

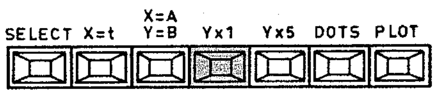


Affichage X = t dérivé du réglage original de base de temps (information de mémoire).

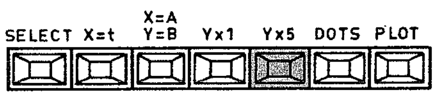


Affichage X/Y des entrées A et B.

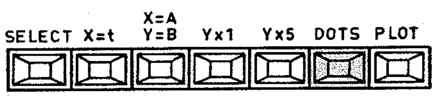
Les signaux A et B sont utilisés respectivement pour la déflexion horizontale et verticale.
Une image de 10 x 2 divisions est affichée.
Lorsque le mode Y x 5 est sélectionné, une image de 10 x 10 divisions peut être obtenue, dont 10 x 8 divisions sont affichables sur l'écran TRC.



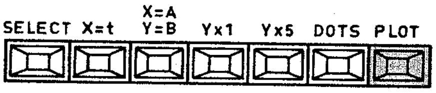
Coefficient de déflexion verticale x1.



Coefficient de déflexion verticale x5.
Dans ce mode, le facteur d'échelle en affichage V/DIV est également modifié (divisé par un facteur 5). Les mémoires affichées sont également visibles sur 10 divisions verticales. Les lignes zéro, si affichées correctement, se situent sur la même ligne de base.



Lorsque ce bouton est enfoncé, l'affichage normal (points reliés) fait place à un affichage à points discrets.



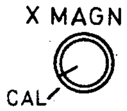
Lorsque le bouton PLOT est enfoncé, des signaux de sortie sont disponibles sur le panneau arrière pour le traçage sur enregistreur X/Y ou X(t). La mémoire contenant l'information à tracer peut être choisie à l'aide du bouton SELECT.

Pour le traçage en modes A et B, le traçage B est démarré après le traçage A. Un point intensifié sur l'affichage TRC indique la progression pendant le traçage.

Pour ce qui est des tensions de sortie X, Y et PEN LIFT, voir chapitre 3.3.9.
Pour permettre le positionnement manuel de la plume, il faut prévoir un retard de 3 secondes avant et de 6 secondes après le traçage. Le temps de traçage total est d'environ 100 sec.

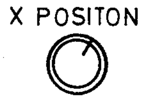
Lorsque le bouton PLOT est enfoncé une nouvelle fois, l'action PLOT (traçage) est arrêtée.

Remarque: Pour faciliter le fonctionnement, X = t et Y x 1 sont automatiquement sélectionnés lorsque tous les boutons sont relâchés.



Agrandisseur x 2,5 horizontal continu.

Remarque: Il n'y a pas d'agrandissement en position CAL et aucune indication dans l'affichage s/DIV.



Commande continue pour décalage horizontal de la trace sur l'écran.

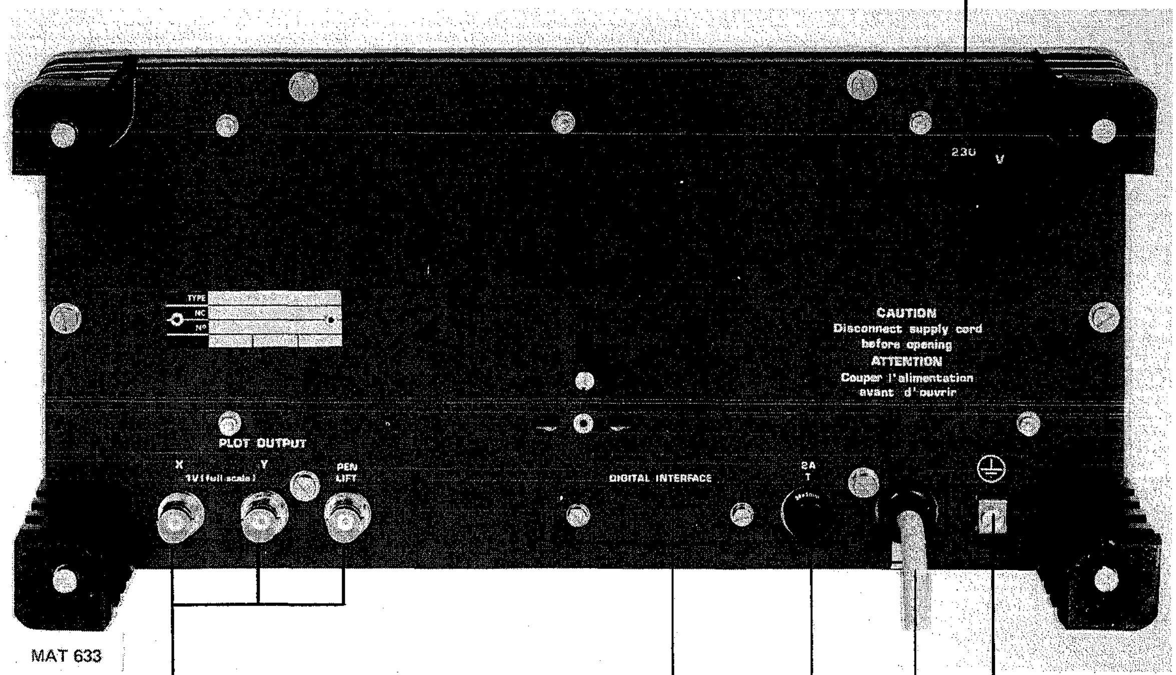
Témoin indiquant que IEC-bus surpasse tous les réglages de commande sur le panneau avant.

La remise en mode "local" ne peut être obtenu qu'à partir du contrôleur IEC-bus ou en déclenchant l'appareil pour le réenclencher ensuite.

Cette possibilité n'est fonctionnelle que dans les appareils pourvus d'une option IEC-bus PM 3325. Réglages et sorties peuvent être commandées à partir d'autres appareils externes à l'oscilloscope.
(Voir section appropriée de la notice d'entretien, instructions de montage et fonctionnement IEC-bus).

3.3.9. Panneau arrière

Adaptateur secteur sur 115 V (100 à 120 V ± 10 %)
Adaptateur secteur sur 230 V (220 à 240 V ± 10 %)



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Protection de terre

Cordon secteur

Porte-fusible secteur (fusible 2 A lent)

Interruption pour prise IEC-bus (fourni avec l'option IEC-bus PM 3325)

Sorties X-Y et PEN LIFT pour connexion d'un enrgistreur à l'oscilloscope.

- La sortie X fournit 1 V (pleine échelle), par ex. 0,1 V par division d'écran TRC.
- La sortie Y fournit 1 V (pleine échelle), par ex. 0,5 V par division d'écran TRC.
- La sortie PEN LIFT est une sortie de collecteur ouverte avec charge maxi $U_{0L} < 0{,}5$ V à 500 mA continu et commute sur zéro (TTL compatible).

Fig. 3.12.

3.4. DESCRIPTION DETAILLEE DES MANIPULATIONS

3.4.1. Généralités

Avant l'enclenchement s'assurer que l'oscilloscope est correctement installé conformément aux instructions de la section 2 et les précautions d'usage ont été observées.

Le procédé suivant donne une indication générale permettant de vérifier si l'oscilloscope fonctionne correctement. De plus, on trouve une routine de démarrage appropriée avant toute mesure.
Le procédé est spécialement utile pour les opérateurs qui ne connaissent pas ce type d'appareil.

Le présent appareil permet de stocker un signal de la voie A et un signal de la voie B (y compris AMPL/DIV et TIME/DIV, réglages du retard de déclenchement par rapport à ces signaux) dans une des quatre mémoires internes ACCU, STO 1, STO 2 ou STO 3 selon la sélection.

En mode normal (Y x 1) deux divisions sont disponibles pour chaque mémoire.
Avec les commandes POSITION en position médiane, l'affichage a lieu comme illustré ci-contre.

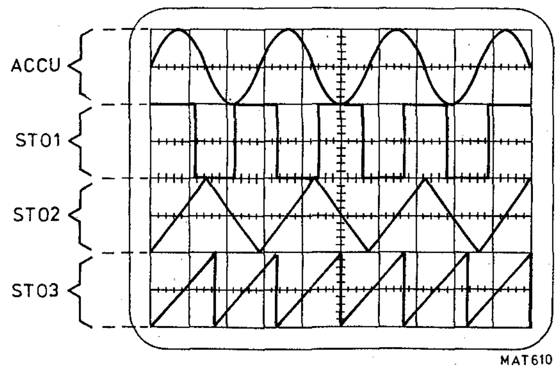


Fig. 3.13.

3.4.2. Affichage du contenu ACCU

Pour afficher le contenu de ACCU les réglages suivants sont nécessaires:
– Aucun signal d'entrée connecté.
– Tous les boutons poussoirs relâchés et tous les commutateurs en position CAL.

Les fonctions suivantes sont alors fonctionnelles

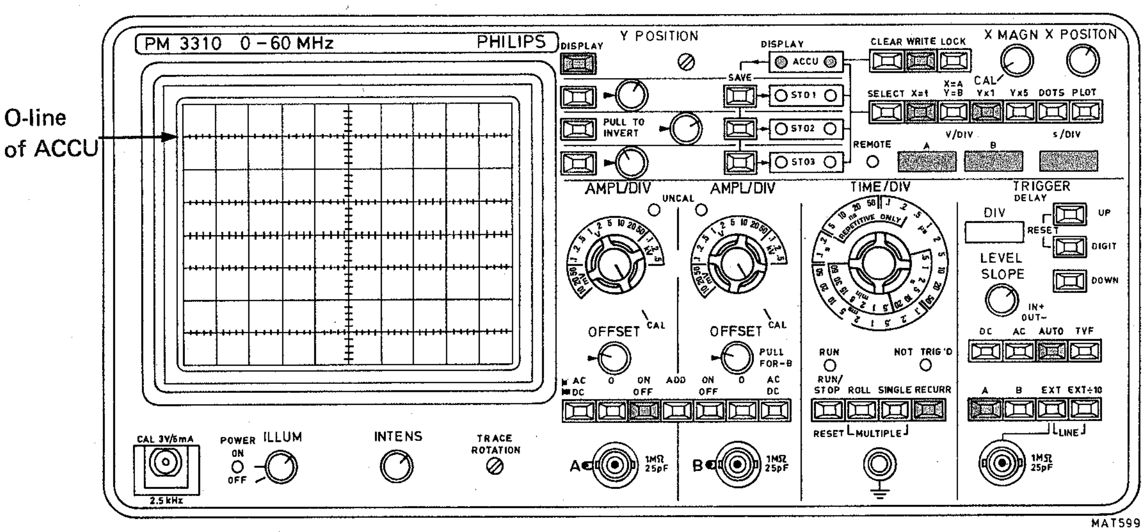


Fig. 3.14.

- Mettre le commutateur POWER en position ON. Vérifier si le voyant est allumé et que le test d'alimentation démarre (voir section 3.2.2.).
  Une trace apparaît alors adans les deux divisions supérieures de l'écran.
- Régler la commande INTENS afin d'obtenir une trace convenable.
- Ajuster la commande OFFSET de la voie A de sorte que la ligne de base affichée coïncide avec la ligne 0 de la section d'affichage ACCU.

L'oscilloscope est pret à accepter un signal d'entrée; cependant avant de poursuivre il est bon de pousser sur les boutons indiqués sur la figure "commandes".
Connecter un signal sinusoïdal à l'entrée A et régler le commutateur TIME/DIV en position appropriée.
L'affichage correct du signal d'entrée sur l'écran TRC peut être trouvé en tournant le bouton TIME/DIV de la position rapide en position lente (en partant de 0,5 ns/div) jusqu'à ce que le premier affichage déclenché soit obtenu.

Remarque 1: *Le commutateur AMPL/DIV de la voie doit être réglé de telle sorte que le signal d'entrée ne couvre pas plus de 2 divisions sur l'écran.*
Pour indiquer un dépassement ou un réglage OFFSET incorrect, le signal clignote jusqu'à ce que le réglage soit correct.

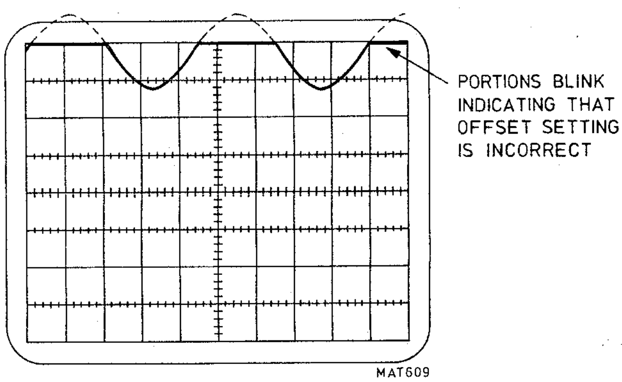


Fig. 3.15.

Remarque 2: *Pour obtenir un affichage total appuyer sur le bouton Y x 5.*
La ligne zéro est alors automatiquement située sur la ligne centrale de l'écran.

Remarque 3: *Si les deux voies A et B sont en service et que des signaux d'entrée sont connectés aux deux voies, les traces seront superposées.*

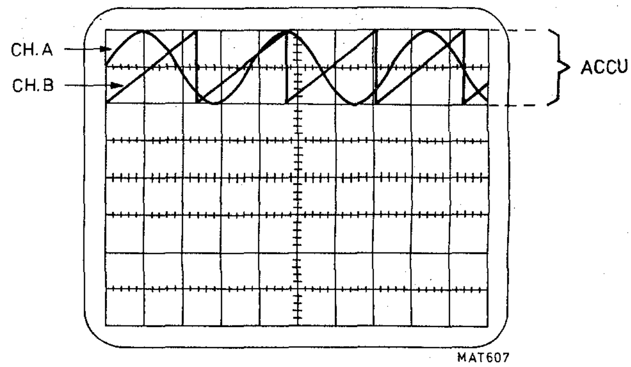


Fig. 3.16

Dans ce cas il est possible de régler le commutateur AMPL/DIV et les commandes OFFSET des voies A et B de telle sorte que chaque trace occupe une division en mode normal (Y x 1).

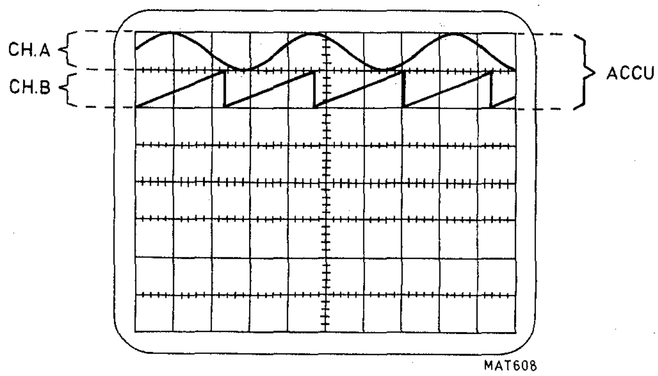


Fig. 3.17.

Remarque 4: *Si un autre bouton DISPLAY ou plus sont enfoncés, deux situations sont possibles:*

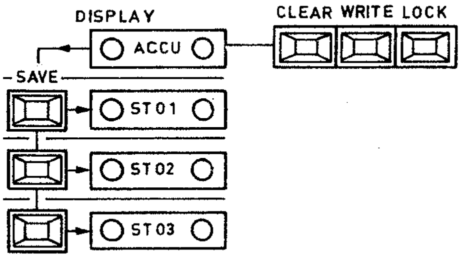
1. *En cas d'assistance batterie, le contenu de la mémoire (ou des mémoires) associée(s) est affiché; par exemple contenu de mémoire précédent la mise hors service de l'appareil.*
2. *Sans assistance batterie, le TRC affiche une information incorrecte et l'affichage alphanumérique indiquera:*

V/DIV A	V/DIV B	s/DIV
NOP	NOP	NOP

DIV
NOP

3.4.3. Stockage de contenu ACCU

Le présent paragraphe décrit le procédé de stockage du contenu ACCU dans une des mémoires STO 1, STO 2 ou STO 3, lesquelles sont seules capables de recevoir ledit contenu.



- Enfoncer le bouton SAVE de la mémoire choisie pour le stockage de l'information ACCU.
- Vérifier si l'information est écrite en mémoire en enfonçant le bouton DISPLAY de cette mémoire.

  Le contenu sera alors affiché sur l'écran TRC.

Une mémoire peut être effacée (seulement en mode WRITE) en effaçant ACCU à l'aide du bouton CLEAR et en stockant le contenu ACCU effacé dans cette mémoire, en actionnant le bouton SAVE correspondant.
En autres mots l'effacement de mémoire a lieu en stockant le contenu ACCU vide.

3.4.4. Usage du bouton SELECT

Les fonctions du bouton SELECT sont les suivantes:

a. Sélectionner la mémoire contenant les réglages V/DIV, s/DIV et DIV (retard) à indiquer.
b. Sélectionner la mémoire contenant les informations à tracer.
c. Si aucun bouton DISPLAY n'est enfoncé, SELECT commence à explorer les mémoires affichées les voyants et les réglages V/DIV, s/DIV et DIV (retard).

Remarque: – *Si un seul bouton DISPLAY est enfoncé, l'actionnement de SELECT n'a aucun effet visible.*
– *Si deux boutons DISPLAY ou plus sont enfoncés, l'actionnement de SELECT signifie l'exploration par le système des voyants et des informations dans les indicateurs V/DIV, s/DIV et DIV (retard).*

Le bouton LOCK permet de garder le contenu inchangé de mémoire.

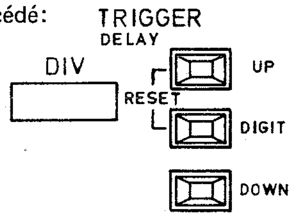
3.4.5. Retard de déclenchement

a. Retard positif

Le retard de déclenchement permet de choisir (en divisions) le temps qui s'écoule entre le déclenchement et le démarrage de l'affichage TRC (à gauche).

EXEMPLE: A supposer que la 6ème ligne d'une mire de télévision soit requise (ligne de télévision = 64 μs). Dans ce cas le retard de déclenchement est de 5 x 64 μs = 320 μs, lorsque la 5ème ligne est dépassée.

Procédé:



- Sélectionner TVF.
- Régler le commutateur TIME/DIV sur 10 μs/DIV.
- Enfoncer UP jusqu'à ce que le chiffre le moins significatif affiche 2
- Enfoncer une fois DIGIT.
- Enfonder UP jusqu'à ce que le deuxième chiffre affiche 3

Un retard de 32 x 10 μs entre l'impulsion de trame et le côté gauche de l'affichage TRC est obtenu.
Ceci résulte en l'affichage de l'information de la 6ème ligne.

b. Retard négativ

Tandis que l'oscilloscope emmagasine continuellement des informations dans le registre de décalage, il permet aussi de réaliser un pré-déclenchement.
En effet une portion du signal précédent le point de déclenchement peut être affichée sur le TRC. Le point de déclenchement peut être choisi sur chaque division de l'écran TRC (0 à 9 divisions).

Si le commutateur TIME/DIV est mis sur une autre position, le réglage du retard de déclenchement (en division) sera automatiquement modifié (recalculé) et affiché. Le résultat de ce calcul est arrondi vers le bas sur division entière (intègre).
Le point de démarrage de ce calcul est le nombre de divisions affichées à un certain moment.

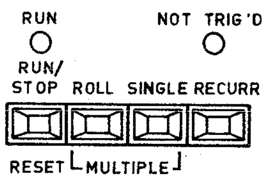
Remarque 1: Le retard de déclenchement préréglé pour une certaine position du commutateur TIME/DIV est stocké à l'intérieur et représente toujours le même retard indépendamment des erreurs d'arrondissement dues à l'actionnement du commutateur TIME/DIV pendant l'opération de calcul.

		premier exemple				deuxième exemple			
	TIME/DIV		DIV		DIV		DIV		DIV
position réglée ⟶	5 µs		0095		0095		0095		0095
		1		12		1		10	
	10 µs		0047		0000		0047		0040
		2		11		2		9	
	20 µs		0023		0000		0023		0020
		3		10		3		8	
	50 µs		0009		0000		0009		0008
		4		9		4		7	
	. 1 ms		0004		0000		0004		0004
		5		8		5		6	
	. 2 ms		0002		0000		0002		0002
		6		7					
	. 5 ms		0000		0000				
			réglage vers le bas		réglage vers le haut		réglage vers le bas		réglage vers le haut

Remarque 2: Si à l'actionnement du commutateur TIME/DIV un retard de déclenchement nulle est atteint, toutes les positions inférieures afficheront un retard de déclenchement (0).
Un retard de déclenchement est mis hors service en mode ROLL, l'indicateur DIV affichant alors OFF.

3.4.6. Modes simple et multiple

Lorsque le bouton SINGLE est enfoncé, ACCU est rafraîchie après une impulsion de déclenchement et un retard tout comme l'affichage, ACCU
Si l'appareil attend une impulsion de déclenchement, le voyant NOT TRIG'D s'allume.



Lorsque les deux boutons ROLL et SINGLE sont enfoncés, l'action SINGLE est répétée 4 fois. On appelle ceci le mode MULTIPLE. Le résultat de la première action est stocké dans la mémoire STO 3, le deuxième résultat en STO 2, le troisième en STO 1 et le quatrième en ACCU.
Si soit l'action SINGLE soit l'action MULTIPLE est achevée, le même mode peut être sélectionné une nouvelle fois en enfonçant le bouton RESET.

3.4.7. Mode ROLL

Le mode ROLL sert surtout pour des signaux à très basse fréquence et est fonctionnel pour des réglages TIME/DIV de 0,5 s à 60 min.
Le signal est formé point par point à partir du côté droit de l'écran TRC et s'écrit vers la gauche. Si 10 divisions de l'écran sont formées dans la mémoire ACCU, l'action SAVE est démarrée automatiquement, de sorte que le contenu ACCU est conservé dans la mémoire STO 3.
L'action en mode ROLL peut être démarrée en sélectionnant ROLL et en appuyant une fois sur le bouton RUN/STOP.

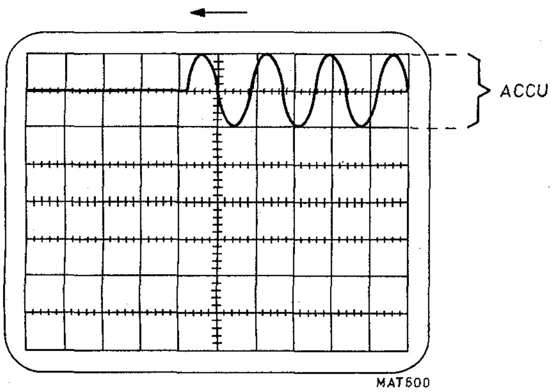


Fig. 3.18. Formation de l'information première dans la mémoire ACCU

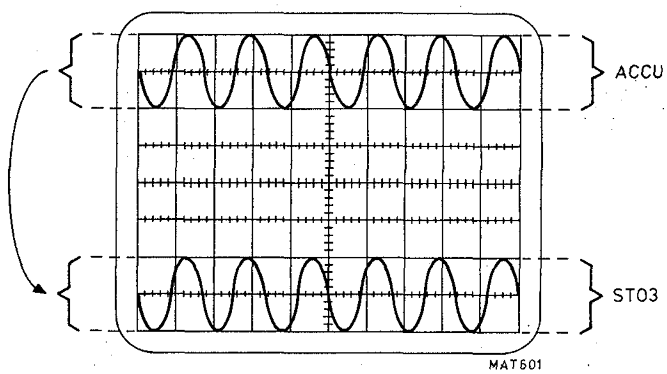


Fig. 3.19. Première action SAVE

La nouvelle information est constituée point par point dans la mémoire ACCU et après accomplissement (10 divisions), la nouvelle information est stockée dans la mémoire STO 2.

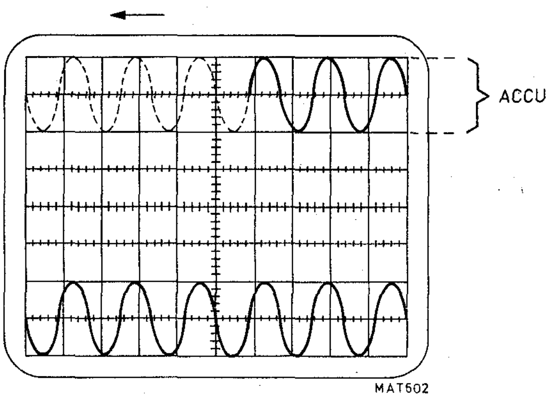


Fig. 3.20. Formation de l'information seconde dans la mémoire ACCU

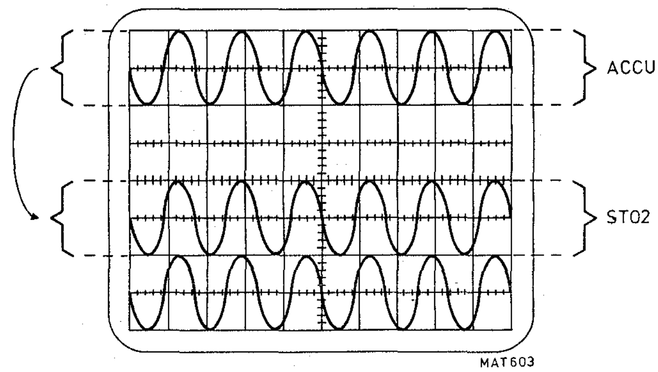


Fig. 3.21. Deuxième action SAVE

La troisième information constituée dans ACCU est stockée dans la mémoire STO 1 comme illustré ci-après.

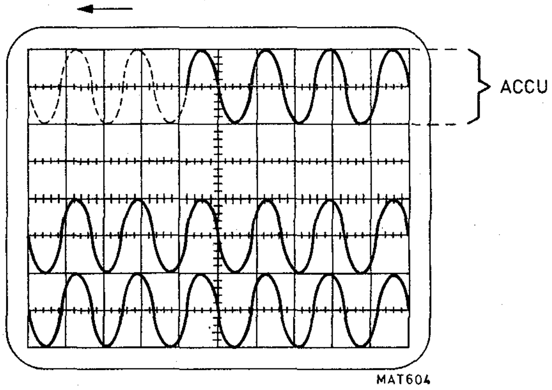


Fig. 3.22. Formation de l'information troisième dans la memoire ACCU

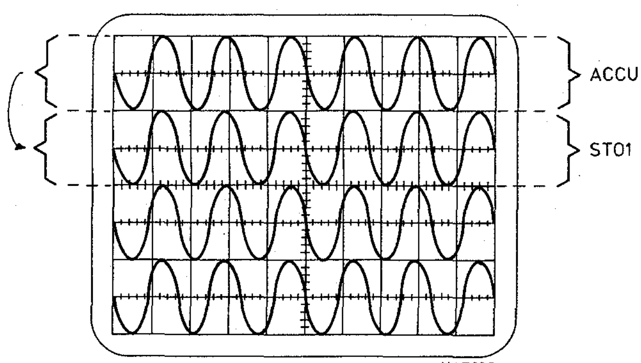


Fig. 3.23. Troisième action SAVE

La dernière information est stockée dans la memoire ACCU comme illustré ci-dessous

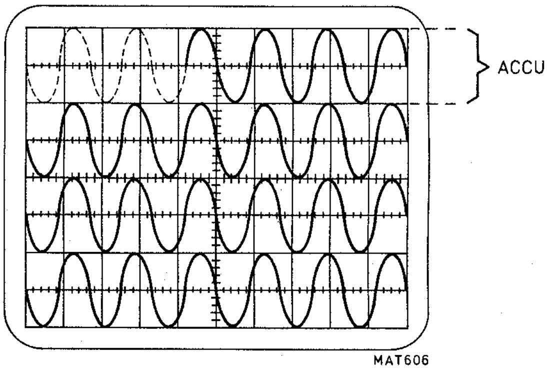


Fig. 3.24.

En mode ROLL, l'indicateur RUN est allumé continuellement et après l'action il clignote. Si en mode ROLL une interruption est nécessaire, enfoncer le bouton RUN/STOP. Le mode ROLL est interrompu et l'indicateur RUN éteint. Cette action peut également être réalisée par un signal continu externe à niveau TTL, à condition que le mode ROLL soit arrêté en actionnant le bouton RUN/STOP.

TTL = 1 $\rightarrow$ RUN TTL = 0 $\rightarrow$ STOP

Si l'on enfonce le bouton RUN/STOP une nouvelle fois, l'action en mode ROLL est poursuivie. A la fin de cette action (RUN clignote), une nouvelle action peut être redémarrée en appuyant sur le bouton CLEAR et ensuite sur le bouton RUN/STOP.

3.4.8. Traçage

- Connecter les sorties X, Y et PEN LIFT de l'oscilloscope à l'enregistreur.
  La sortie X produit 0,1 V par division TRC (1 V par pleine échelle).
  La sortie Y produit 0,5 V par division TRC (1 V par pleine échelle).
  La sortie PEN LIFT est une tension de collecteur ouverte avec charge maximale de 500 mA continu permettant de mettre la sortie à zéro; il est TTL compatible.
- Enfoncer le bouton SELECT afin de sélectionner la mémoire contenant l'information à tracer.
- Enfoncer le bouton PLOT pour démarrer le traçage; ceci est visible sur l'écran TRC par un point intensifié se déplaçant de gauche à droite sur la trace sélectionnée.
  Le traçage peut être interrompu en appuyant une nouvelle fois sur le bouton PLOT.

Si le levage automatique de plume n'est pas disponible, le mouvement vertical de plume manuel a lieu comme suit:

- Enfoncer PLOT.
- Attendre 2 secondes.
- Pousser la plume vers le bas (au bout d'une seconde le traçage démarrera).
- Après traçage du signal, relever la plume.
- En fonctionnement double voie, la plume commence, au bout de 6 secondes, à se déplacer vers le point de démarrage de la deuxième voie.
- Pousser la plume vers le bas.
- Après traçage de la deuxième voie, relever la plume.

Remarque 1: *Pendant le traçage l'oscilloscope est en mode bloqué (LOCK), ce qui signifie que le contenu des mémoires ne peut être modifié.*

Remarque 2: *En cas de traçage des voies A et B, la voie A sera d'abord tracée et ensuite la voie B.*

Remarque 3: *Le traçage est pourvu d'un retard de 3 secondes en début et en fin d'action, permettant d'économiser un temps suffisant nécessaire au positionnement de la plume.*

3.4.9. Réglage des sondes atténuatrices

- Connecter la boîte de compensation à la prise A et appliquer la pointe de sonde à la prise CAL.
- Enfonder Y x 5.
- Sélectionner un réglage approprié du commutateur AMPL/DIV de la voie A.
- Introduire un petit tournevis par le trou dans la boîte de compensation et ajuster le trimmer pour obtenir un affichage correct comme illustré à la figure 3.25.

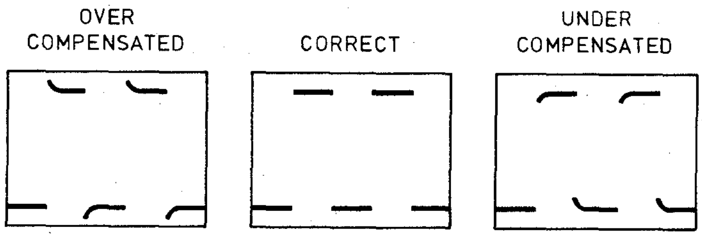


Fig. 3.25. MAT 635

3.4.10. Mode différentiel

On peut choisir le mode A – B en enfonçant ADD et en tirant la commande POSITION de la voie B.
Dans les mesures au cours desquelles il y a réception de signaux de mode commun de valeur appréciable (par exemple ronflement), le mode différentiel annule ces signaux pour ne conserver que la valeur intéressante (A – B). La capacité de l'oscilloscope à supprimer les signaux de mode commun est donnée par le coefficient de réjection mode commum (CMR) (voir figure 3.26).
Pour obtenir le degré spécifié de réjection mode commun, il faut tout d'abord égaliser les gains respectifs des voies A et B. On peut obtenir ce résultat en connectant les deux voies au connecteur CAL et en ajustant l'un des commutateurs AMPL/DIV pour une déviation minimale sur l'écran.
Si l'on emploie des sondes passives 10 : 1, il est recommandé d'employer une méthode d'égalisation similaire consistant à régler leurs commandes de compensation pour une déviation minimale.

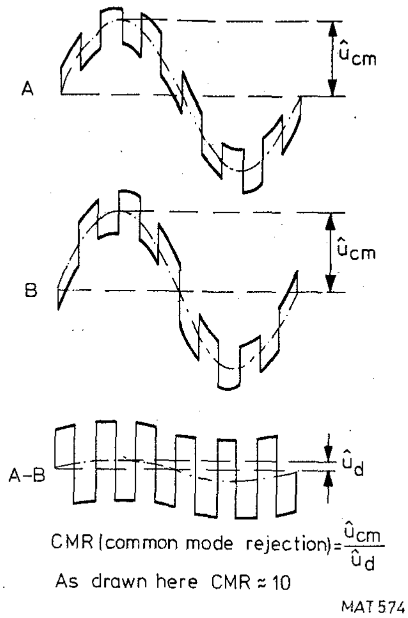


Fig. 3.26. Réjection en mode commun

3.4.11. X = A et Y = B

Dans ce mode, le signal est formé point par point. Le circuit continu "points reliés" est automatiquement mis hors service.

Procédé:

- Connecter des signaux d'entrée aux prises d'entrée pour les voies A et B.
- Régler les commutateurs AMPL/DIV en position appropriée.
- Enfoncer X = t et régler le commutateur TIME/DIV de telle sorte qu'au moins une période soit affichée sur le TRC.
- Enfoncer X = A.
  Y = B.

La déflexion horizontale est alors déterminée par l'entrée de voie A et la déflexion verticale par l'entrée de voie B.

4. METHODE DE CONTROLE

4.1. GENERALITES

Le présent contrôle permet de vérifier l'oscilloscope en un minimum de points et de tests. L'opérateur est supposé bien connaître les oscilloscopes et leur caractéristiques.

ATTENTION: Avant la mise en service, s'assurer que l'oscilloscope est installée conformément aux instructions mentionnées au chapitre 2.

Si ce test est démarré quelques minutes après la mise en service, ne pas oublier que des tests peuvent ne pas répondre aux caractéristiques à la suite du temps de réchauffage trop court. Pour assurer un test adéquat, attendre le temps de chauffage spécifié.

Le test doit être effectué à une température ambiante de 20 à 30 °C.

Tous les contrôles peuvent être réalisés sans déposer les couvercles supérieur et de fond de l'appareil.

Pour obtenir un contrôle totale des étalonnages dans chaque partie de l'appareil, se référer la section "Checking and Adjusting Procedure" et omettre les étapes d'ajustage.

4.2. REGLAGES PRELIMINAIRES DES COMMANDES

- Démarrer la présent procédé avec aucun signal d'entrée connecté et tous les boutons relâchés et tous les commutateurs en position CAL.
- Enfoncer les boutons comme indiqué ci-dessous sur la figure

O-line of ACCU

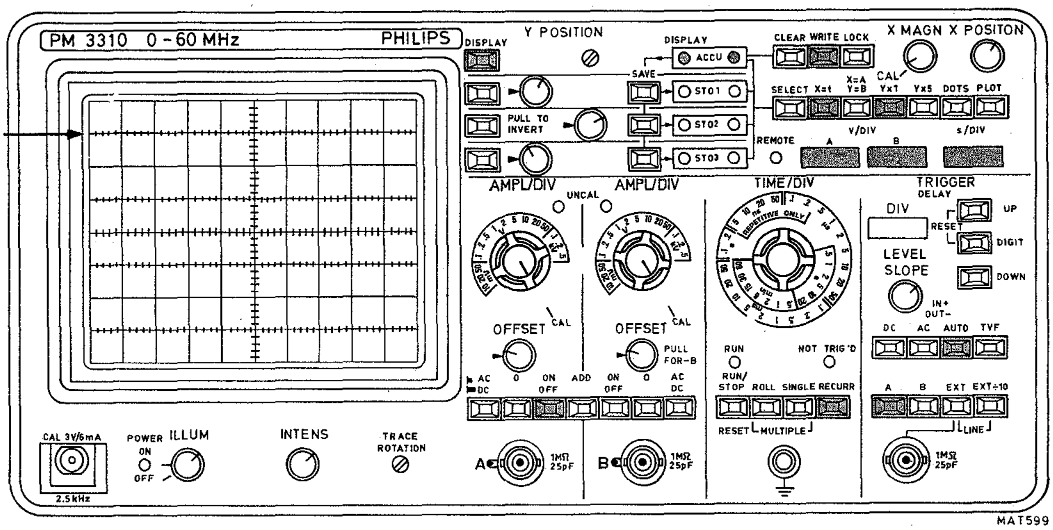


Fig. 3.27.

A moins qu'indiqué différemment, les commandes occupent toujours les mêmes positions que pour le contrôle précédent.

4.3. PROCEDE DE CONTROLE

Section TRC

- Mettre le commutateur POWER en position ON. Vérifier si le témoin s'allume et si le test d'alimentation démarre conformément au chapitre 3.3.2.
- Après le pré-chauffage, l'affichage TRC indiquera la base de temps contenu en mémoire ACCU.
- Vérifier l'illumination d'écran en tournant la commande ILLUM.
- Régler la commande INTENS afin d'obtenir une intensité d'affichage appropriée.
- Une ligne horizontale apparaît au centre des deux divisions supérieures de l'affichage TRC tant que le bouton CLEAR est enfoncé.

Section verticale

- Régler le commutateur AMPL/DIV en position 5 V/DIV.
- Régler le commutateur TIME/DIV en position 0,2 ms/DIV.
- Vérifier si la ligne affichée est exactement parallèle aux lignes de graticule horizontales. (La correction est possible à l'aide du réglage par tournevis TRACE ROTATION sur le panneau avant).
- Tourner la commande OFFSET vers la droite et vérifier si la trace brille au sommet de l'écran. Lorsque cette commande est tournée vers la gauche, la ligne inférieure de l'affichage ACCU brille.
- Régler la commande OFFSET de sorte que la ligne de base soit décalée vers le centre des deux divisions supérieures.
- Connecter le signal de sortie de la borne CAL à la prise d'entrée.
  Vérifier si chaque période couvre 2 divisions dans le sens horizontal et si l'amplitude est de 0,6 divisions dans le sens vertical.
- Enfoncer le bouton de couplage d'entrée AC/DC sur AC et vérifier si le signal est symétrique par rapport à la ligne centrale des deux divisions supérieures.
- Relâcher le commutateur en position DC.
- Enfoncer le commutateur 0. Une ligne de base apparaît sur la ligne centrale des deux divisions supérieures.
- Relâcher le commutateur 0.
- Vérifier si la gamme de la commande continue AMPL/DIV présente une atténuation de 2,5 fois ou plus.
- Si la commande continue AMPL/DIV n'est plus étalonnée, le témoin UNCAL s'allume et un astérisque apparaît sur l'affichage V/DIV.
  Régler la commande continue en position CAL.
- Vérifier si toutes les positions du commutateur AMPL/DIV sont affichées sur l'affichage V/DIV et passer ensuite en mode 5 V/DIV.
- Le précédent contrôle peut dès lors être réalisé sur l'autre voie.
- Appuyer le commutateur ON/OFF de la voie B en position ON.
- Régler les commutateurs d'entrée (voies A et B) en position AC.
- Connecter le signal CAL aux entrées des voies A et B.
  Ajuster les commandes OFFSET de sorte que les traces se chevauchent.
- Pousser ADD et vérifier si le signal affiché est doublé par rapport à l'amplitude.
- Actionner le commutateur PULL FOR –B et vérifier si une amplitude de signal minimale est affichée.
- Régler les deux commutateurs de couplage d'entrée sur DC et relâcher ADD.
- Relâcher le commutateur ON/OFF de la voie B en position OFF.
- Repousser la commande OFFSET pour obtenir le mode normal.
- Déconnecter le signal d'entrée B.

Section affichage

- Enfoncer les quatre boutons-poussoirs DISPLAY et vérifier si les témoins DISPLAY s'allument.
- Enfoncer le bouton CLEAR et vérifier si la partie d'affichage ACCU et donc le contenu de mémoire ACCU sont effacés.
- Vérifier si les mémoires STO 1, STO 2 et STO 3 sont également effacées en enfonçant simultanément le bouton CLEAR et le bouton SAVE requis.
- Vérifier s'il y a quatre traces sur l'écran (par ex. le signal d'entrée et les trois lignes de base de STO 1, STO 2 et STO 3) et si les trois lignes de base peuvent être décalées en sens vertical en tournant le commande Y POSITION.
  Ajuster les commandes Y POSITION de sorte que les traces se situent sur leurs lignes de base.
- Vérifier si le contenu de mémoire ACCU peut être stocké dans les mémoires STO 1, STO 2 ou STO 3 en enfonçant les boutons-poussoirs SAVE correspondants.
- Vérifier si les traces STO 1, STO 2 et STO 3 peuvent être inversées en tirant sur les commandes Y POSITION.
- Pousser les commandes Y POSITION.
- Enfoncer LOCK et vérifier si le contenu de mémoire n'est pas influencé jusqu'à l'actionnement du bouton WRITE.

Modes d'affichage

- Tourner la commande X MAGN complètement vers la droite.
- Vérifier si l'affichage agrandi peut être décalé entièrement à l'aide de la commande X POSITION.
- Enfoncer le bouton DOTS et vérifier si des points séparés sont visibles sur l'écran.
- Mettre X MAGN sur CAL; relâcher DOTS et régler X POSITION en vue d'aun affichage correct.

Régler TIME/DIV sur	Appuyer sur SAVE de	ACCU	Appuyer sur SELECT de	Lire en s/DIV
1 ms/div	STO 1		STO 1	1 - 3
.5 ms/div	STO 2		STO 2	.5 - 3
.2 ms/div	STO 3		STO 3	.2 - 3
.1 ms/div		ACCU	ACCU	.1 - 3

- Relâcher les boutons STO 1, STO 2 et STO 3 DISPLAY.
- Enfoncer le commutateur de couplage d'entrée en position AC.
- Vérifier si, en poussant sur Y x 5, l'affichage sur l'écran tout entier est possible et si la ligne zéro se situe au centre de l'écran.
- Pousser Y x 1.
- Enfoncer PLOT et vérifier si un point intensifié apparaît à gauche sur l'écran. Ce point suivra la trace au bout de quelques secondes. Au besoin, vérifier les sorties d'enregistreur à l'arrière (1 V pleine échelle).

Section horizontale

- Enfoncer SINGLE.
  Chaque fois que le bouton RESET est enfoncé, le contenu de la mémoire ACCU est rafraîchi et affiché.
- Enfoncer les boutons STO 1, STO 2 et STO 3 DISPLAY.
- Enfoncer MULTIPLE (ROLL et SINGLE) et vérifier si l'action SINGLE est répétée quatre fois (dans les quatre mémoires ACCU, STO 1, STO 2 et STO 3).
- Enfoncer ROLL et appliquer un signal de 1 Hz à la prise d'entrée; mettre AMPL/DIV en position adéquate.
- Régler TIME/DIV sur .5 s/DIV.
- Enfoncer RUN et vérifier si le signal est stocké comme décrit au chapitre 3.4.7.
- Vérifier si le témoin RUN est allumé en permanence après l'exploration ROLL et clignote lorsque l'action RUN est achevée.
- Déconnecter le signal d'entrée et enfoncer RECURR.
- Vérifier si toutes les positions du commutateur TIME/DIV sont affichées correctement dans l'affichage s/DIV et régler le commutateur TIME/DIV sur .2 ms/DIV.
- Connecter la sortie CAL à la prise d'entrée.

Retard de déclenchement

- Vérifier si, en enfonçant UP une fois, la trace est décalée d'une division vers la gauche.
  Vérifier si, en enfonçant DOWN une fois, la trace est décalée en position originale.
- Enfoncer DIGIT. Vérifier si le chiffre suivant dans l'affichage DIV clignote et peut être changé enfonçant UP ou DOWN.
  Si l'on enfonce DOWN, l'affichage ne sera jamais inférieur à –9.
- Vérifier si l'affichage DIV indique 0 en enfonçant RESET (simultanément UP et DOWN).

5. ENTRETIEN PREVENTIF

5.1. GENERALITES

Le présent appareil ne requiert en principe aucune maintenance, car il ne contient pas de composants sujets à l'usure. Cependant, pour garantir le fonctionnement fiable et sans défaillances, l'appareil ne doit pas être exposé à l'humidité, le chaleur, des éléments corrosifs ou la poussière excessive.

5.2. NETTOYAGE DU REVETEMENT SUEDE NEXTEL

ATTENTION: Le revêtement suède NEXTEL résistance à l'éthanol, pas à l'alcool à brûler: la décomposition d'une des substances endommagerait le revêtement NEXTEL de façon irréparable.

Au bout d'un certain temps, le revêtement suède NEXTEL perd de son éclat. Un nettoyage régulier de la surface à l'aide d'un chiffon humide (eau, éthanol ou autre détergent) ne donnera pas le résultat escompté. La surface frottée par un chiffon sera nettoyée, non les granulations et les griffes.

3M-COMPANY a développé une nouvelle méthode de nettoyage permettant le nettoyage des granulations. L'éponge no. 8840 de 3M doit être trempée dans l'eau, l'éthanol ou un détergent courant. Il s'agit d'un chiffon ayant les mêmes propriétés que les éponges ou les chiffons abrasifs: il nettoie les surfaces et leur redonne l'éclat sans toutefois les griffer.

5.3. DEPOSE DE LA VISIERE ET DE LA PLAQUE DE CONTRASTE

- Prendre les coins inférieurs de la visière et la déposer du panneau avant par légére traction (Fig. 3.28).
- Le filtre contraste est facilement démontable hors de la visière par légère pression.
- Le filtre est sensible à la striation. S'assurer donc qu'un chiffon doux (sans poussière, ni matériel dur) soit utilisé au nettoyage.

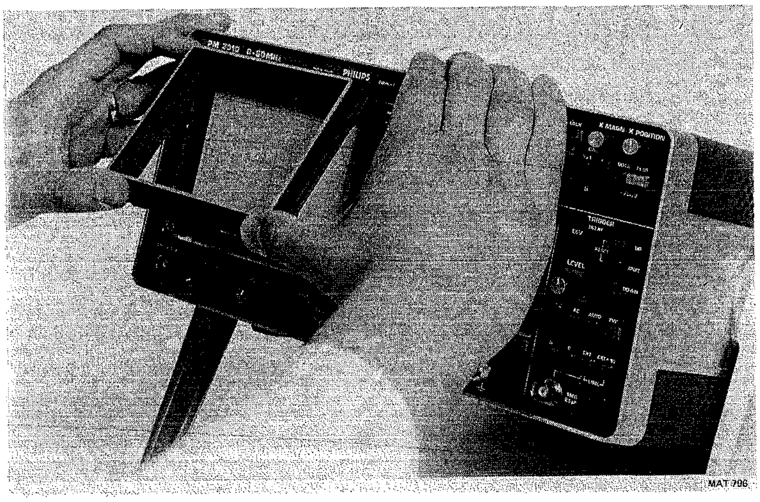


Fig. 3.28.

5.4. RE-ETALONNAGE

La pratique a prouvé que l'oscilloscope fonctionne dans les limites spécifiés pendant une période de 1000 heures de travail ou de 6 mois en cas d'usage irrégulier.
De plus, le remplacement de composants peut nécessiter un ré-étalonnage des circuits affectés. Les procédés de contrôle et d'ajustage peuvent également servir à détecter certaines fautes dans l'appareil.
Dans certains cas, des troubles mineurs peuvent être localisés et/ou corrigés par le ré-étalonnage. Les instructions complètes de contrôle et d'ajustage sont mentionnées au chapitre "Contrôles et réglages". Si un étalonnage partiel est requis, il suffit de consulter la carte "Adjustment interactions".

CONTENTS

6. CIRCUIT DESCRIPTIONS

6.1. BLOCK DIAGRAM DESCRIPTION

This chapter serves to explain the main functions of the oscilloscope. The working principle is divided into four sections:

6.1.1. Acquisition system
6.1.2. Display system
6.1.3. Microprocessor and software
6.1.4. Power supply

6.1.1. Acquisition system

By means of the acquisition system the analog input signals are converted into digital information.
Before conversion the analog signals must be adapted so that an Analog to Digital Converter (ADC) is able to convert them. This system can be divided into the following sections:

6.1.1.1. The vertical channels
6.1.1.2. The analog-to-digital convertor (including P^2CCD)
6.1.1.3. Trigger and trigger delay circuits
6.1.1.4. The sampling system
6.1.1.5. The time base system
6.1.1.6. The acquisition control

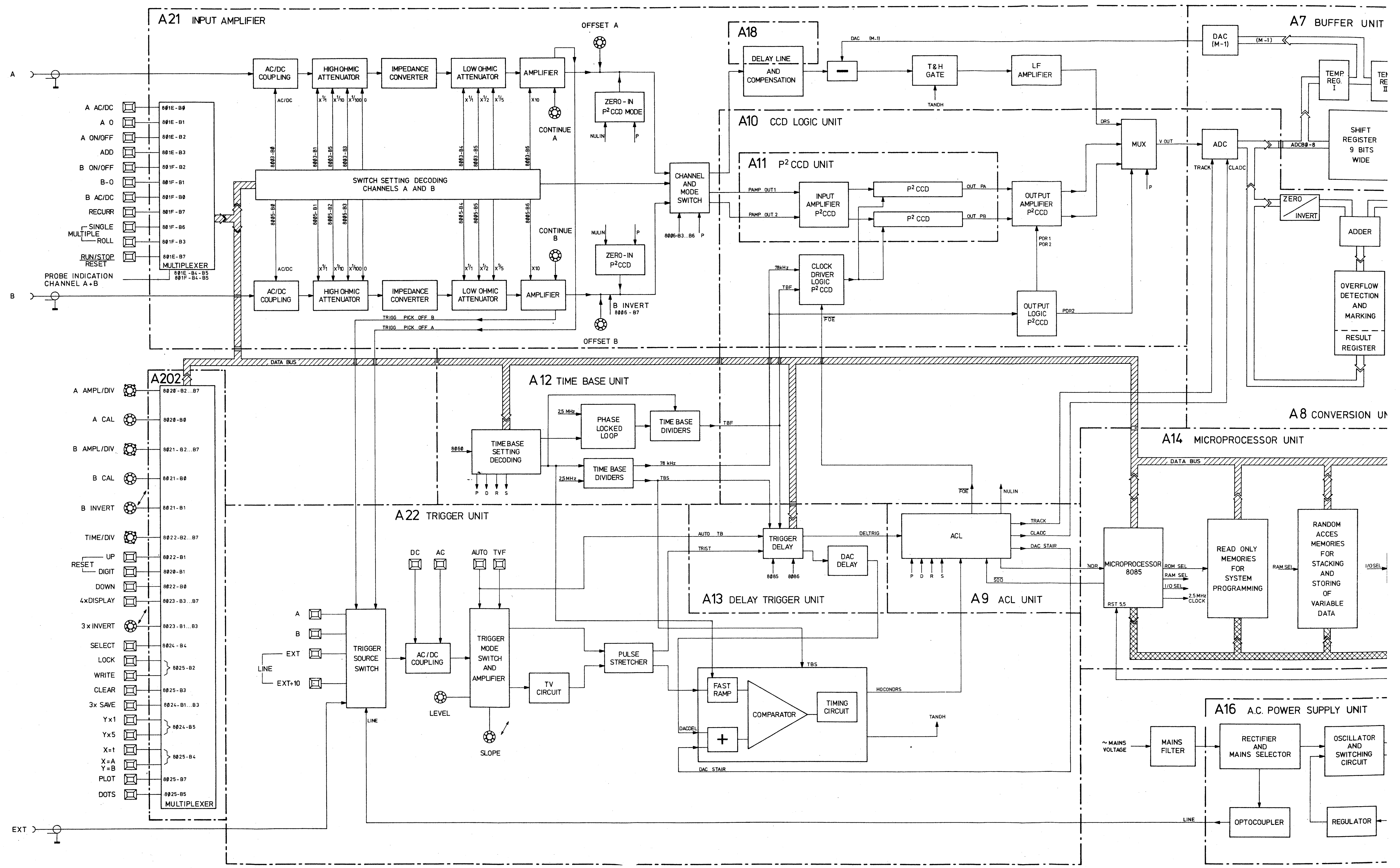
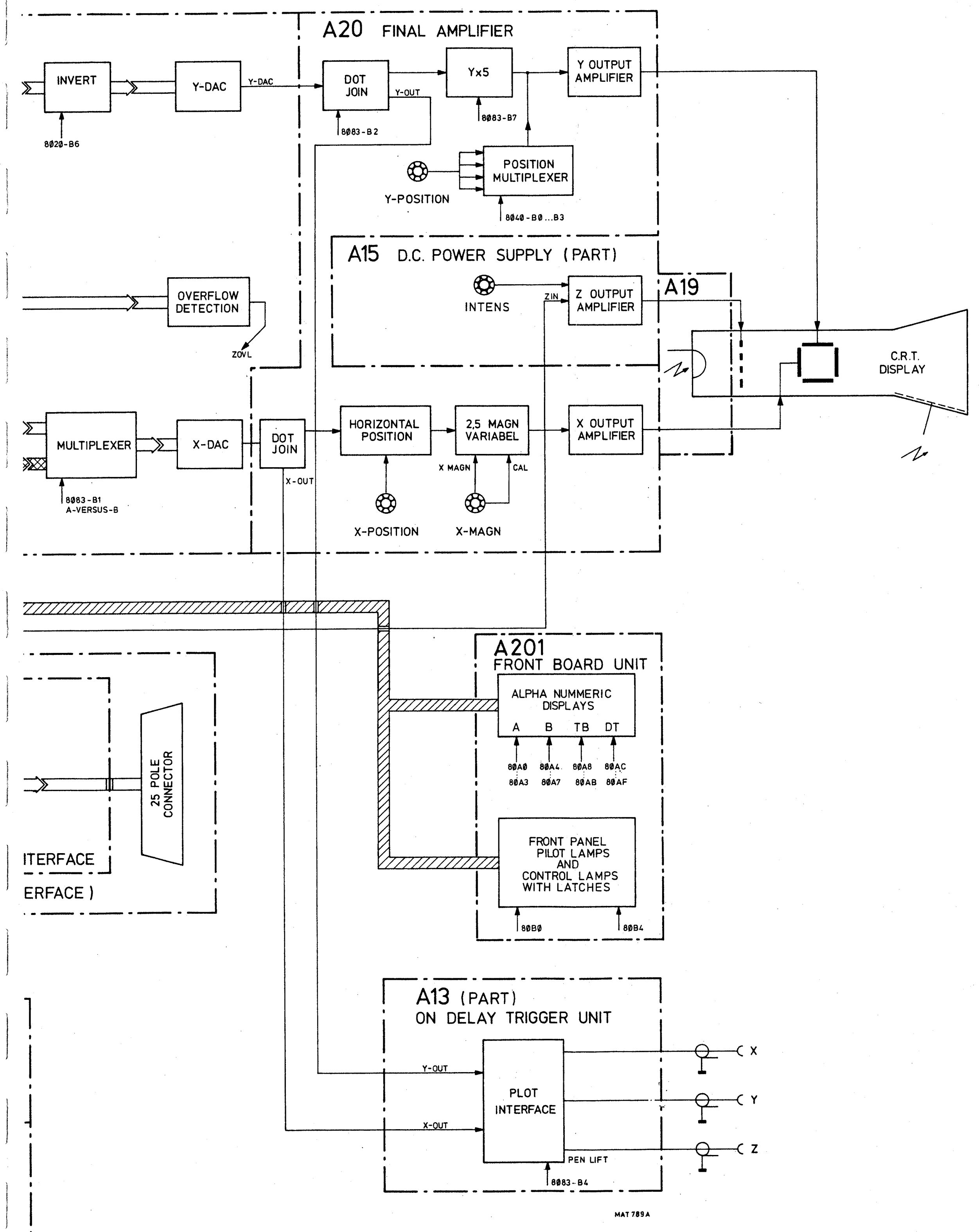

A21 INPUT AMPLIFIER
A18
A7 BUFFER UNIT
A10 CCD LOGIC UNIT
A11 P²CCD UNIT
A202
A12 TIME BASE UNIT
A8 CONVERSION UN
A14 MICROPROCESSOR UNIT
A22 TRIGGER UNIT
A13 DELAY TRIGGER UNIT
A9 ACL UNIT
A16 A.C. POWER SUPPLY UNIT
AC/DC COUPLING
HIGH OHMIC ATTENUATOR
IMPEDANCE CONVERTER
LOW OHMIC ATTENUATOR
AMPLIFIER
OFFSET A
OFFSET B
ZERO-IN P²CCD MODE
ZERO-IN P²CCD
CONTINUE A
CONTINUE B
B INVERT
SWITCH SETTING DECODING CHANNELS A AND B
CHANNEL AND MODE SWITCH
DELAY LINE AND COMPENSATION
T&H GATE
LF AMPLIFIER
DAC (M-1)
TEMP REG. I
MUX
ADC
SHIFT REGISTER 9 BITS WIDE
ZERO INVERT
ADDER
OVERFLOW DETECTION AND MARKING
RESULT REGISTER
INPUT AMPLIFIER P²CCD
P²CCD
OUTPUT AMPLIFIER P²CCD
CLOCK DRIVER LOGIC P²CCD
OUTPUT LOGIC P²CCD
MULTIPLEXER
PROBE INDICATION CHANNEL A+B
DATA BUS
TIME BASE SETTING DECODING
PHASE LOCKED LOOP
TIME BASE DIVIDERS
TRIGGER DELAY
DAC DELAY
ACL
MICROPROCESSOR 8085
READ ONLY MEMORIES FOR SYSTEM PROGRAMMING
RANDOM ACCES MEMORIES FOR STACKING AND STORING OF VARIABLE DATA
TRIGGER SOURCE SWITCH
AC/DC COUPLING
TRIGGER MODE SWITCH AND AMPLIFIER
TV CIRCUIT
PULSE STRETCHER
FAST RAMP
COMPARATOR
TIMING CIRCUIT
LEVEL
SLOPE
MAINS FILTER
RECTIFIER AND MAINS SELECTOR
OSCILLATOR AND SWITCHING CIRCUIT
OPTOCOUPLER
REGULATOR
~MAINS VOLTAGE
A AC/DC
A 0
A ON/OFF
ADD
B ON/OFF
B-0
B AC/DC
RECURR
SINGLE
MULTIPLE
ROLL
RUN/STOP
RESET
A AMPL/DIV
A CAL
B AMPL/DIV
B CAL
B INVERT
TIME/DIV
UP
RESET
DIGIT
DOWN
4xDISPLAY
3xINVERT
SELECT
LOCK
WRITE
CLEAR
3x SAVE
Yx1
Yx5
X=t
X=A
Y=B
PLOT
DOTS
EXT
EXT÷10
LINE
DC
AC
AUTO
TVF

Fig. 6.1.1.



6.1.1.1. *The vertical channels (unit A21 page 6—188)*

The vertical channel consist of two identical channels A and B except for the possibility B invert.
The sensitivity range is 10 mV/div ... 50 V/div in a 1-2-5 sequence.
All front panel settings of the vertical channels except for the CONTINUE an OFFSET controls are read each main loop of the program of the microprocessor system via multiplexers.
After calculation in the microprocessor, the settings are written into the switch setting decoding. This decoding generates the signals to set the ac/dc coupling, the high and low ohmic attenuators and the amplifier gain according to the front panel settings. Moreover these settings can be determined by the IEC Bus interface option
The input signal is applied to the channel switch via the ac/dc coupling, the high ohmic attenuator, the impedance convertor, the low ohmic attenuator and the amplifier.
Just after the amplifier a zero in signal NULIN for P^2CCD-mode operation is applied to the channel switch.
For time base settings of 3600 s/div. 0.5ms/div - and 0.2 μs/div - 5 ns/div the channel switch connects the signal to the delay line.
In dual channel mode (A and B) the microprocessor system generates via the switch setting decoding the signals A ON and B ON in such a way, that a chopped signal is applied to the delay line. The output of the delay line is connected to a compensation network to correct the faults introduced by the delay line.

6.1.1.2. *The analog-to-digital convertor (including P^2CCD) (unit A10 + A11 page 6—110 and page 6—122).*

The output signal of the delay line is applied to the T&H (Track and Hold) gate via a subtractor.
This T&H gate tracks the input signal continuously and at a command TANDH its output is held to the momentary value of the input signal for about 4 μseconds. The signal TANDH is generated on the trigger unit and will be described later. Via a low frequency amplifier and a multiplexer the output signal of the T&H gate is applied to the sample and hold gate of an ADC in which the output signal of the T&H gate is taken over and held to the same value for at least the conversion time.
The ADC is controlled by the signals TRACK and CLADC which are generated at the Acquisition Control Logic A9 (ACL).

To eliminate faults of the ADC conversion a correction takes place.
In ROLL, DIRECT and SAMPLING (see operating manual and chapter 6.1.1.6.) mode the correction functions as follows:

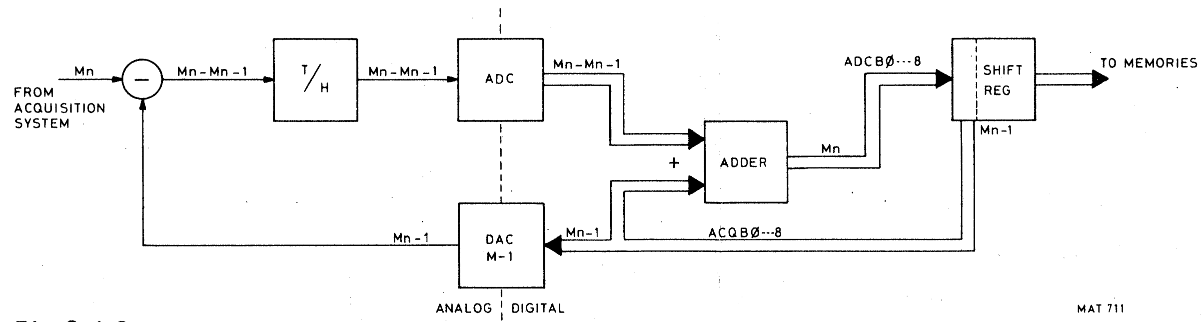
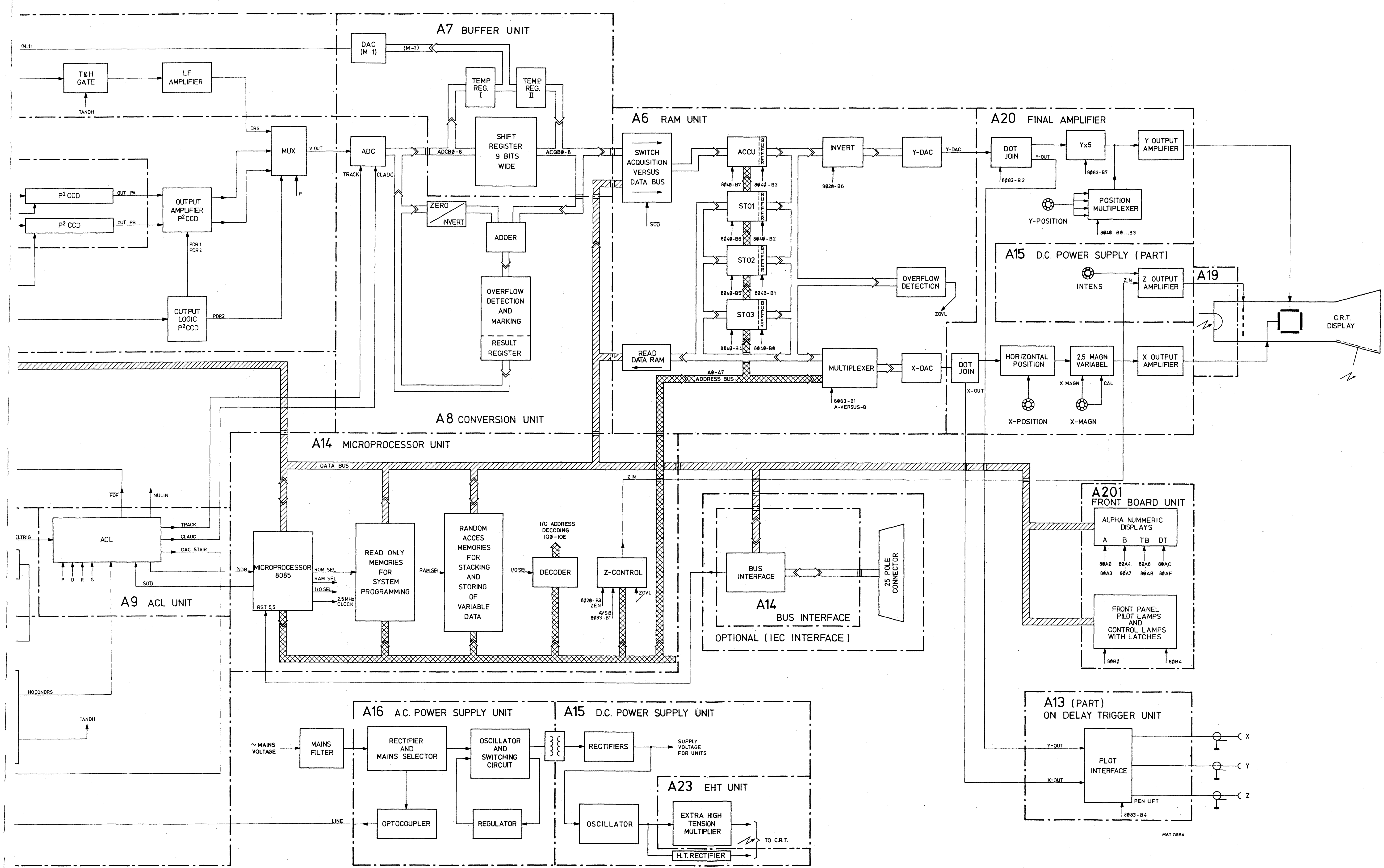


Fig. 6.1.2.



A7 BUFFER UNIT
DAC (M-1)
T&H GATE
LF AMPLIFIER
TEMP REG. I
TEMP REG. II
SHIFT REGISTER 9 BITS WIDE
MUX
ADC
ZERO INVERT
ADDER
OVERFLOW DETECTION AND MARKING
RESULT REGISTER
OUTPUT AMPLIFIER P²CCD
OUTPUT LOGIC P²CCD
P² CCD
A8 CONVERSION UNIT
A6 RAM UNIT
SWITCH ACQUISITION VERSUS DATA BUS
READ DATA RAM
ACCU
ST01
ST02
ST03
BUFFER
INVERT
Y-DAC
OVERFLOW DETECTION
MULTIPLEXER
X-DAC
ADDRESS BUS
A20 FINAL AMPLIFIER
DOT JOIN
Yx5
Y OUTPUT AMPLIFIER
POSITION MULTIPLEXER
Y-POSITION
A15 D.C. POWER SUPPLY (PART)
INTENS
Z OUTPUT AMPLIFIER
A19
C.R.T. DISPLAY
HORIZONTAL POSITION
2,5 MAGN VARIABEL
X OUTPUT AMPLIFIER
X-POSITION
X-MAGN
A14 MICROPROCESSOR UNIT
DATA BUS
ACL
A9 ACL UNIT
MICROPROCESSOR 8085
READ ONLY MEMORIES FOR SYSTEM PROGRAMMING
RANDOM ACCES MEMORIES FOR STACKING AND STORING OF VARIABLE DATA
I/O ADDRESS DECODING IOØ-IOE
DECODER
Z-CONTROL
BUS INTERFACE
A14 BUS INTERFACE
25 POLE CONNECTOR
OPTIONAL (IEC INTERFACE)
A201 FRONT BOARD UNIT
ALPHA NUMMERIC DISPLAYS
A B TB DT
FRONT PANEL PILOT LAMPS AND CONTROL LAMPS WITH LATCHES
A13 (PART) ON DELAY TRIGGER UNIT
PLOT INTERFACE
PEN LIFT
X
Y
Z
A16 A.C. POWER SUPPLY UNIT
~ MAINS VOLTAGE
MAINS FILTER
RECTIFIER AND MAINS SELECTOR
OSCILLATOR AND SWITCHING CIRCUIT
OPTOCOUPLER
REGULATOR
A15 D.C. POWER SUPPLY UNIT
RECTIFIERS
SUPPLY VOLTAGE FOR UNITS
A23 EHT UNIT
OSCILLATOR
EXTRA HIGH TENSION MULTIPLIER
H.T. RECTIFIER
TO C.R.T.
MAT 789A

To reduce errors in conversion, analog samples for digitising are compared with preceding samples, these being subtracted so that only small increments are converted to digital values in the ADC. After conversion, the digital equivalent of the original analog signal is produced by adding the differential signal from the ADC to the digital value of the preceding sample.
Referring to the block diagram, M_n is the new sample of the input signal from the acquisition system; M_{n-1} is the preceding sample, derived from the shift register and re-converted by DAC M-1 to analog form. At the input to the Track and Hold circuit, M_{n-1} is subtracted from M_n to produce a differential analog voltage, which is then converted to digital form in the ADC and added to the preceding digital value M_{n-1}.

$$\text{i.e.}\ (M_n - M_{n-1}) + M_{n-1} = M_n$$

After this procedure, the adder output value M_n will be shifted into a shift register as a new and corrected value. This system of digital adding is also used, in a different way, in the P^2CCD-mode as described below.

For time base settings of 0.2 ms/div - 0.5 μs/div the instrument operates in P^2CCD mode. P^2CCD means Profiled Peristaltic Charge Coupled Device in which an input signal can be written-in at a high speed and afterwards can be read out at a low speed.

If the instrument operates in P^2CCD mode, the output of the channel selector is applied to the input amplifier of the P^2CCD. Because of the principle of the P^2CCD in dual channel mode the signals – A and + B are applied as P AMP OUT 1 and P AMP OUT 2 resp. The P^2CCD contents is read out by a 78 kHz signal and written in by a Time Base Fast (TBF) pulse via the clock driver input logic. The output of the P^2CCD is amplified and applied to a multiplexer which switches between the two P^2CCD outputs. So in the P^2CCD mode the chopper switch of the channel switch is inoperative.
Output VOUT of the multiplexer is applied to the sample and hold gate of the ADC.

Due to internal P^2CCD faults and differences between the frequencies f_{in} and f_{out}, an incorrect zero level of the P^2CCD output signal is possible as shown in the following graph.

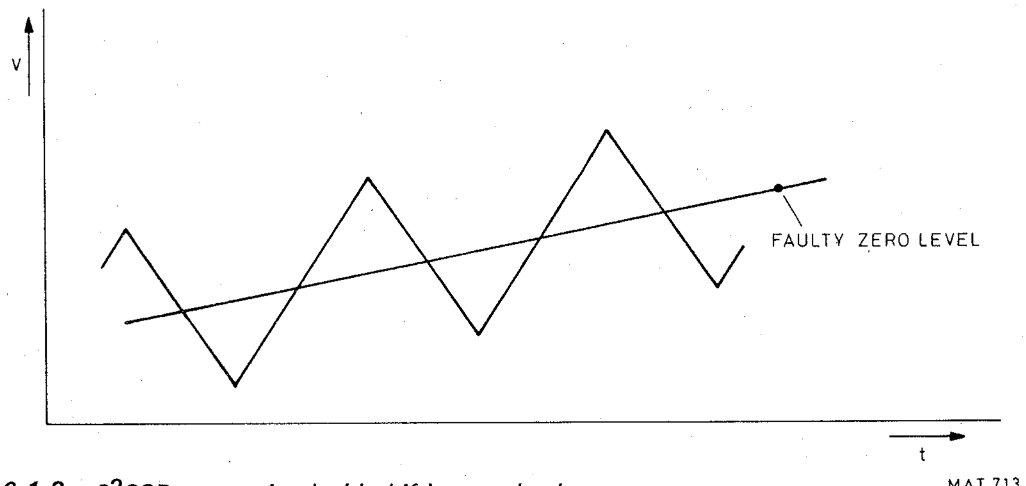


Fig. 6.1.3. P^2CCD output signal with shifting zero level

Under these conditions, the total faulty contents of the P^2CCD are converted from analog form to digital in 256 steps and after each conversion the data is put on the ADCBØ ... ADCB8 bus and directly shifted into the 9-bit shift register on buffer unit A7. After 256 steps, the total P^2CCD contents are stored here, and the register is then blocked.

In order to correct the zero level, the P^2CCD input is switched to zero by a signal NULIN and 256 samples of this zero signal are shifted into the P^2CCD at the same frequency f_{in} as for the normal input signal.

By reading the P^2CCD contents again, with the same frequency f_{out} (78 kHz) as for the faulty ADC input signal, an incorrect zero level having the same errors as described above will appear on the P^2CCD output as shown below.

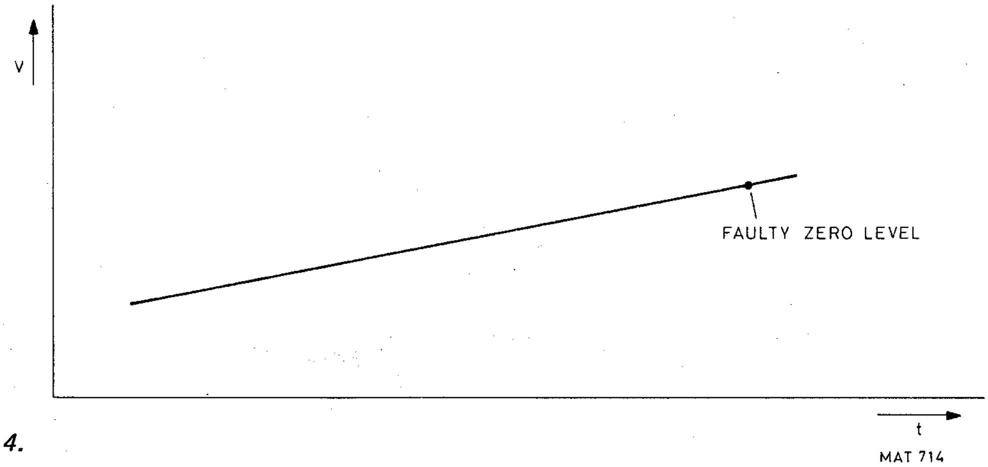


Fig. 6.1.4.

This incorrect zero level is then digitally subtracted (in 256 steps) from the faulty ADC input signal, which was already stored in the shift register.
The corrected result is then re-stored in the shift register.

6.1.1.3. *Trigger and trigger delay circuits (unit A22 page 6–211)*

In the trigger channel a signal derived from one of the sources A, B, external or line is applied to the AC/DC switch. The output of this switch is applied to the automatic level circuit which determines the peak-peak value. If automatic triggering is selected the peak-peak value is applied to the level potentiometer to obtain the possibility to level over the complete signal.
In the modes AC or DC a constant voltage is applied to the level potentiometer. In TVF mode the same voltage is applied to both sides of the potentiometer so that leveling is inoperative.
The slope determines which voltage is selected; positive or negative peak voltage.
After amplification the slope is selected and the trigger signal is applied to the pulse stretcher. The TV path in parallel applies its output signal also to the pulse stretcher.
If the TV signal contains equalisation pulses there is a selection to odd or even frame pulses. Otherwise only frame pulses are available at the output.
The pulse stretcher output signal is applied to two circuits: the sampling circuit and the trigger delay circuit.
The trigger delay circuit contains a down counter of which the loading is effected by the microprocessor system via an output port with a value derived from the front panel settings in combination with the TIME/DIV switch setting. Upon the receipt of a trigger pulse from the trigger circuit the down-counter starts counting time base pulses (see also 6.1.1.5.) until its zero state is reached. This effects in a pulse which blocks the reading of new information in the shift register. After this the shift register contents can be copied in the ACCU memory.

6.1.1.4. *The sampling system (unit A22 page 6–211)*

In sampling mode the output of the pulse stretcher is controlling the fast ramp generator. The ramp is determined by the TIME/DIV switch setting via the microprocessor and the control signals LØ ... L2. The fast ramp output is applied to a comparator. At the other input of the comparator a signal DACSTAIR is applied which is a stair case voltage derived from the ACL counter that increases one step every time that a conversion is completed and a COUNT pulse is counted by the ACL counter. To this staircase voltage a voltage called DACDEL is added which is derived from the trigger delay unit. This is a voltage proportional to the preset trigger delay.
If now the fast ramp voltage reaches the same potential as the sum of DACDEL and DACSTAIR, the system generates a HOCON (Hold and convert) and a TANDH (Track and hold) pulse to start an analog to digital conversion. If a conversion is completed the output of the pulse stretcher is enabled to generate via the fast ramp generator a new HOCONDRS pulse to start the next conversion. Now the DACSTAIR signal will be increased one stair level so this conversion takes place at the following point of the repetitive input signal.

6.1.1.5. *The time base system (unit A12 page 6–135)*

With respect to an ordinary oscilloscope this digital storage oscilloscope does not need a sawtooth time base generator because the position on the screen is determined digitally.
Therefore the time-base system consists mainly of frequency dividers.
The base frequency is 2.5 MHz derived from the cristal clock frequency of the microprocessor system.
Because the need of higher frequencies then 2.5 MHz a voltage controlled oscillator is introduced with a frequency of 100 MHz. This frequency is kept stable by dividing it by a factor of 80 and to compare it with the microprocessor clockpulse divided by a factor of 2. Now both signals have a frequency of 1.25 MHz and via a feedback loop the VCO is controlled.
For the P^2CCD mode a TBF signal is generated and in DIRECT and ROLL mode a TBS signal.
The dividing factors, so the frequencies of the TBF and TBS signals, are determined by the setting of the TIME/DIV switch which is decoded by the time base setting decoding.
The frequency of the TBF and TBS signals is such that for one horizontally division on the screen exactly 25 TBF or TBS periods are generated.

6.1.1.6. *The acquisition control (unit A9 page 6–92)*

The most important part of the acquisition control is a counter which counts the number of conversions by counting COUNT pulses.
Each conversion is initiated by a HOCON (hold and convert pulse) and results after completion into a COUNT pulse.
So it is counting how many input values are written into the shift register.

The acquisition control is operating in a different way for each of the four system modes DIRECT (D) - ROLL (R) - SAMPLING (S) and P^2CCD (P).
In each of these four modes NDR (New Data Ready) pulses are generated to indicate to the microprocessor that new data is ready and can be copied in the ACCU memory.
The microprocessor in turn answers with SOD pulses telling that the copying of new information into the ACCU memory is completed and that new information can be stored in the shift register.

Direct mode

After a hold-off period in which at least 256 new input signal samples are shifted into the shift register, so after a total refreshment of the shift register contents the acquisition system is enabled to react on a new trigger pulse.
Upon the receipt of such a trigger pulse a NDR pulse will be generated just after the completion of the last conversion.

ROLL-mode

The ROLL-mode action is started when ROLL-mode is selected and the front panel R/S pushbutton is depressed. This results in the generation of TBS pulses by the time-base unit. These TBS pulses are converted by the trigger unit in HOCONDRS (Hold and convert) pulses which are used in the ACL unit to initiate the conversions of new input signal samples.
After each completed conversion a COUNT pulse is generated and so a NDR pulse.

On each NDR pulse the total shift register contents are copied into the RAM memory and in the same time the shift register output information is shifted again into this shift register by coupling the output of the shift register directly to its input.
Furthermore ROLL-mode functions are under the control of the software.
The software counts the number of NDR pulses and after 256 NDR pulses it saves the ACCU contents into STO3, after again 256 pulses into STO2, then into STO1. After in total 4 x 256 pulses the software stops the ROLL-mode action and indicates this by generating a flashing command for the RUN lamp.

Sampling mode

In sampling mode a HOCONDRS pulse is generated on each incoming TRIST pulse except for those coming within the hold-off period. These HOCONDRS pulses initiate conversions of the input signal samples.
After 256 samples are converted and stored in the shift register a NDR pulse is generated and the shift register contents are copied into the ACCU memory.
The microprocessor generates a $\overline{\text{SOD}}$ signal after this copying, the ACL counter is reset to zero and the system reacts again on new incoming triggers.

P2CCD-mode

After reading in at least 256 samples of new input information into the P2CCD circuit, these samples are read out, converted and shifted into the shift register.
Then for a period of about 5 ms zero information will be shifted into the P2CCD, controlled by the signal NUL IN from the ACL unit which is active in the vertical channels (see also 6.1.1.1.).
These zero information is then read out and corrected (see also 6.1.1.2.) with the 256 samples of signal information which was already stored in the shift register and the corrected information is shifted again in the shift register. This total procedure results then in a NDR pulse and copying of shift register contents into the ACCU memory can be started.

6.1.2. Display system

The display part consists of hardware to store and display data on the CRT display. Moreover this part arranges the coding for information to be displayed on pilot and control lamps and on the alphanumeric display.
This chapter can be divided in:

6.1.2.1. Memories
6.1.2.2. Dot join and plot
6.1.2.3. Vertical amplifier
6.1.2.4. Horizontal amplifier
6.1.2.5. CRT section
6.1.2.6. Alphanumeric display

6.1.2.1. Memories (unit A6 page 6–61)

The memories are consisting of four separate parts which can be written and read independently. If from the acquisition control logic the signal New Data Ready arrives, new information is written in the ACCU.
This means that the contents of the shift register is copied in the ACCU.
This information is now read out continuously with a speed, determined so that the display on the CRT seams to be steady.
At a "SAVE" command the contents of the ACCU is copied in one or more of the registers STO1 . . . STO3.
The registers STO1 ... STO3 can only copy information from the ACCU. The only other possibility to write in one of the memories STO1 . . . STO3 is with the use of the IEC-bus interface via the databus.
The information is stored in the memories as a two-complement notation which means that the data are integers with values from −128 up to and including +127. To convert this in straight binary notation for the YDAC only the most significant bit has to be inverted. After that the complete information can be inverted by operating the push pull knobs "pull to invert". This inversion takes place by an eight-bit-exclusive-or.
Via the databus the information can be applied also to the X-DAC. This is necessary in the mode X = A; Y = B.

6.1.2.2. Dot join and plot (unit A20 page 6–178)

If the mode "DOTS" is selected separate dots will appear on the CRT display.
The dot join circuit generates straight lines between the consecutively dots. The block diagram of the dot join principle is shown in the figure below.

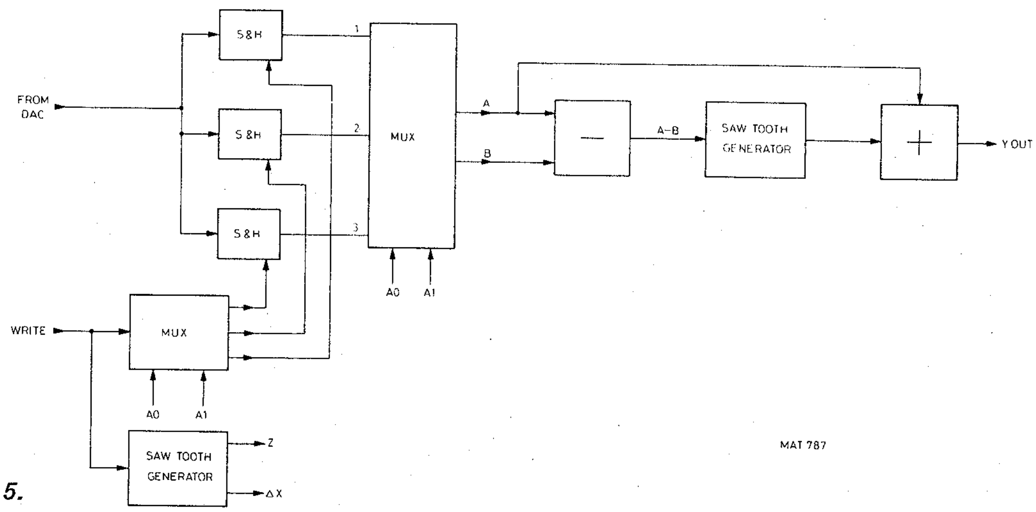


Fig. 6.1.5.

In dual channel operation on points 1 and 3 is always the information of one channel. By the control signals AØ and A1 this information is switched to the output of the multiplexer. Suggest A is the oldest information and B the newest, then, the subtractor output is A-B. This voltage controls the variable sawtooth generator of which the ramp is determined so that the B value is reached before a new write pulse arrives. The output of the sawtooth generator is added to the oldest information A and applied to the final amplifier.
If the sawtooth generator is reset the CRT display is blanked.
For X-deflection also a sawtooth voltage is generated but now with a fixed ramp and amplitude.
The plot action is principally a software matter.
The microprocessor system activates the sample and hold gates for the plots so that every 0.25 sec a new sample is taken. This is visible on the CRT display as an intensified point so it is traceable for how far the plot action is got.
The speedness is choosen in such a way that a simple chart recorder is able to record the information.

6.1.2.3. *Vertical amplifier (unit A20 page 6–178)*

After the dot join it is possible to magnify the signal 5x. Now it is possible to obtain the contents of the ACCU or STO1 ... STO3 for full screen deflection. In Y x 1 mode for each memory two divisions are available. Midrange of the position controls effects in displaying the memory base lines on the CRT at resp. 1, 3, 5 and 7 cm with respect to the screen top. This offset is switched to zero if the Y x 5 mode is choosen.
Now all base lines of the memories are situated in the centre of the screen.
The final amplifier consists of a long tailed pair which drives the CRT directly. This is possible because of the low bandwidth of 1 MHz.

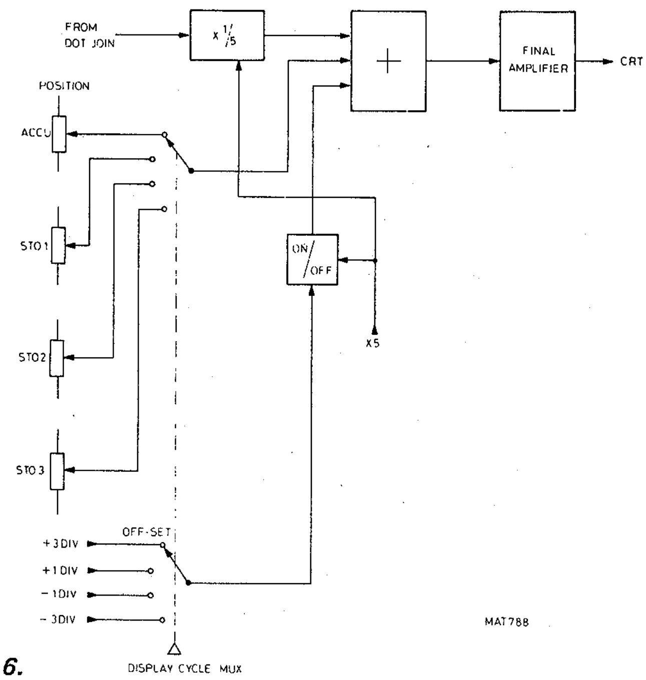


Fig. 6.1.6.

6.1.2.4. *Horizontal amplifier (unit A20 page 6–178)*

The horizontal amplifier consists of an integrated circuit for the magnifier adjusting and a final amplifier consisting of two shunted feedback pushpull amplifiers. Position control is effected at the input of the integrated circuit.

6.1.2.5. *CRT section (unit A15 page 6–157)*

Because of the principle of the CRT it is not necessary to correct the barrel and pin cushion distortion.
The cathode current of the CRT as used in the concept of this oscilloscope will never yet very high so that a focus voltage dependent to the intensity setting can be arranged automatically. Now there is no need for a front panel focus control.
The Z-control is arranged by the microprocessor system.
Only if a memory is read the CRT is unblanked.
If via the overflow detection a maximum or a minimum value is exceeded this part is displayed with a frequency of approx. 5 Hz so the display blinks.

6.1.2.6. *Display (unit A2 page 6–25)*

There are four front-panel alphanumeric displays:
– channel A V/DIV display
– channel B V/DIV display
– s/DIV display
– DIV display.

Each of these alphanumeric displays is an intelligent four-digit unit with a built-in CMOS integrated circuit. The integrated circuit contains a memory, an ASCII-character generator, and a LED multiplexing and drive circuit.

The displays are controlled by the microprocessor, each individual display section being selected by means of addresses fed to the ADDRESS-bus by the microprocessor.

The characters that are required to be displayed are generated by the microprocessor system in Standard ASCII character code and are placed on the databus (signals DØ ... D7).

Control and pilot lamps

The NOT TRIG'D, RUN and REMOTE lamps are directly controlled by the signals $\overline{\text{NOT TRIG'D}}$, $\overline{\text{RUNL}}$ and $\overline{\text{REM}}$, which are generated on the microprocessor board.

The DISPLAY lamps, the SELECT lamps, the UNCAL A and UNCAL B lamps, the A and B AMPL/DIV control lamps and the TIME/DIV control lamps are controlled by addresses generated by the microprocessor system.

6.1.3. **Microprocessor** (unit A4 page 6–45)

As shown in the simplified block diagram, the micro-processor unit basically consists of the following circuit elements:
– A micro-processor integrated circuit block for controlling and organising data flow.
– Ereasable and programmable read-only memories (EPROMs) for system programming.
– Random-access memories (RAMs) for stacking and storing the variable data.
– Address and data selection latches for the multiplexed address bus.
– Decoders for RAM and ROM selection and address decoding.
– Trap and watchdog circuits to guard against loss of data
– Two-way buffer circuit to the system data-bus.
– A blanking circuit for the c.r.t.

The heart of the microprocessor unit is an 8-bit microprocessor type 8085 with 16 address lines.
The first eight address lines AØ ... A7 are multiplexed with the eight data lines DØ ... D7 and are defined as ADØ ... AD7. Addressing is selected by the ALE (address latch enable) signal from the microprocessor, which gives an external indication when address information is on the bus-lines.

Trap Input Circuit

The TRAP input is effective when the battery back-up facility is used. It prevents the RAM contents being disturbed when the instrument is switched off or in the event of a power failure. The TRAP input forces the microprocessor to continue with the execution of the program at the starting address of the POWER DOWN routine. Failure of the power supply activates the TRAP input of the microprocessor.

A 5 MHz crystal, is connected to the clock inputs of the microprocessor to provide an accurate timing reference source.

A reset signal is generated when the instrument is switched ON. This reset signal forces the microprocessor to start the execution of the main program.

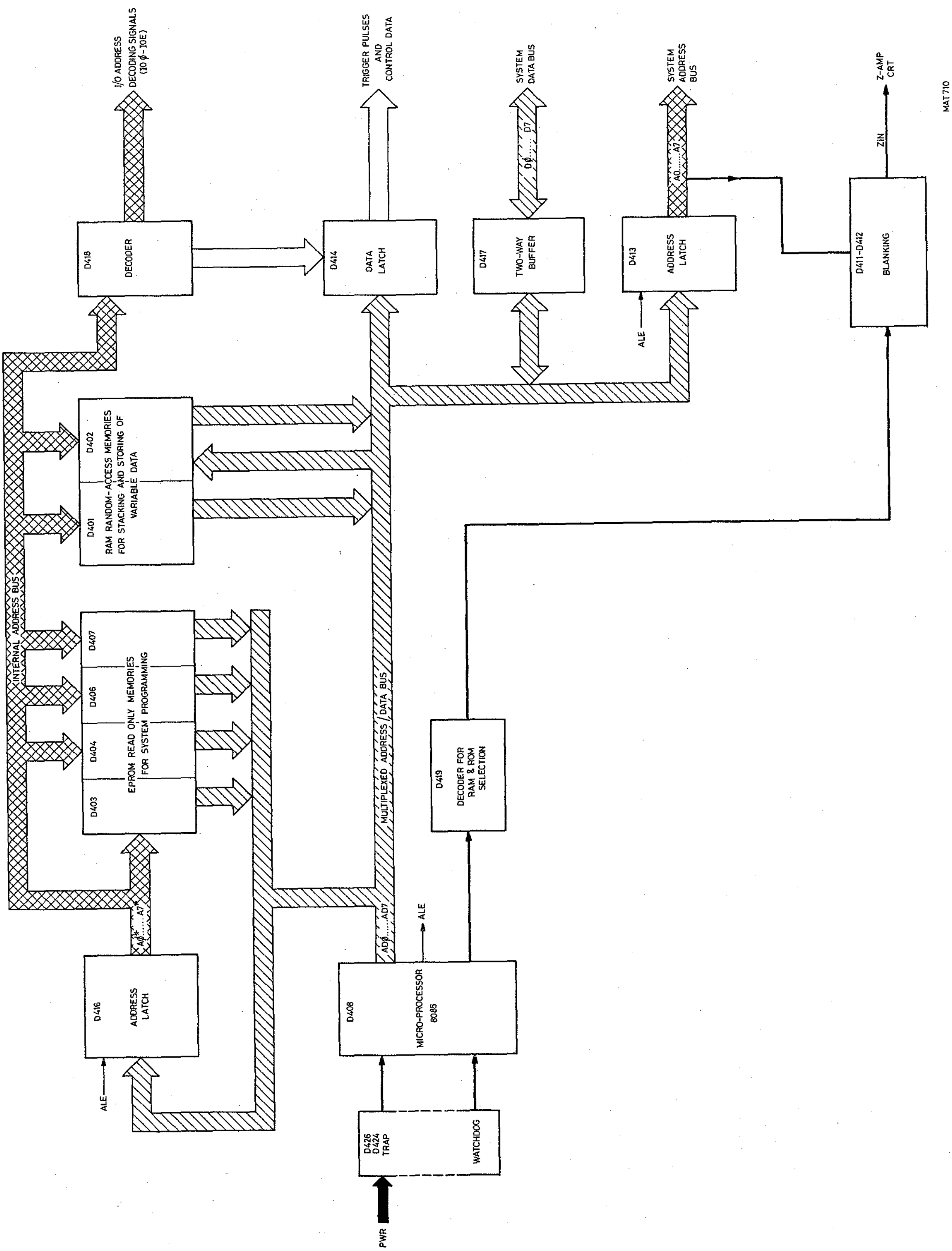


Fig. 6.1.7. Simplified block diagram microprocessor unit.

Connection to the system address bus

The first eight address bits placed by the microprocessor on the multiplexed address-data bus lines ADØ ... AD7 have to be separated from the eight data bits.
This separation is achieved by an address latch, which is enabled by signal ALE.
The group of output signals AØ ... A7 constitute the system address bus.

Connection to the system data-bus

The eight data bits placed by the microprocessor on the multiplexed address-data bus lines ADØ ... AD7 have to be separated from the first eight address bits.
This separation is done by a bidirectional buffer.

System memory map

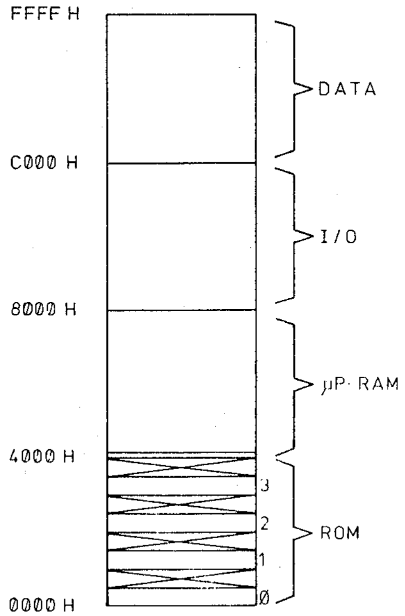


Fig. 6.1.8.

MAT 832

ROM memory

The ROM (read-only memory), which contains the system program, consists of the four EPROM chips of 2K-bytes each (2048X 8 bits).
Because the microprocessor's first eight address lines ADØ ... AD7 are multiplexed in the microprocessor with the data lines, the addresses have to be latched by the address latch D416 with the aid of the ALE signal.
When a certain ROM address is selected, the contents of the selected location are placed on the multiplexed address-data bus lines ADØ ... AD7.

RAM memory

The µP-RAM (microprocessor random access memory) is used by the microprocessor for stack purposes and for storage of variable data.
It consists of two RAM chips - of ¼ K-nibbles each (256 x 4 bits), which means that a maximum of 256 bytes of data can be stored.

Each µP-RAM memory address can be selected by the address lines AØ* ... A7*

Reading the RAM contents or writing data into a RAM location is controlled by the signals $\overline{RD}$* and $\overline{WR}$*

The data to be written into, or read from the RAM memory is transported via the multiplexed address-data bus ADØ ... AD7.

Blanking circuit

This circuit provides for a blanking signal ZIN (Z-amplifier input) for blanking the trace on the c.r.t. display.

6.1.4. Power supply (unit A15 page 6–157 and A16 page 6–166)

The mains voltage is applied via the mains filter and the mains selector switch on the AC POWER UNIT A16 to a rectifier where it is full-wave rectified and fed to a regulated sine-converter (oscillator and switching circuit).
The output voltage of the sine converter is kept constant by regulating the duty cycle of the applied voltage by a special integrated circuit.
This output voltage is applied to the primary of a transformer, the secundary voltages of this transformer are applied to DC POWER unit A15 where they are full-wave rectified, smoothed and applied to the various circuits.
Also the voltages for the C.R.T. filament and the C.R.T. cathode (−1,5 kV) are generated here.
The −1.5 kV is also applied to the EHT unit A23 which gives a high tension for g8 of the C.R.T.

The MAINS triggering is taken direct from the mains and, via an opto-isolator, fed to the trigger circuitry on a safe level.

6.2. UNIT DESCRIPTIONS

6.2.1. Front side unit A1

The front side unit consists of an aluminium front cast on which the following items are mounted.

- LED B24 + LED-holder
- Light reflector assembly inclusive two lampholders and two 28 V - 80 mA lamps E1 and E2.
- CAL output terminals X1 and X2.
- Measuring earth socket X5.
- BNC input socket X6 for external triggering.
- LEVEL/SLOPE control R9/S27.
- INTENS control R15.
- TRACE ROTATION control R16.
- Trigger mode selector switch S29.

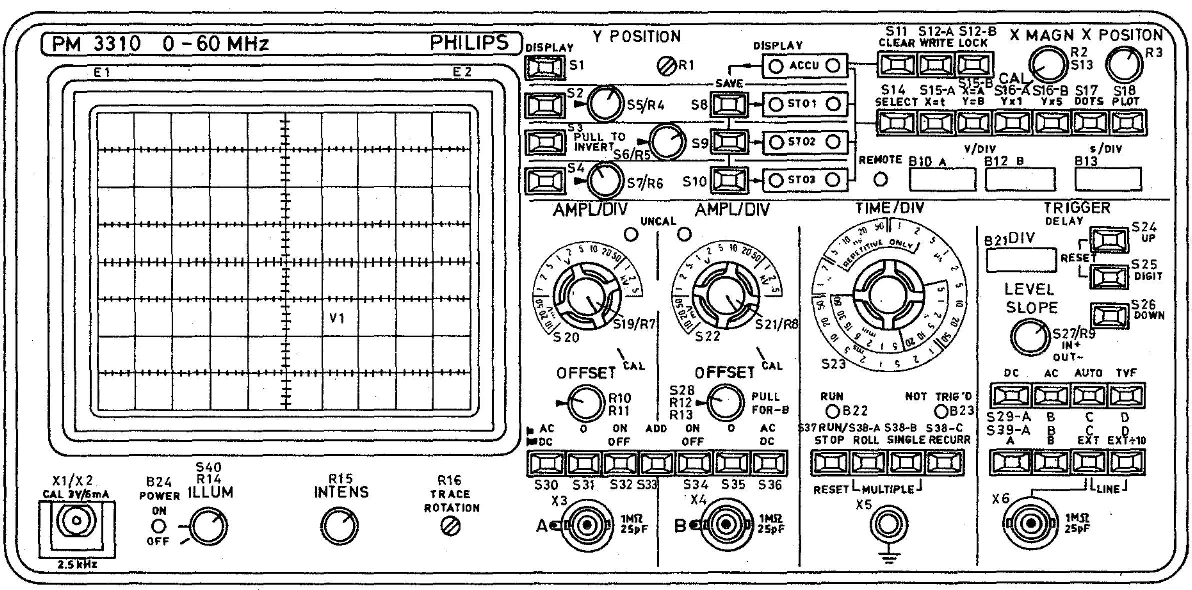


Fig. 6.2.1.

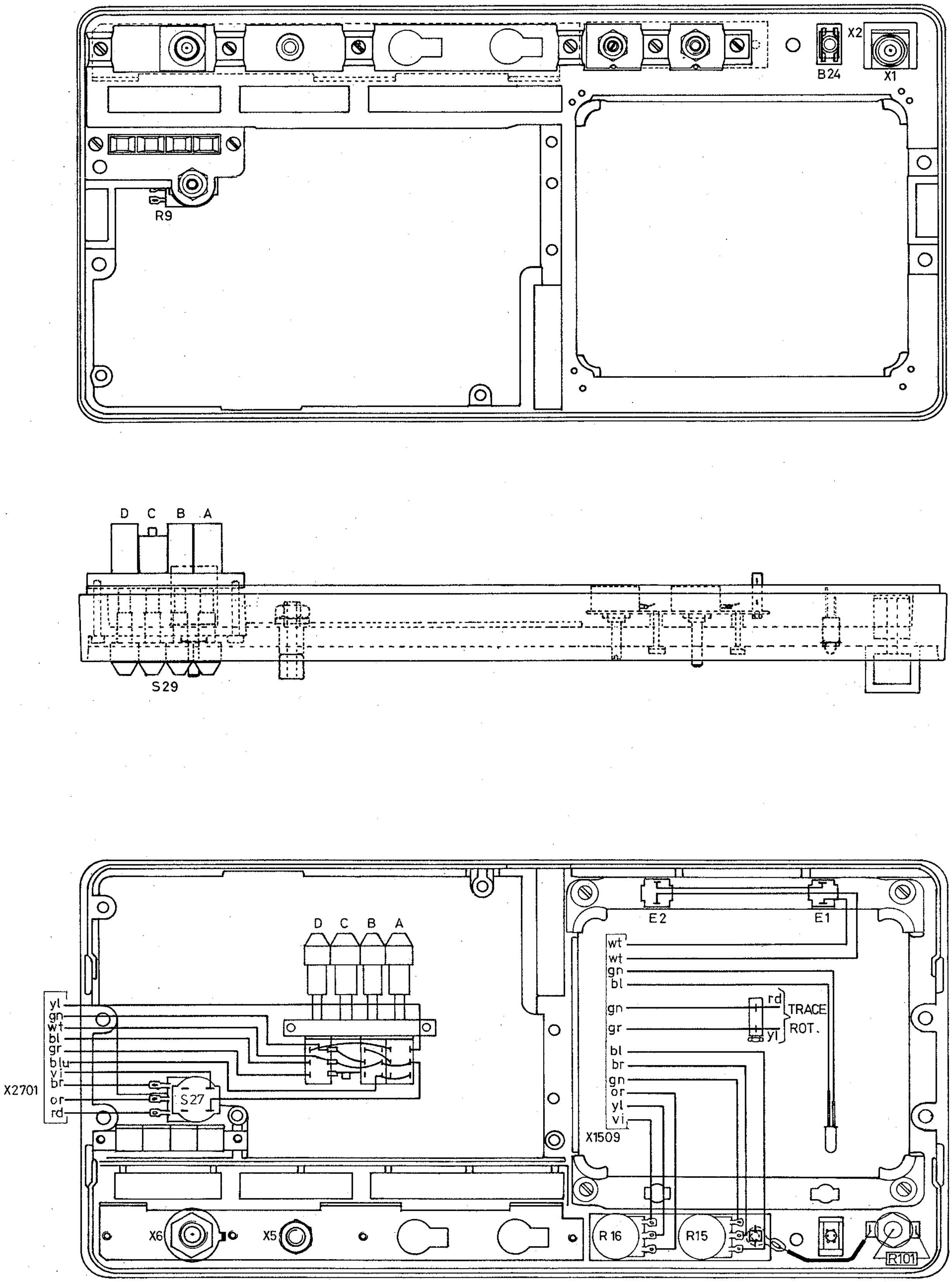


Fig. 6.2.2.

MAT 707A

6.2.2. Front unit A2

6.2.2.1. Front board A201

The front board houses all the front-panel control lamps, pilot lamps and alphanumeric displays.

Alphanumeric intelligent displays

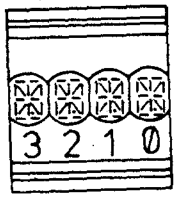
There are four front-panel alphanumeric displays:
- channel A V/DIV display
- channel B V/DIV display
- s/DIV display
- DIV display

Each of these alphanumeric displays is an intelligent four-digit unit with a built-in CMOS integrated circuit. The integrated circuit contains a memory, an ASCII-character generator, and a LED multiplexing and drive circuit.

The displays are controlled by the microprocessor, each individual display section being selected by means of addresses fed to the ADDRESS-bus by the microprocessor.

DECADE	AØ	A1
Ø	0	0
1	0	1
2	1	0
3	1	1

DECADE



A V/DIV display

DECADE	CONTROL ADDRESS
Ø	8ØAØ
1	8ØA1
2	8ØA2
3	8ØA3

B V/DIV display

DECADE	CONTROL ADDRESS
Ø	8ØA4
1	8ØA5
2	8ØA6
3	8ØA7

s/DIV display

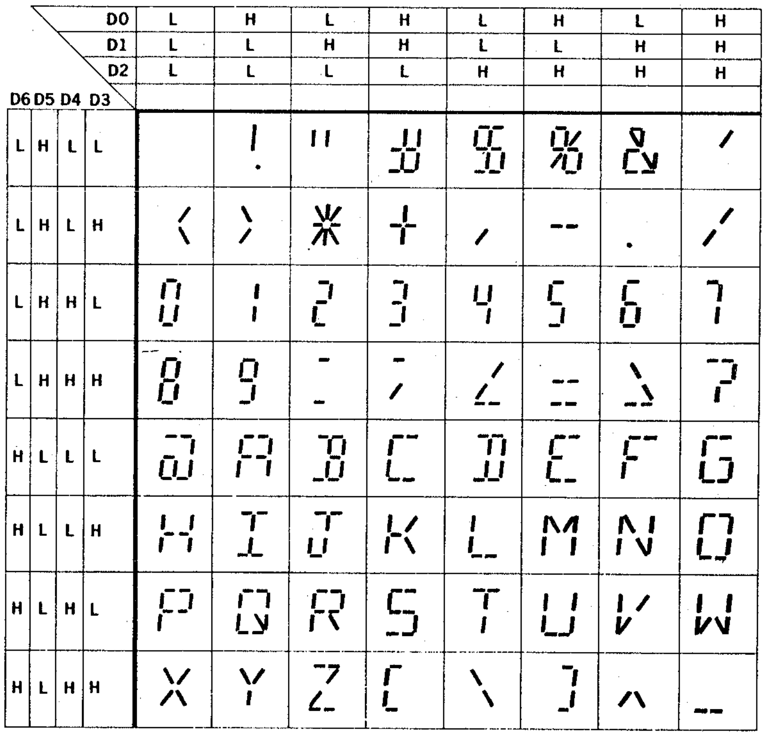
DECADE	CONTROL ADDRESS
Ø	8ØA8
1	8ØA9
2	8ØAA
3	8ØAB

DIV display

DECADE	CONTROL ADDRESS
Ø	8ØAC
1	8ØAD
2	8ØAE
3	8ØAF

The characters that are required to be displayed are generated by the microprocessor system in Standard ASCII character code and are placed on the data-bus (signals DØ ... D7).

CHARACTER SET



CHARACTER SET
(all other input codes display 'BLANK')

Control and pilot lamps

The NOT TRIG'D, RUN and REMOTE lamps are directly controlled by the signals $\overline{\text{NOT TRIG'D}}$, $\overline{\text{RUNL}}$, and $\overline{\text{REM}}$, which are generated on the microprocessor board.

The DISPLAY lamps (DISØ ... DIS3), the SELECT lamps (SELØ ... SEL3), the UNCAL A and UNCAL B lamps, the A and B AMPL/DIV control lamps LA1, LA1Ø, LB1, LB1Ø and the TIME/DIV control lamps LREC - LROLL are controlled by the addresses 8ØBØ and 8ØB4 as shown in the table in conjunction with the data bits DØ to D7.

ADDRESS	D7	D6	D5	D4	D3	D2	D1	DØ
8ØBØ	SEL3	SEL2	SEL1	SELØ	DIS3	DIS2	DIS1	DISØ
8ØB4	UNCB	UNCA	LROLL	LREC	LB1Ø	LB1	LA1Ø	LA1

Selection of a display segment or a group of pilot lamps or control lamps is achieved by decoder D203.
This three-bit decoder decodes the three address-bits A2, A3 and A4 if the input signal combination WR.IOA is active. This results in one active decoder output line at a time.
The IOA signal is an address decoding signal for address lines A5 ... A15 and decodes addresses 8ØAØ to 8ØBF.

INCOMING SIGNAL	OUTGOING SIGNAL	GENERATED ON UNIT	DESCRIPTION
AØ		A4	
A1		A4	
A2		A4	Address bits from system address bus
A3		A4	
A4		A4	
DØ		A4	
D1		A4	
D2		A4	
D3		A4	
D4		A4	Data bits from system data-bus
D5		A4	
D6		A4	
D7		A4	
$\overline{\text{NOT TRIG'D}}$		A4	Control for NOT TRIG'D lamp
$\overline{\text{IOA}}$		A4	Address decoding signal for addresses 8ØAØH - 8ØFFH (Display select)
$\overline{\text{REM}}$		A4	Control for REMOTE lamp
$\overline{\text{RUNL}}$		A4	Control for RUN lamp
$\overline{\text{WR}}$		A4	Signal WRITE from microprocessor
+5 V		A15	
⏚		A15	

FRONT BOARD A201

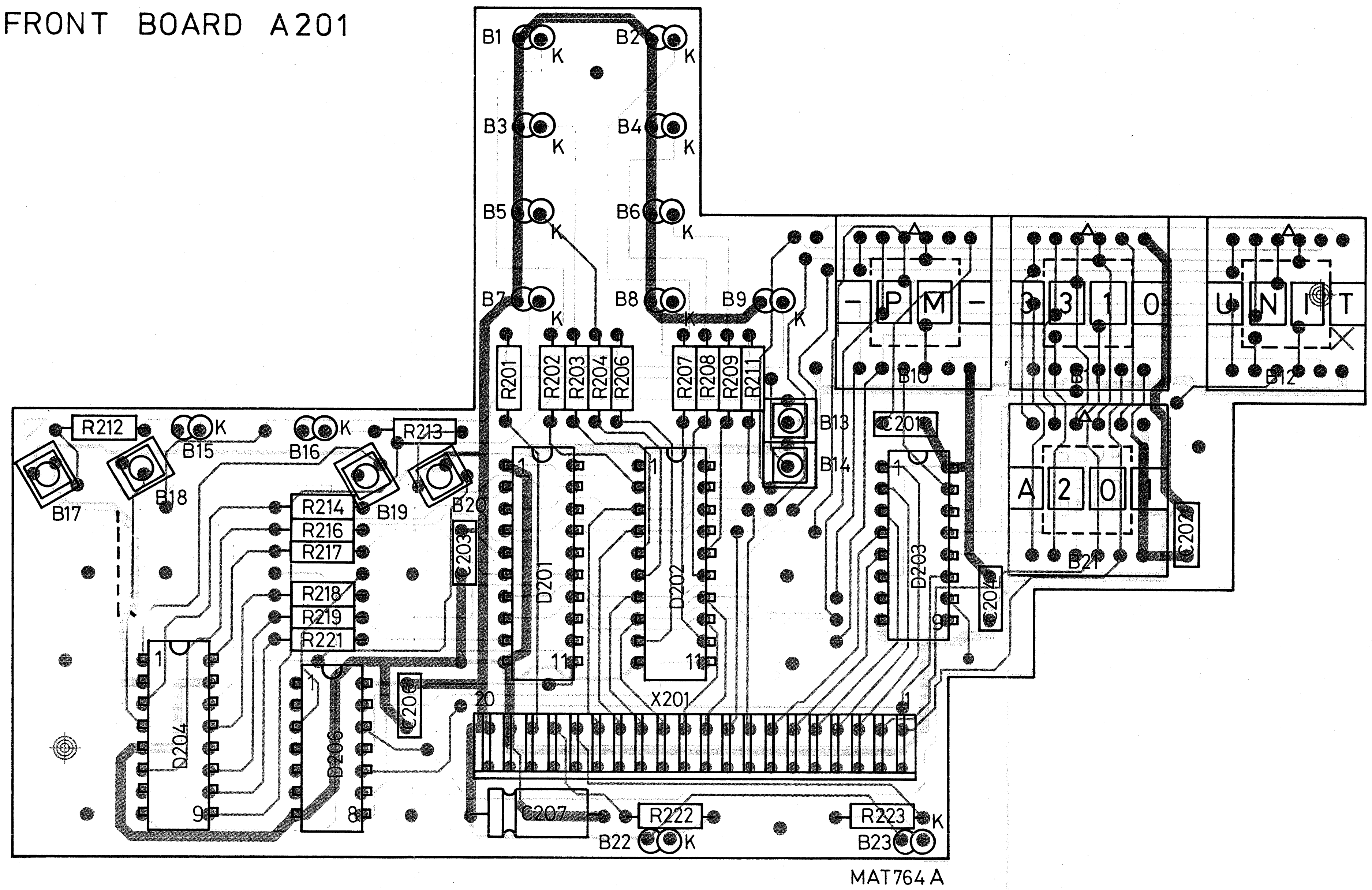
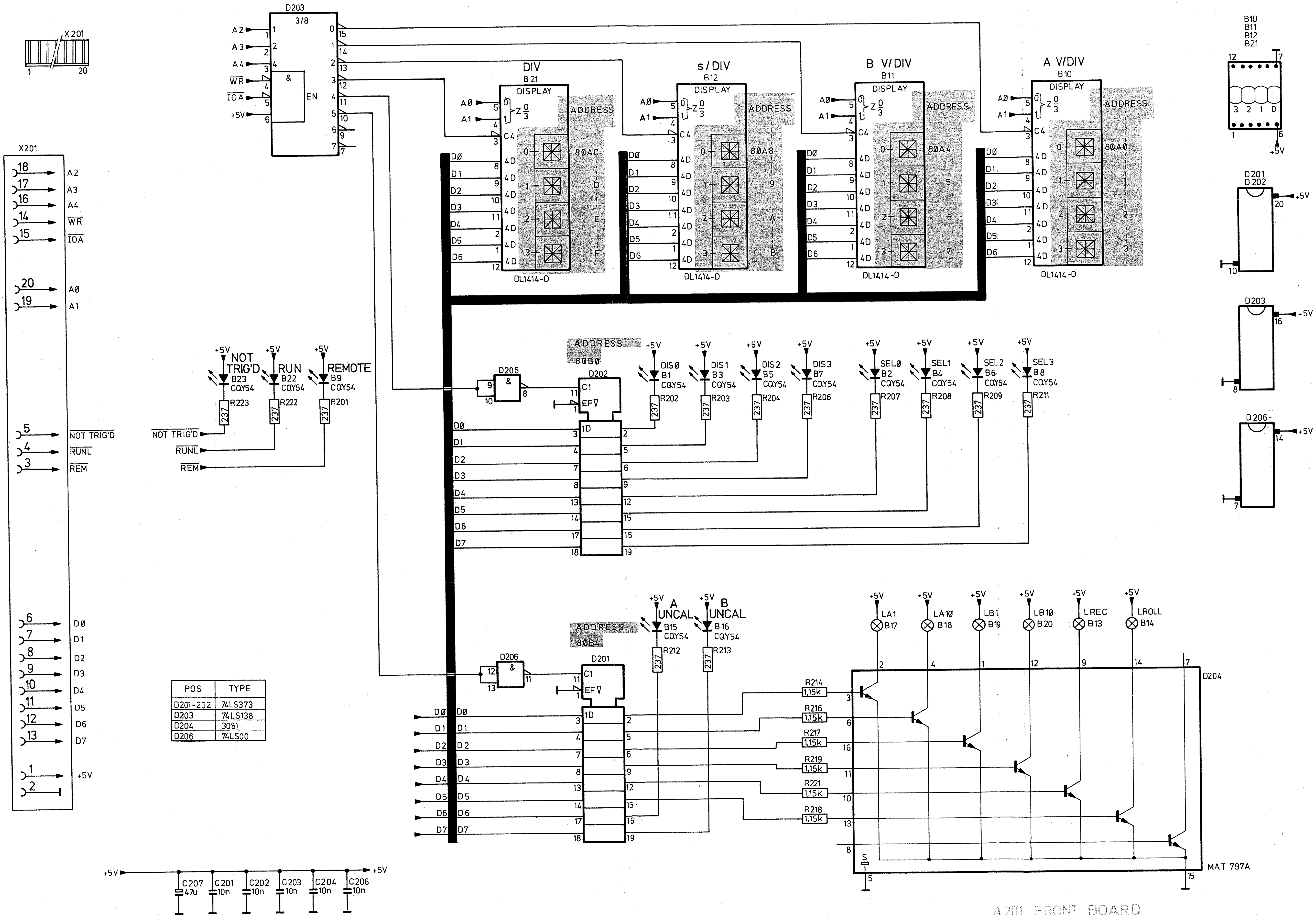


Fig. 6.2.3.



POS	TYPE
D201-202	74LS373
D203	74LS138
D204	3081
D206	74LS00

Fig. 6.2.4.

6.2.2.2. Switchboard A202 and Switch Units A203 ... A207

The front-panel controls listed below are located on these units.

A202 switchboard

SWITCHES	Circuit ref.	Switch signals
YA AMPL/DIV	S20	YA1 YA2 YA4 YA5 YA6 YA7
YB AMPL/DIV	S22	YB1 YB2 YB4 YB5 YB6 YB7
TB TIME/DIV	S23	TB1 TB2 TB4 TB5 TB6 TB7
INV STO1	S5	$\overline{\text{INV1}}$
INV STO2	S6	$\overline{\text{INV2}}$
INV STO3	S7	$\overline{\text{INV3}}$
CAL A	S19	$\overline{\text{CALA}}$
CAL B	S21	$\overline{\text{CALB}}$
INV YB	S28	$\overline{\text{BIN}}$
SERV 1	X241	$\overline{\text{SERV1}}$
SERV 2	X241	$\overline{\text{SERV2}}$

POTENTIOMETERS	Circuit ref.	Slider signals
X POSITION	R3	X POS
X MAGN	R2	X MAGN (+12 V in X CAL)
OFFSET A	R10/R11	OFF A
OFFSET B	R12/R13	OFF B
POS ACCU	R1	POSØ
POS STO1	R4	POS1
POS STO2	R5	POS2
POS STO3	R6	POS3
CONT A	R7	ACON
CONT B	R8	BCON

The slider signals of the above-listed potentiometers are applied to various units of the instrument via connector X259

A203 interconnection board

Provides the connection between units S201 and A202.

A204 display switch board

		Switch signals
DISPLAY ACCU	S1	$\overline{\text{DISØ}}$
DISPLAY STO1	S2	$\overline{\text{DIS1}}$
DISPLAY STO2	S3	$\overline{\text{DIS2}}$
DISPLAY STO3	S4	$\overline{\text{DIS3}}$

A 205 I delay switch board

UP ┐ RESET	S24	$\overline{\text{UP}}$
DIG ┘	S25	$\overline{\text{DIG}}$
DOWN	S26	$\overline{\text{DOWN}}$

A 205 II save switch board

SAVE STO1	S8	$\overline{\text{SAV1}}$
SAVE STO2	S9	$\overline{\text{SAV2}}$
SAVE STO3	S10	$\overline{\text{SAV3}}$

A206 clear switch board

CLEAR	S11	$\overline{\text{CLEAR}}$
WRITE	S12A	–
LOCK	S12B	$\overline{\text{LOCK}}$

A207 select switch board

SELECT	S14	$\overline{\text{SEL}}$
X=t	S15A	–
X=A/Y=B	S15B	$\overline{\text{A/B}}$
Yx1	S16A	–
Yx5	S16B	$\overline{\text{Yx5}}$
DOTS	S17	$\overline{\text{DOTS}}$
PLOT	S18	$\overline{\text{PLOT}}$

The settings of all the switches on the above units are read periodically by the microprocessor system via three groups of multiplexers, D241/D247, D242/D248, D243/D249 according to the following table:

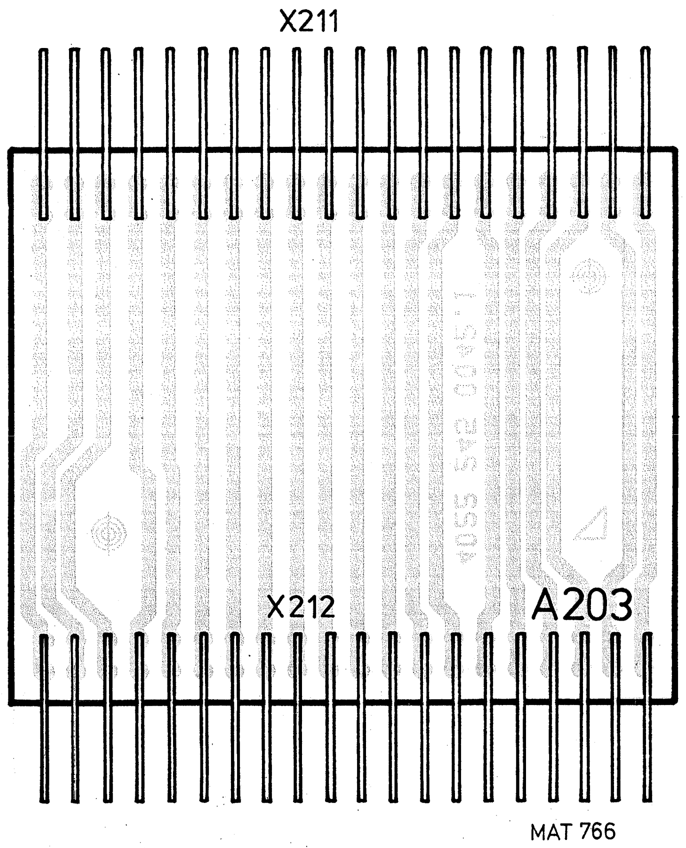
ADDRESS		AØF	D7	D6	D5	D4	D3	D2	D1	DØ
8Ø2Ø	$\overline{\text{RDFØ}}$=Ø	1	YA1	YA4	YA5	YA6	YA7	YA2	$\overline{\text{DIG}}$	$\overline{\text{CALA}}$
8Ø21	$\overline{\text{RDFØ}}$=Ø	Ø	YB1	YB4	YB5	YB6	YB7	YB2	$\overline{\text{BIN}}$	$\overline{\text{CALB}}$
8Ø22	$\overline{\text{RDF2}}$=Ø	1	TB1	TB4	TB5	TB6	TB7	TB2	$\overline{\text{UP}}$	$\overline{\text{DOWN}}$
8Ø23	$\overline{\text{RDF2}}$=Ø	Ø	$\overline{\text{DIS3}}$	$\overline{\text{DIS2}}$	$\overline{\text{DIS1}}$	$\overline{\text{DISØ}}$	$\overline{\text{INV3}}$	$\overline{\text{INV2}}$	$\overline{\text{INV1}}$	FRUN
8Ø24	$\overline{\text{RDF4}}$=Ø	1	+5 V	FASA	$\overline{\text{Yx5}}$	$\overline{\text{SEL}}$	$\overline{\text{SAV3}}$	$\overline{\text{SAV2}}$	$\overline{\text{SAV1}}$	DELTRG
8Ø25	$\overline{\text{RDF4}}$=Ø	Ø	$\overline{\text{PLOT}}$	Ø V	$\overline{\text{DOTS}}$	$\overline{\text{A/B}}$	$\overline{\text{CLEAR}}$	$\overline{\text{LOCK}}$	$\overline{\text{SERV2}}$	$\overline{\text{SERV1}}$

The selection of one of the multiplexer groups and the internal setting of the selected group is made via the address selector circuit, which consists of NAND-gate D244 (11, 12, 13) and the three-to-eight decoder circuit D246, as shown in the following table:

ADDRESS	$\overline{\text{IO2}}$	A3	A2	A1	AØ	AØF
8Ø2Ø	Ø	Ø	Ø	Ø	Ø	1
8Ø21	Ø	Ø	Ø	Ø	1	Ø
8Ø22	Ø	Ø	Ø	1	Ø	1
8Ø23	Ø	Ø	Ø	1	1	Ø
8Ø24	Ø	Ø	1	Ø	Ø	1
8Ø25	Ø	Ø	1	Ø	1	Ø

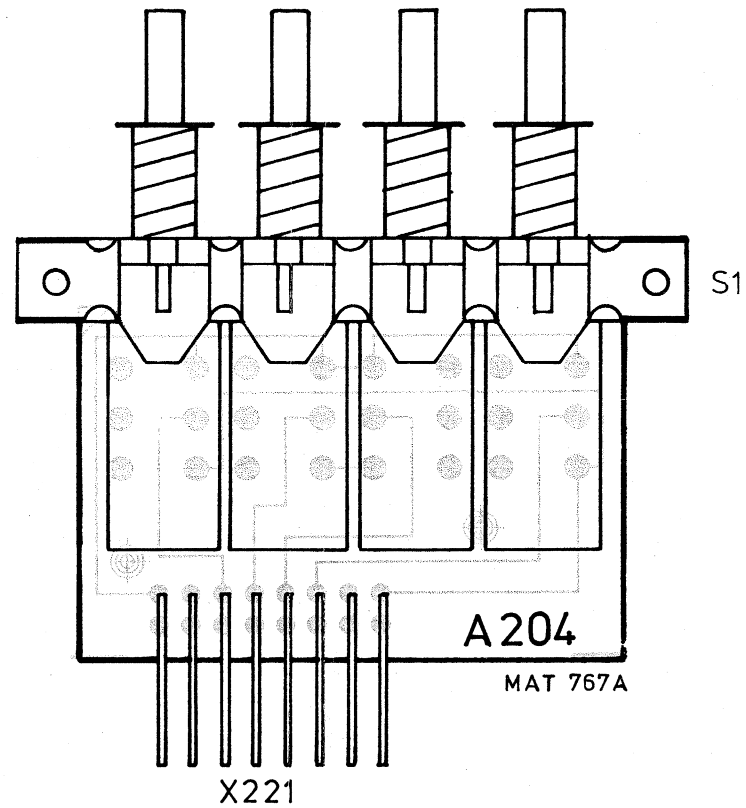
INCOMING SIGNAL	OUTGOING SIGNAL	GENERATED ON UNIT	USED ON UNIT	DESCRIPTION
AØ ... A4		A4		Address bits from system address-bus
	ACON	A202	A21	Slider of channel A continuous control
	BCON	A202	A21	Slider of channel B continuous control
DØ ... D7		A4		Data bits from system data-bus
	DØ ... D7	A202	A4	Data bits to system data-bus
DELTRG		A13	A9	Delayed trigger signal
FASA		A9		Output phase flip-flop
FRUN		A13		Freerun signal
$\overline{\text{IO2}}$		A4		Input switches select } I/O address decoding signals
$\overline{\text{IOA}}$		A4		Display select
$\overline{\text{NOT TRIG'D}}$		A4		Control for NOT TRIG'D lamp
	OFFA	A202	A21	Slider of channel A OFFSET control
	OFFB	A202	A21	Slider of channel B OFFSET control
	POSØ	A202	A20	Slider of ACCU position control
	POS1	A202	A20	Slider of STO1 position control
	POS2	A202	A20	Slider of STO2 position control
	POS3	A202	A20	Slider of STO3 position control
$\overline{\text{REM}}$		A4		Control for REMOTE lamp
$\overline{\text{RUNL}}$		A4		Control for RUN lamp
$\overline{\text{RD}}$		A4		Signal READ from microprocessor
$\overline{\text{WR}}$		A4		Signal WRITE from microprocessor
	XMAG	A202	A20	Slider of XMAGN control
	XPOS	A202	A20	Slider of X POSITION control
+5 V		A15		
−12 K		A15		
+12 K		A15		
−12 L		A15		
+12 L		A15		
⏚		A15		

TEST POINTS	
X248	DØ
X249	D1
X251	D4
X252	D5



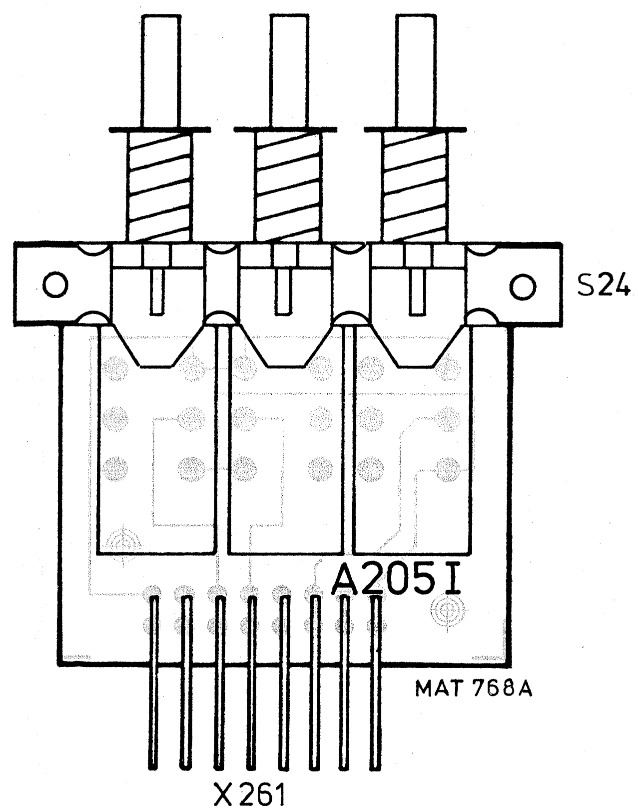
INTERCONNECTION BOARD

Fig. 6.2.5.



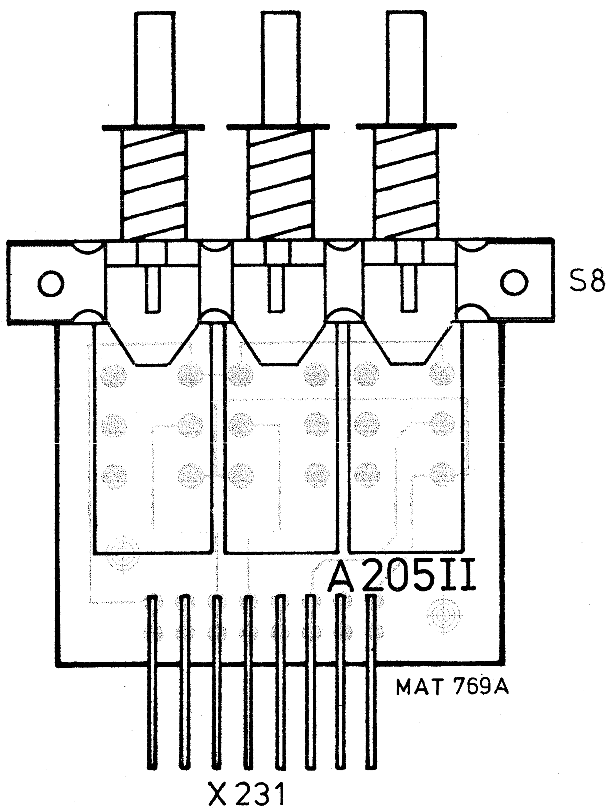
DISPLAY SWITCH BOARD

Fig. 6.2.6.



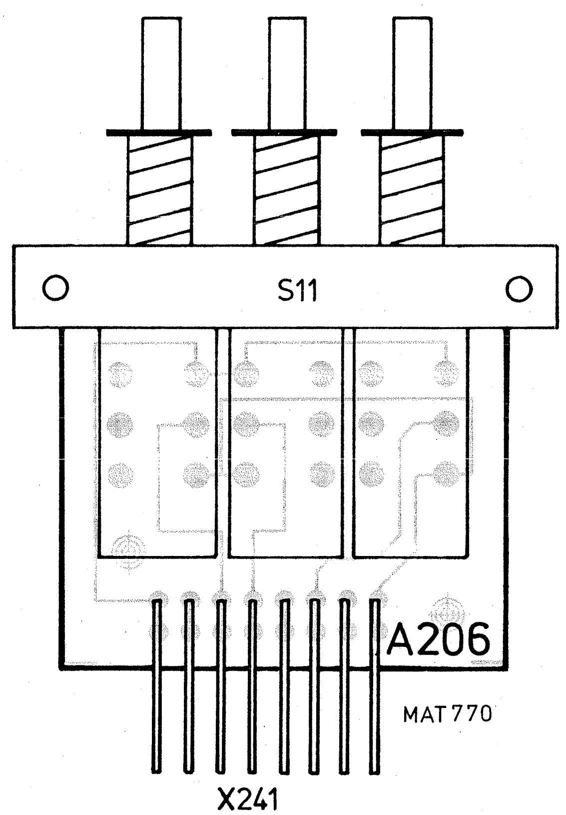
DELAY SWITCH BOARD

Fig. 6.2.7.



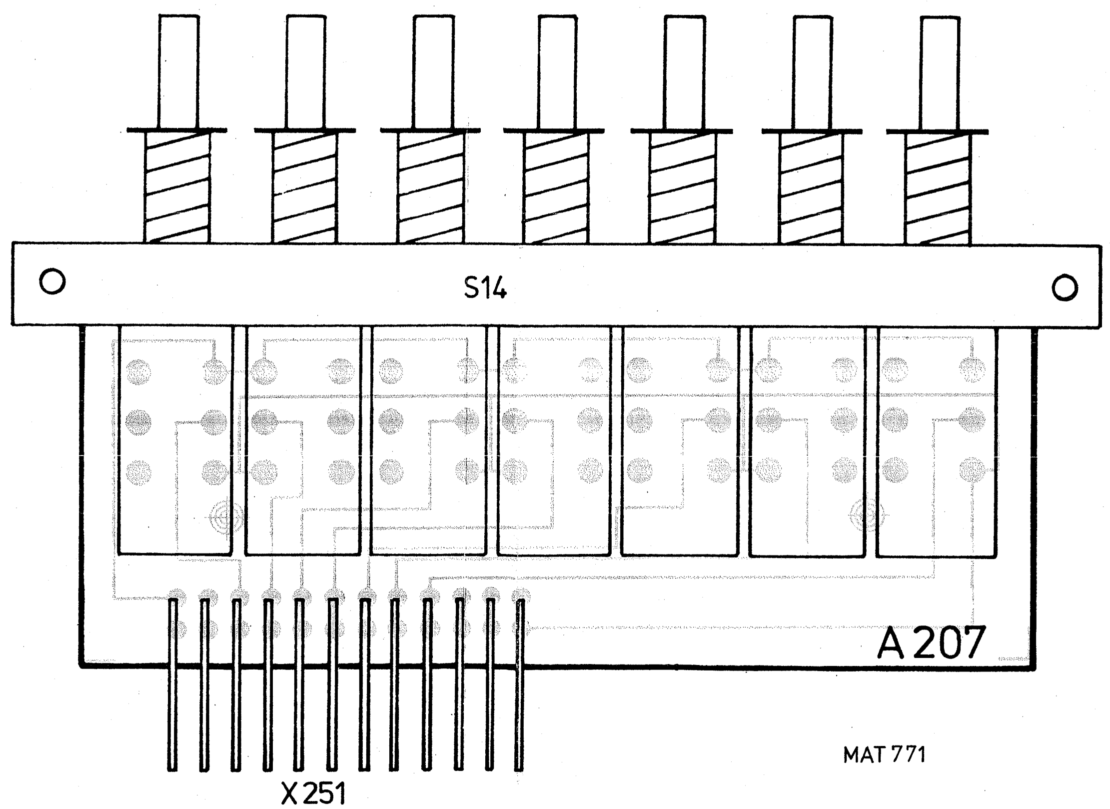
SAVE SWITCH BOARD

Fig. 6.2.8.



CLEAR SWITCH BOARD

Fig. 6.2.9.



SCALE SWITCH BOARD

Fig. 6.2.10.

SWITCH BOARD A 202

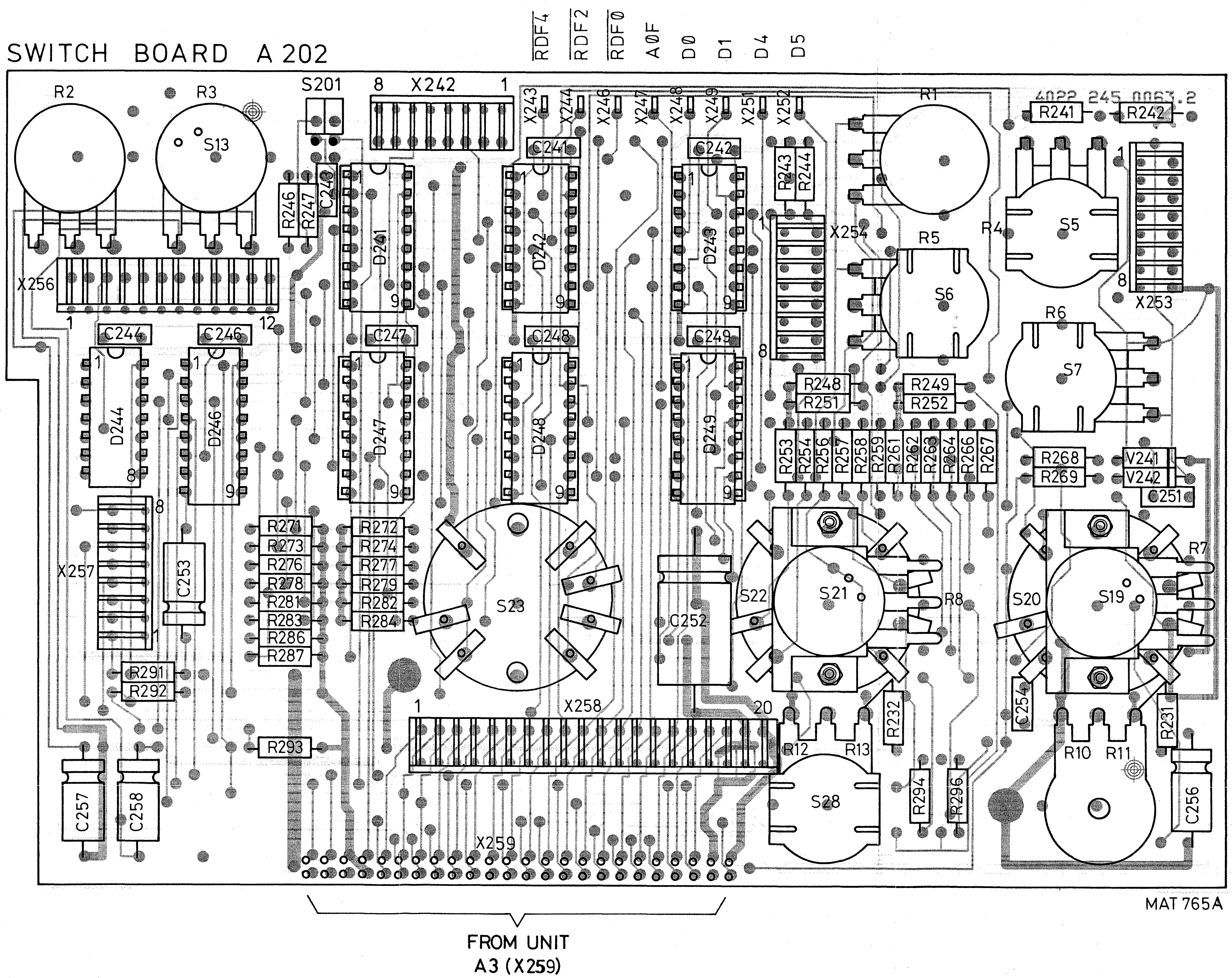


Fig. 6.2.11.

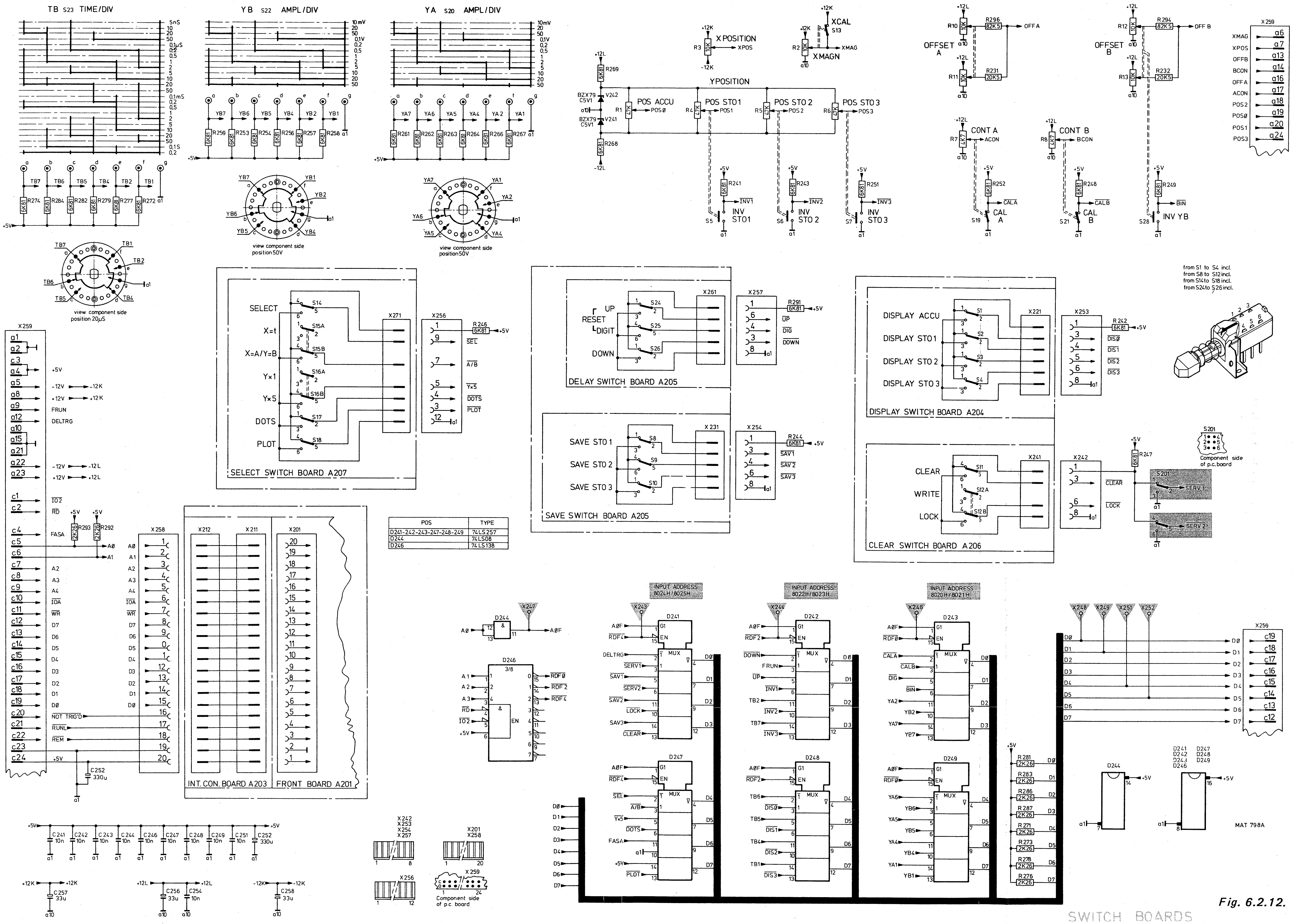


Fig. 6.2.12.

SWITCH BOARDS

6.2.3. Motherboard unit A3

The motherboard unit is installed to interconnect the various plug-in units. No components are mounted on this board.

MOTHERBOARD UNIT A3

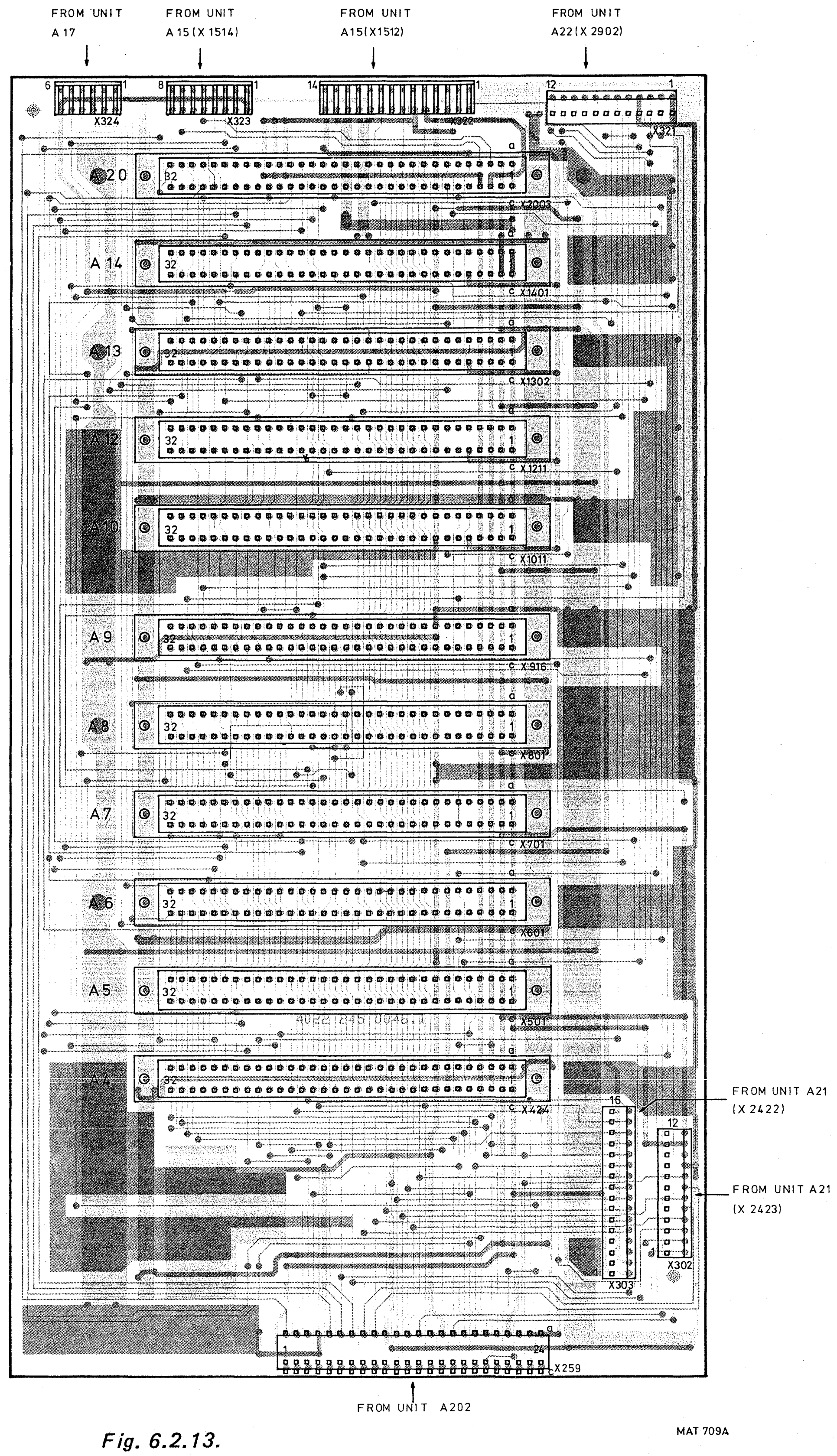


Fig. 6.2.13.

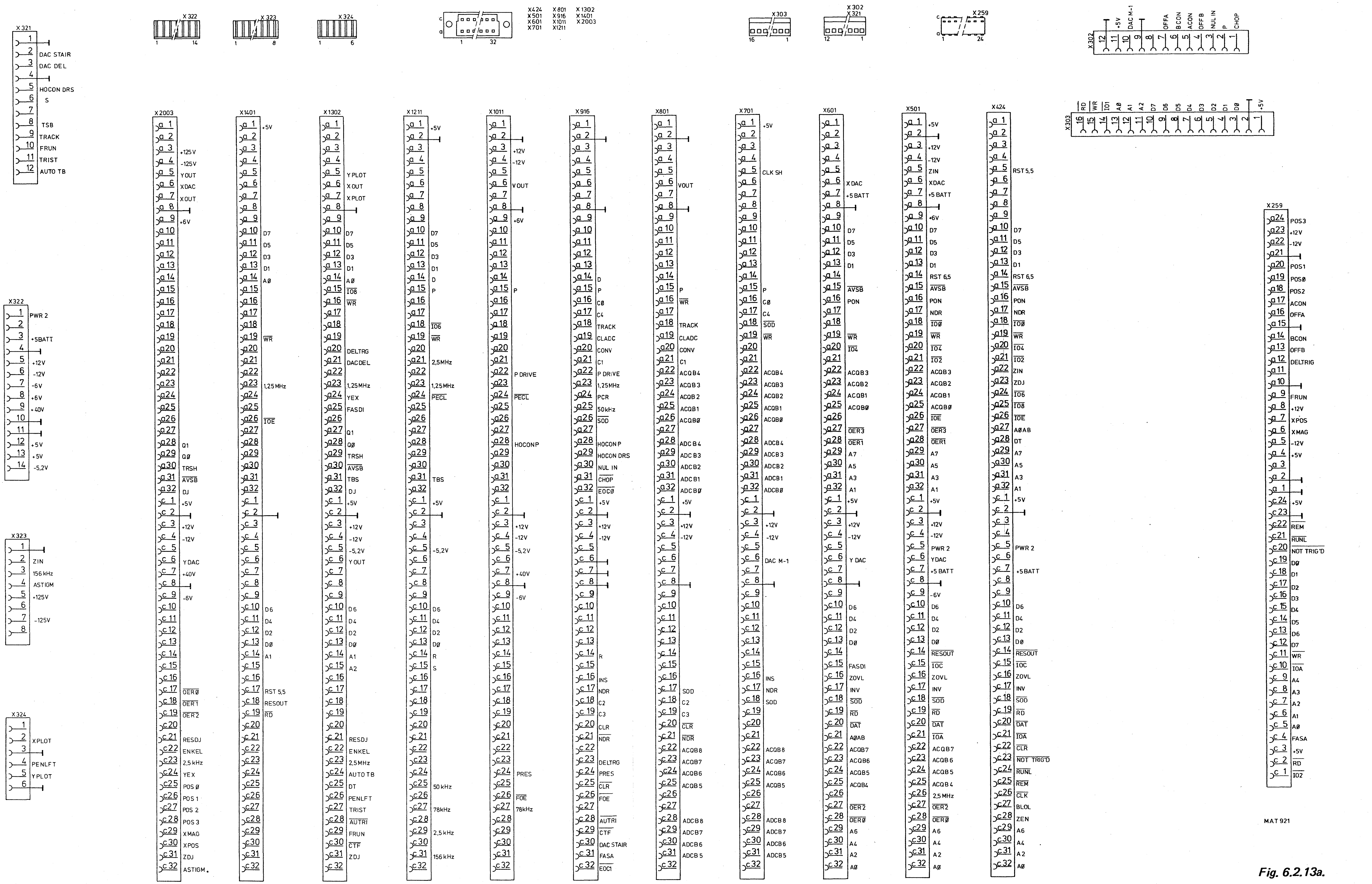

X 321
X 322
X 323
X 324
X424 X501 X601 X701 X801 X916 X1011 X1211 X1302 X1401 X2003
X 303
X 302
X 259
X2003
X1401
X1302
X1211
X1011
X916
X801
X701
X601
X501
X424
MAT 921

Fig. 6.2.13a.

6.2.4. Microprocessor unit A4

6.2.4.1. General

As shown in the simplified block diagram, the microprocessor unit basically consists of the following circuit elements:

- A microprocessor integrated circuit block for controlling and organising data flow.
- Erasable and programmable read-only memories (EPROMs) for system programming.
- Random-access memories (RAMs) for stacking and storing the variable data.
- Address and data selection latches for the multiplexed address bus.
- Decoders for RAM and ROM selection and address decoding.
- Trap and watchdog circuits to guard against loss of data.
- Two-way buffer circuit to the system data-bus.
- A blanking circuit for the c.r.t.

The heart of the microprocessor unit is integrated circuit D408, an 8-bit microprocessor type 8085 with 16 address lines.
The first eight address lines AØ ... A7 are multiplexed with the eight data lines DØ ... D7 and are defined as ADØ ... AD7. Addressing is selected by the ALE (address latch enable) signal from the microprocessor, which gives an external indication when address information is on the bus-lines.

6.2.4.2. Trap Input Circuit

The TRAP input is effective when the battery back-up facility is used. It prevents the RAM contents being disturbed when the instrument is switched off or in the event of a power failure. The TRAP input can be regarded as a non-maskable restart input. A logic 1 level on this input forces the microprocessor to continue with the execution of the program starting at address ØØ24H, the starting address of the POWER DOWN routine.

The signal PWR (power), a 50Hz sinewave signal generated on the power supply unit, is converted to a 50Hz squarewave voltage on pin 3 of Schmitt trigger D426 and integrated by C437/R412 to provide pulses on input 11 of the retriggerable one-shot D424.

During the initial switching-on of the power supply, a low voltage on reset input 13 of the one-shot holds the circuit in its reset state. When the power supply is started, however, the retriggerable one-shot switches over and signal PON (power on) goes to logic 1. As long as pulses are generated on input 12, the one-shot will remain in this state.

Failure of the power supply, i.e. no control pulses on input 11, causes the one-shot to be reset and thus activate the TRAP input of the microprocessor.
For test procedures, the circuit can be isolated by unsoldering the spot on the printed-circuit track.

6.2.4.3. CLOCK inputs X_1 and X_2

A 5 MHz crystal, B401, is connected to the clock inputs X_1 and X_2 of the microprocessor to provide an accurate timing reference source.

6.2.4.4. $\overline{\text{RESIN}}$ input and WATCHDOG Circuit

A reset signal is generated when the instrument is switched ON. This reset signal forces the microprocessor to start the execution of the main program beginning at the address ØØØØH.

The retriggerable one-shot D424 is initially reset by input pin 3 (R) during the switching-on of the instrument. After switching on, the one-shot is set to the logic 1 state by the DT (display timing) pulses from the display timing flip-flop D409, pin 9 on this p.c. board, applied to D424-5.

The one-shot remains in this state as long as the system continues to generate DT pulses.

If these pulses are interrupted, the circuit functions as a watchdog and resets the microprocessor. The one-shot will in fact be reset to logic 0 and a 1 Hz Schmitt oscillator consisting of C432/V402/R421 and D426 will switch the $\overline{\text{RESIN}}$ input of the microprocessor between logic 0 and logic 1.

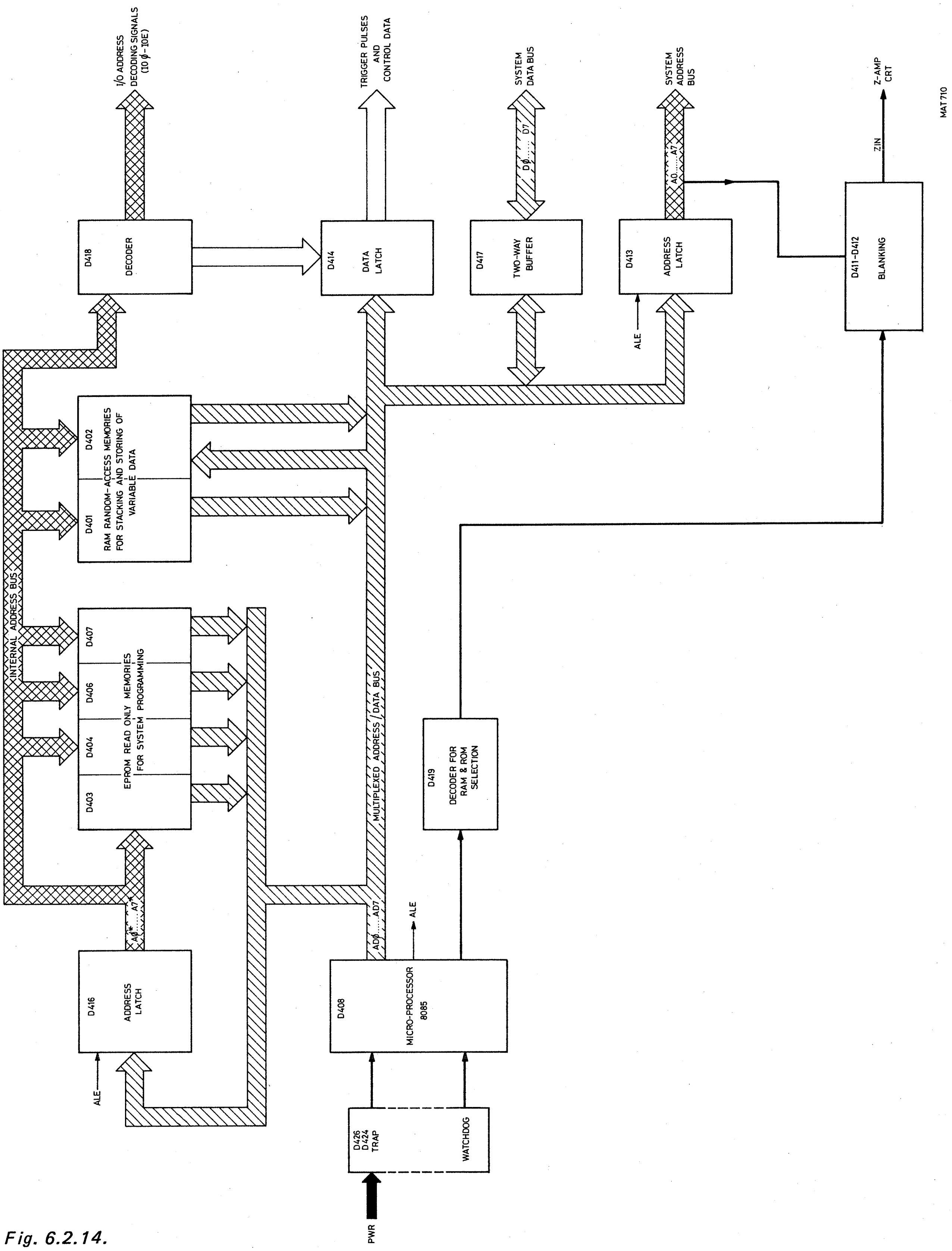

I/O ADDRESS
DECODING SIGNALS
(IO Ø-IOE)
TRIGGER PULSES
AND
CONTROL DATA
SYSTEM
DATA BUS
SYSTEM
ADDRESS
BUS
Z-AMP
CRT
MAT 710
ZIN
DØ D7
A0 ...... A7
D418
DECODER
D414
DATA
LATCH
D417
TWO-WAY
BUFFER
D413
ADDRESS
LATCH
ALE
D411-D412
BLANKING
D402
D401
RAM RANDOM-ACCESS MEMORIES
FOR STACKING AND STORING OF
VARIABLE DATA
INTERNAL ADDRESS BUS
D407
D406
D404
D403
EPROM READ ONLY MEMORIES
FOR SYSTEM PROGRAMMING
MULTIPLEXED ADDRESS / DATA BUS
D419
DECODER FOR
RAM & ROM
SELECTION
AØ A7
AD0 ...... AD7
ALE
D416
ADDRESS
LATCH
ALE
D408
MICRO-PROCESSOR
8085
D426
D424
TRAP
WATCHDOG
PWR

Fig. 6.2.14.

This reset process continues unless the program resumes correct running.

For test purposes, the watchdog circuit can be replaced by a fixed reset circuit by soldering the spot on the printed-circuit track.

6.2.4.5. *RST 7.5 – RST 6.5 – RST 5.5 inputs*

These restart inputs to the microprocessor force it to continue the program on defined addresses, from where it can jump to different programs.

RESTART INPUTS	PRIORITY	RESTART ADDRESS	REMARKS
RS 7.5	Highest	ØØ3CH	Not used in standard instruments (can eventually be used for test purposes)
RS 6.5		ØØ34H	Not used in standard instruments (connected to 'SPARE' connector)
RS 5.5	Lowest	ØØ2CH	Used by IEC-bus interface option

6.2.4.6. *SID (Serial data input)*

The microprocessor will receive the information NDR (new data ready) on the SID input.

6.2.4.7. *READY input*

Via this input, additional WAIT states are generated to double the $\overline{\text{RD}}$* and $\overline{\text{WR}}$* pulse duration. This is necessary to provide correct adaption between the microprocessor and the slower acting data RAM circuits.
The length of the signals $\overline{\text{RD}}$* and $\overline{\text{WR}}$* is doubled by flip-flop D423 only when signal $\overline{\text{DAT}}$ is logic 0.
The output of this flip-flop D423 is connected to the microprocessor READY input to indicate the end of the wait time.

6.2.4.8. *Connection to the system address bus*

The first eight address bits placed by the microprocessor on the multiplexed address-data bus lines ADØ ... AD7 have to be separated from the eight data bits. This separation is achieved by address latch D413, which is enabled by signal ALE.
The group of output signals AØ ... A7 constitute the system address bus.

6.2.4.9. *Connection to the system data-bus*

The eight data bits placed by the microprocessor on the multiplexed address-data bus lines ADØ ... AD7 have to be separated from the first eight address bits.
This separation is done by the bidirectional buffer D417.
This buffer is selected if address line A15 is logic 1 (as in I/O and DATA part of the memory map).
Input or output data depends on the logic level of signal RD*.

RD* = logic 1 means OUTPUT
RD* = logic 0 means INPUT

Data is transported between the D417 in- and outputs and the system data-bus over the lines DØ ... D7.

SYSTEM MEMORY MAP

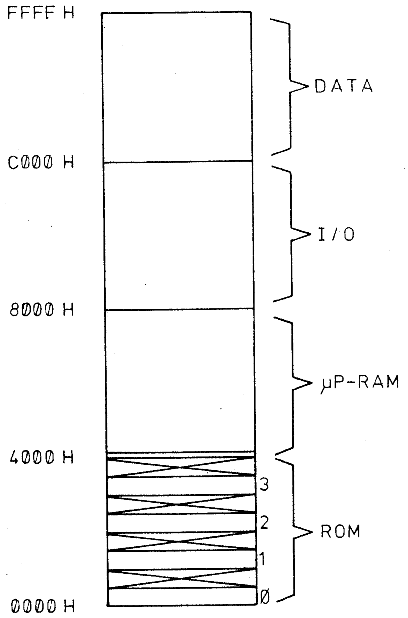


Fig. 6.2.15.

MAT 832

ADDRESS DECODING

6.2.4.10. ROM - μP/RAM - I/O - DATA selection

In decoder D419, four select signals are generated as follows:

A15	A14	OUTPUT SIGNAL
0	0	ROM selection to pin 15 - D419
0	1	μPRAM selection signal $\overline{\text{UPR}}$
1	0	I/O selection signal (not used)
1	1	DATA SELECTION SIGNAL $\overline{\text{DAT}}$

ROM chip select signals ROMØ ... ROM3

A15	A14	A13	A12	OUTPUT SIGNAL	ADDRESSES
0	0	0	0	$\overline{\text{ROMØ}}$	ØØØØ - Ø7FF
0	0	0	1	$\overline{\text{ROM1}}$	1ØØØ - 17FF
0	0	1	0	$\overline{\text{ROM2}}$	2ØØØ - 27FF
0	0	1	1	$\overline{\text{ROM3}}$	3ØØØ - 37FF

I/O select signals $\overline{\text{IOØ}}$ ... $\overline{\text{IOE}}$.

The three-bit decoder D418 decodes the address bits A15, A14, A7*, A6* and A5* into the eight address decoding signals $\overline{\text{IOØ}}$ ... $\overline{\text{IOE}}$. Each of these signals represent a group of addresses as shown in the table. The signals are used in various circuits of the instrument.

A15	A14	A7*	A6*	A5*	OUTPUT SIGNAL	ADDRESSES
1	0	0	0	0	$\overline{\text{IOØ}}$	8ØØØ - 8Ø1F
1	0	0	0	1	$\overline{\text{IO2}}$	8Ø2Ø - 8Ø3F
1	0	0	1	0	$\overline{\text{IO4}}$	8Ø4Ø - 8Ø5F
1	0	0	1	1	$\overline{\text{IO6}}$	8Ø6Ø - 8Ø7F
1	0	1	0	0	$\overline{\text{IO8}}$	8Ø8Ø - 8Ø9F
1	0	1	0	1	$\overline{\text{IOA}}$	8ØAØ - 8ØBF
1	0	1	1	0	$\overline{\text{IOC}}$	8ØCØ - 8ØDF
1	0	1	1	1	$\overline{\text{IOE}}$	8ØEØ - 8ØFF

ROM MEMORY

The ROM (read-only memory), which contains the system program, consists of the four EPROM chips D403 - D404 - D406 and D407 and 2K-bytes each (2048X 8 bits).

Because the microprocessor's first eight address lines ADØ ... AD7 are multiplexed in the microprocessor with the data lines, the addresses have to be latched by the address latch D416 with the aid of the ALE signal. The ALE signal enables the latching of the AØ* ... A7* signals. These AØ* ... A7* signals are placed on the microprocessor board internal address bus.

Each ROM memory address can be selected by the address lines AØ* ... A7* together with address lines A8 - A9 and A10.

Each ROM memory chip is selected by the read signal $\overline{\text{RD}}$* and the relevant ROM selection signal $\overline{\text{ROMØ}}$, $\overline{\text{ROM1}}$, $\overline{\text{ROM2}}$ or $\overline{\text{ROM3}}$.

When a certain ROM address is selected in this way, the contents of the selected location are placed on the multiplexed address-data bus lines ADØ ... AD7.

μP-RAM MEMORY

The μP-RAM (microprocessor random access memory) is used by the microprocessor for stack purposes and for storage of variable data.
It consists of two RAM chips D401 - D402 of ¼K-nibbles each (256 x 4 bits), which means that a maximum of 256 bytes of data can be stored.

Each μP-RAM memory address can be selected by the address lines AØ* ... A7*.
The two chips are selected by the signal combination PON.UPR.

Reading the RAM contents or writing data into a RAM location is controlled by the signals $\overline{\text{RD}}$* and $\overline{\text{WR}}$*.

The data to be written into, or read from the RAM memory is transported via the multiplexed address-data bus ADØ ... AD7.

DATA LATCH D414

When the microprocessor places the address 8Ø2Ø on the multiplexed address data bus, this results in signal $\overline{\text{IO2}}$ going to logic 0. This $\overline{\text{IO2}}$ combined with the $\overline{\text{WR}}$ signal on gate D421 enables data latch D414 to latch the byte of data present on the multiplexed address data-bus.

The byte of data consists of the following signals:

BIT Ø	$\overline{\text{CLR}}$	Clear signal for clearing the shift register
BIT 1	$\overline{\text{REM}}$	Control signal for REMOTE lamp
BIT 2	$\overline{\text{NOT TRIG'D}}$	Control signal for NOT TRIG'D lamp
BIT 3	$\overline{\text{ZEN}}$	Z enable signal
BIT 4	$\overline{\text{RUNL}}$	Control signal for RUN lamp
BIT 5	BLOL	Blinking overload signal
BIT 6	INV	Invert signal for RAM output data
BIT 7	CLDT	Clear display timing flip-flop

BLANKING CIRCUIT

This circuit provides for a blanking signal ZIN (Z-amplifier input) for blanking the trace on the c.r.t. display.

ZIN = logic 1 means blanking.

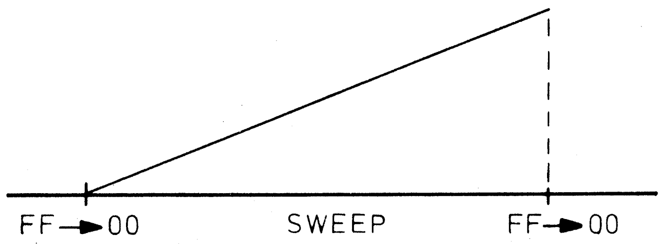
The trace on the c.r.t. display is only present if all the input signals of NAND circuit D411 are logic 1 at the same time.

– pin 4 The signal ZEN is only present during the time that a selected memory (ACCU, STO1, STO 2 or STO3) is displayed.

– pin 11 If an overflow is detected on the RAM unit the short signal ZOVL (Z-overflow), will be latched in a D-type flip-flop D423 with the clock signal DAT.WR.
As the output signal of the flip-flop is connected to OR circuit D421, the blinking overload signal is passed to pin 11 of the NAND D411, resulting in blinking of the trace at a low frequency.

– pin 3 In mode DOTS, the ZDJ (Z dot join) blinking signal will be active.

– pin 5 Signal DT (display timing) blanks the trace when no memory contents (ACCU, STO1, STO2 or STO3) are displayed. Signal DT is derived from the addresses, which are also applied to the XDAC for horizontal deflection.



NAND circuit D412 detects the address FFH on the first eight address lines.
The output signal indicates the beginning and the end of a sweep by going to logic 1 level. This signal is latched in D-type flip-flop D409 with the clock signal DAT.WR, resulting in a signal DT.
The trace is blanked if DT = logic 0. Flip-flop D409 can be reset by signal CLDT (clear display timing flip-flop) resulting in a blanked trace.

– pin 1 In mode X = A/Y = B (A versus B – AVSB)
a signal ZAB is generated on output pin 5 of flip-flop D409.
Data can only be latched in this flip-flop on clock signal DAT.WR.
This data is derived from signal AØAB.
(AØAB is address AØ in mode X = A/Y = B)

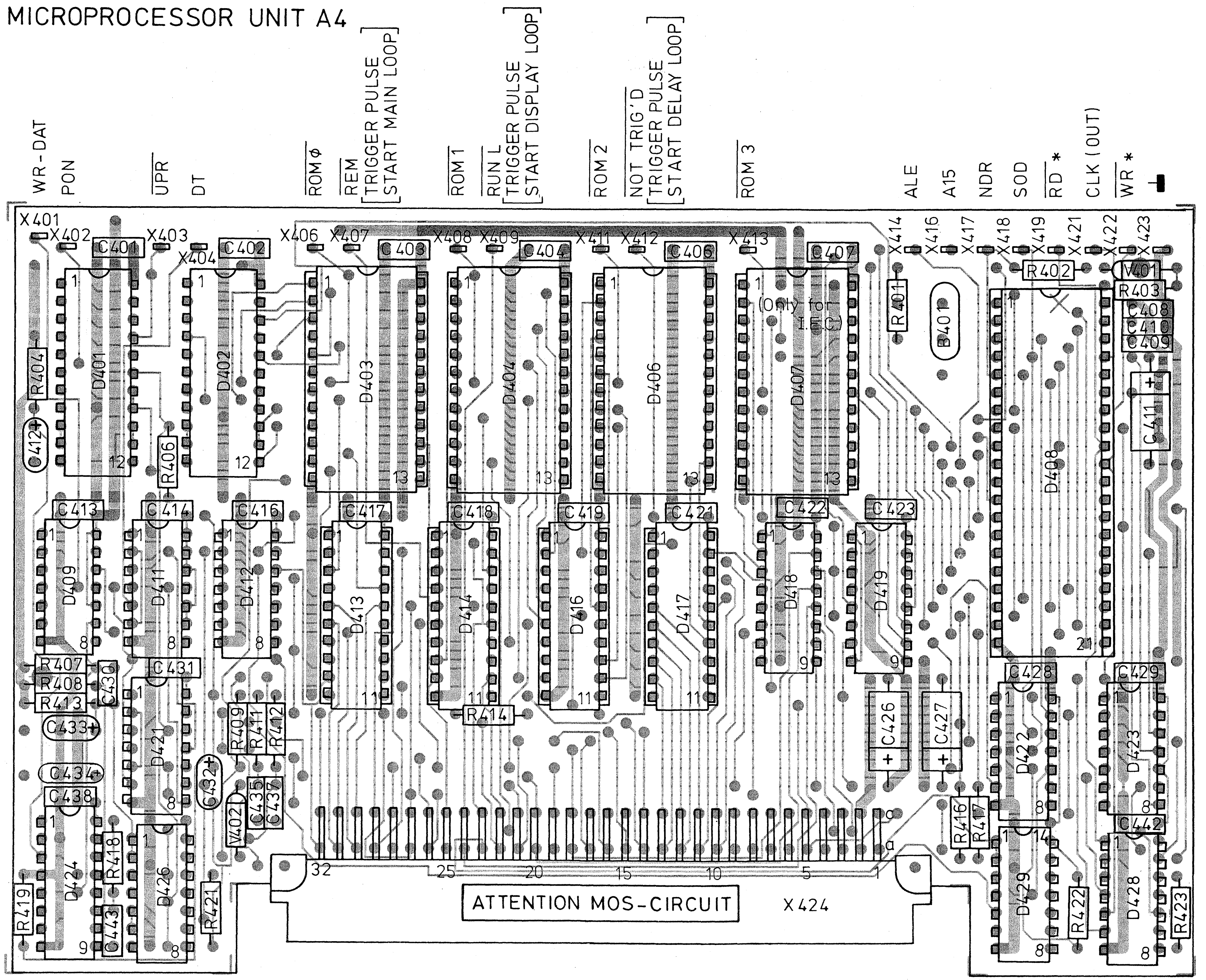
TRIGGER PULSES FOR TEST PURPOSES

Trigger pulse 'START MAINLOOP' is available at X407
Trigger pulse "START DISPLAY LOOP" is available at X409
Trigger pulse 'START DELAY LOOP' is available at X412

INCOMING SIGNAL	OUTGOING SIGNAL	GENERATED ON UNIT	USED ON UNIT	DESCRIPTION	
	AØ ... A7	A4		Address bits from system address bits	
AØAB		A6		Address bit AØ in X = A/Y = B mode	
$\overline{\text{AVSB}}$		A13	A6	Logic 0 in X = A/Y = B mode	
	BLOL	A4		Blinking overload	
	$\overline{\text{CLK}}$	A4		Microprocessor clock pulse output signal (2,5 MHz)	
	$\overline{\text{CLR}}$	A4	A8–A9	Clear signal for shift register	
DØ ... D7	DØ ... D7	A4-A6		Data bits from system data-bus	
	$\overline{\text{DAT}}$	A4	A6	Data selection	
	DT	A4	A13	Display timing	
	INV	A4	A6	Signal invert	
	$\overline{\text{IOØ}}$	A4	A21	Input switches select amplifier settings (A21)	I/O address decoding signals.
	$\overline{\text{IO2}}$	A4	A202	Input switches select (A2) Output port select (A4)	
	$\overline{\text{IO4}}$	A4	A6	Data RAM select (A6)	
	$\overline{\text{IO6}}$	A4	A12	Time-base select (A12)	
	$\overline{\text{IO8}}$	A4	A13	Delay trigger unit settings (A13)	
	$\overline{\text{IOA}}$	A4	A201/A202	Display select (A2)	
	$\overline{\text{IOC}}$	A4	NOT USED		
	$\overline{\text{IOE}}$	A4	A14		
NDR		A9		New data ready	
	$\overline{\text{NOT TRIG'D}}$	A4	A201/A202	Control for NOT TRIG'D lamp	
	PON	A4	A6	Power on	
PWR		A15		Power signal (20 kHz)	
	$\overline{\text{RD}}$	A4		Signal READ from microprocessor	
	$\overline{\text{REM}}$	A4	A201/A202	Control for REMOTE lamp	
	$\overline{\text{RESOUT}}$	A4	A14	Microprocessor RESET OUTPUT signal	
RST5,5		A14		Restart 5,5 input from IEC-bus interface	
RST6,5		A5		Restart 6,5 input (not used)	
	$\overline{\text{RUNL}}$	A4	A201/A202	Control for RUN lamp	
	$\overline{\text{SOD}}$	A4	A6–7–9	Microprocessor serial output data	
	$\overline{\text{WR}}$	A4		Signal WRITE from microprocessor	
ZDJ		A13		Z dot join	
	ZEN	A4		Z enable	
	ZIN	A4	A15	Z input	
ZOVL		A6		Z overflow signal	
+5 V		A15			
⏚		A15			
+5 BATT		A15			

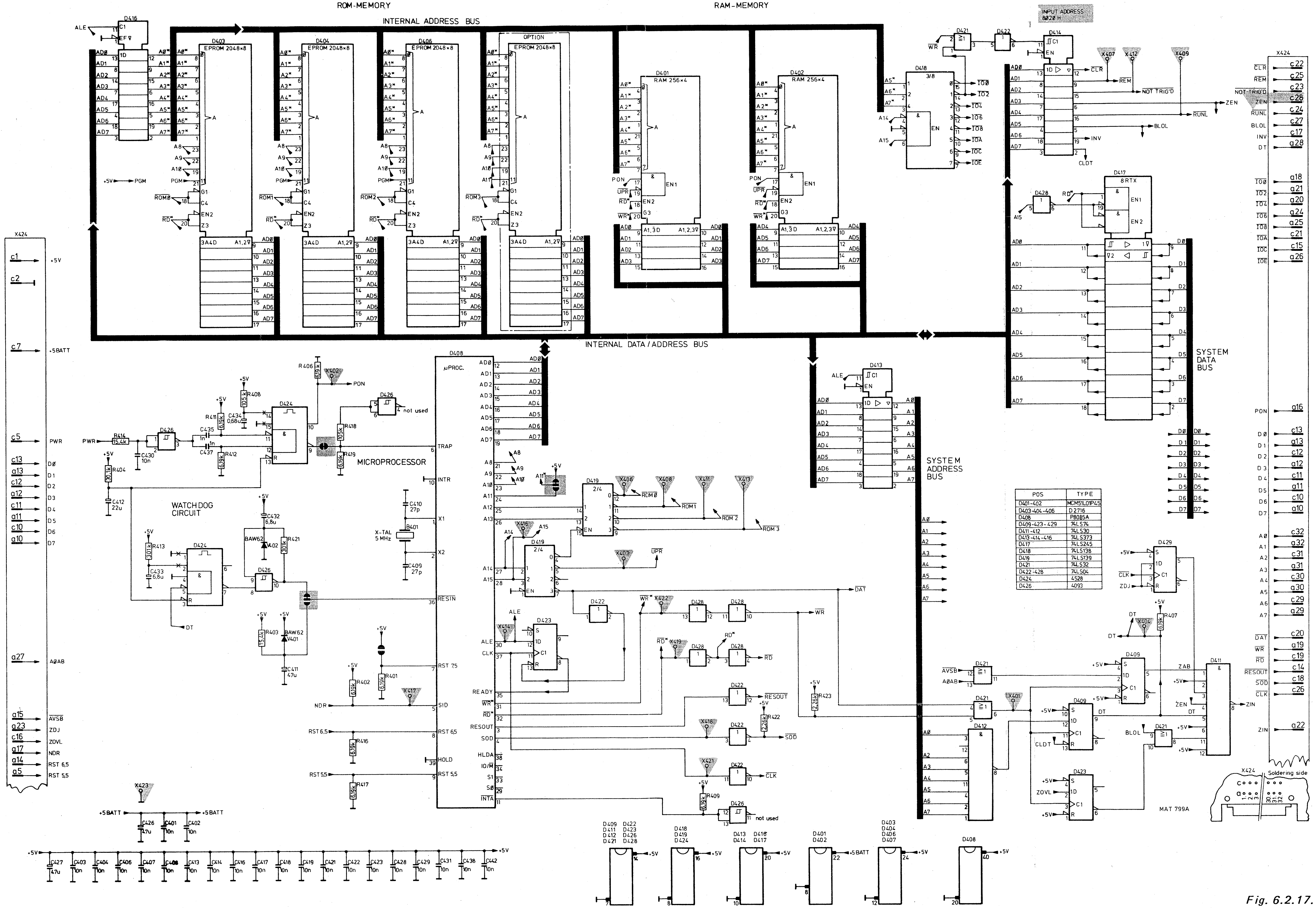
TEST POINTS	
X401	D421-pin 6 (WR.DAT)
X402	PON
X403	$\overline{\text{UPR}}$
X404	DT
X406	$\overline{\text{ROMØ}}$
X407	$\overline{\text{REM}}$
X408	$\overline{\text{ROM1}}$
X409	$\overline{\text{RUNL}}$
X411	$\overline{\text{ROM2}}$
X412	$\overline{\text{NOT TRIG'D}}$
X413	$\overline{\text{ROM3}}$
X414	ALE
X416	A15
X417	NDR
X418	SOD
X419	$\overline{\text{RD}}$*
X421	CLK (OUT)
X422	$\overline{\text{WR}}$*
X423	

MICROPROCESSOR UNIT A4



MAT 772A

Fig. 6.2.16.



POS	TYPE
D401-402	MCM51L01P45
D403-404-406	D 2716
D408	P8085A
D409-423-429	74LS74
D411-412	74LS30
D413-414-416	74LS373
D417	74LS245
D418	74LS138
D419	74LS139
D421	74LS32
D422-428	74LS04
D424	4528
D426	4093

Fig. 6.2.17.

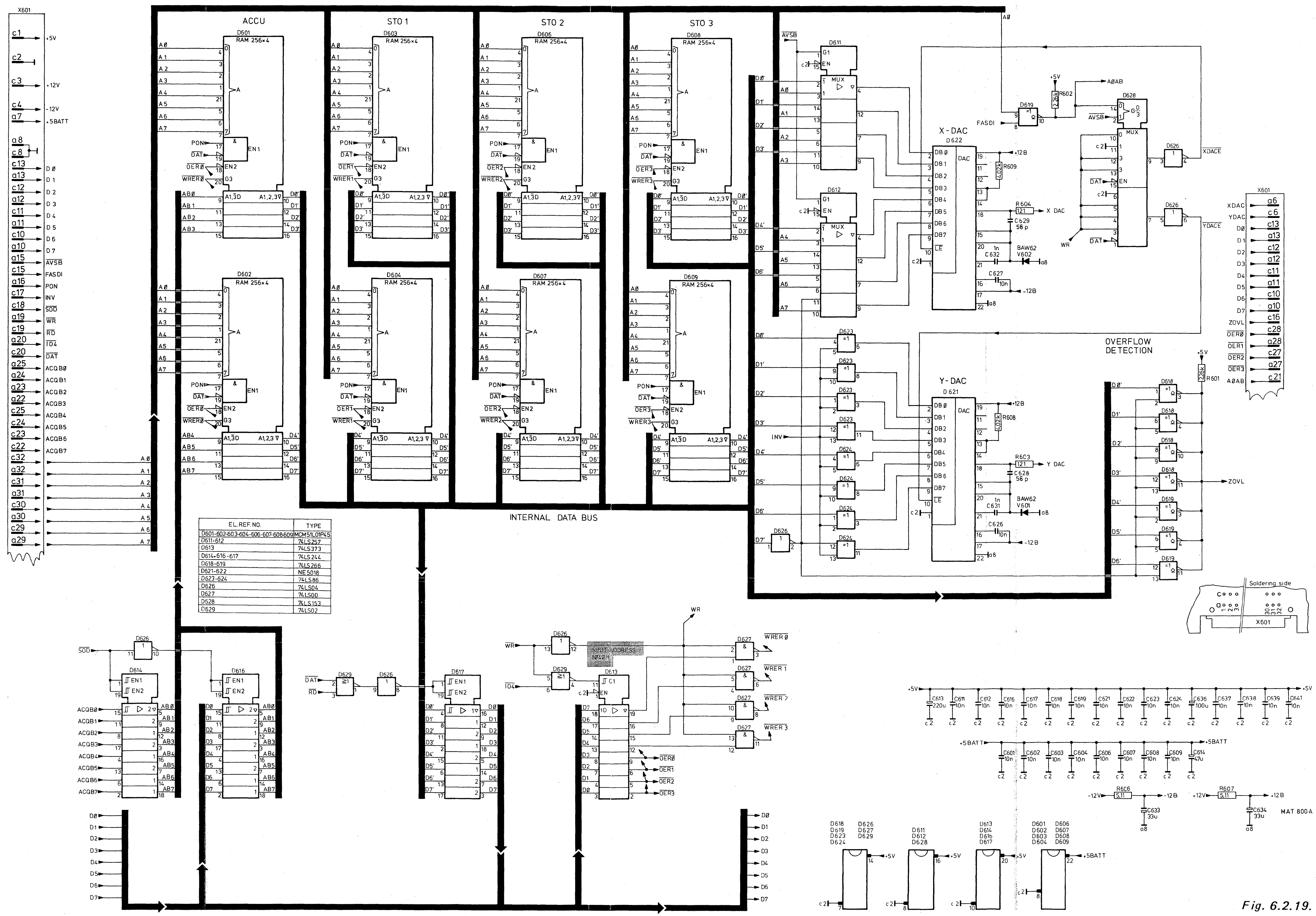
A4 MICRO PROC. UNIT

6.2.5. Spare unit A5

There is a connector X501 available on the motherboard unit A3 in which no plug-in unit is placed.

On this connector X501 a number of signals are available for measuring purposes.

A1	+5 V	C1	+5 V
A2	0 V	C2	0 V
A3	+12 V	C3	+12 V
A4	−12 V	C4	−12 V
A5	ZIN	C5	PWR2
A6	XDAC	C6	YDAC
A7	+5 BATT	C7	+5 BATT
A8	0 V	C8	0 V
A9	+6 V	C9	−6V
A10	D7	C10	D6
A11	D5	C11	D4
A12	D3	C12	D2
A13	D1	C13	DØ
A14	$\overline{\text{RST 6.5}}$	C14	$\overline{\text{RES OUT}}$
A15	$\overline{\text{AVSB}}$	C15	$\overline{\text{IOC}}$
A16	PON	C16	ZOVL
A17	$\overline{\text{NDR}}$	C17	$\overline{\text{INV}}$
A18	$\overline{\text{IOØ}}$	C18	$\overline{\text{SOD}}$
A19	$\overline{\text{WR}}$	C19	$\overline{\text{RD}}$
A20	$\overline{\text{IO4}}$	C20	$\overline{\text{DAT}}$
A21	$\overline{\text{IO2}}$	C21	$\overline{\text{IOA}}$
A22	ACQB3	C22	ACQB7
A23	ACQB2	C23	ACQB6
A24	ACQB1	C24	ACQB5
A25	ACQBØ	C25	ACQB4
A26	$\overline{\text{IOE}}$	C26	2,5 MHz
A27	$\overline{\text{OER3}}$	C27	$\overline{\text{OER2}}$
A28	$\overline{\text{OER1}}$	C28	$\overline{\text{OERØ}}$
A29	A7	C29	A6
A30	A5	C30	A4
A31	A3	C31	A2
A32	A1	C32	AØ



EL.REF.NO.	TYPE
D601-602-603-604-606-607-608-609	MCM51L01P45
D611-612	74LS257
D613	74LS373
D614-616-617	74LS244
D618-619	74LS266
D621-622	NE5018
D623-624	74LS86
D626	74LS04
D627	74LS00
D528	74LS153
D629	74LS02

Fig. 6.2.19.

A6 RAM UNIT

6.2.7. Buffer unit A7

6.2.7.1. General

The buffer unit consists of a 9-bit x 256 digital shift register for data storage and a digital-to-analog converter DAC M-1, which re-converts the digital output signals from the ADC for the correction of subsequent analog signals.

Analog information from the acquisition section of the oscilloscope is converted into a 9-bit digital value ADCBØ ... ADCB8 on the conversion unit. After conversion and final correction, these signal bits are shifted into the 9-bit x 256 digital shift register D701 ... D711 on this buffer unit, for storage.
The contents of this shift register are only shifted under the control of a clock signal CLKSH, generated in D718, D719.

$$CLKSH = \overline{(\overline{INS.NDR}) + (SOD.WR)}$$

Shifting can be interrupted therefore by blocking signal CLKSH.

The nine shift register output signals will only be applied to the ACQB bus in the P^2CCD-mode (signal P = logic 1) for correction purposes or if signal NDR = logic 1 (new data is available).
Data is applied to the ACQB bus via the 3-state non-inverting buffers D716 and D717.

6.2.7.2. Data routeing and correction in P^2CCD mode

For details of this, refer to the Conversion Unit A8 description.

6.2.7.3. Data routeing and correction in DRS-mode

In the DRS-mode (Direct, Roll and Sample), inaccuracies of the Track/Hold circuit and the ADC circuit are corrected before the information is stored in the shift register.
The circuit is operative for dual-channel mode working, i.e. with both channel A and channel B switched on.
This mode is arranged to function automatically even if only one channel is selected.

Principle of operation

Fig. 6.2.20

To reduce errors in conversion, analog samples for digitising are compared with preceding samples, these being subtracted so that only small increments are converted to digital values in the ADC. After conversion, the digital equivalent of the original analog signal is produced by adding the differential signal from the ADC to the digital value of the preceding sample.

Referring to the block diagram, M_n is the new sample of the input signal from the acquisition system; M_{n-1} is the preceding sample, derived from the shift register and re-converted by DAC M-1 to analog form. At the input to the Track and Hold circuit, M_{n-1} is subtracted from M_n to produce a differential analog voltage, which is then converted to digital form in the ADC and added to the preceding digital value M_{n-1}.

$$\text{i.e. } (M_n - M_{n-1}) + M_{n-1} = M_n$$

EL. REF. NO.	TYPE
D701-702-703-704-706-707-708-709-711	HEF4731
D712-713	HEF4508
D714	NE 5018
D716-717	HEF40097
D718	HEF4001
D719	HEF4049

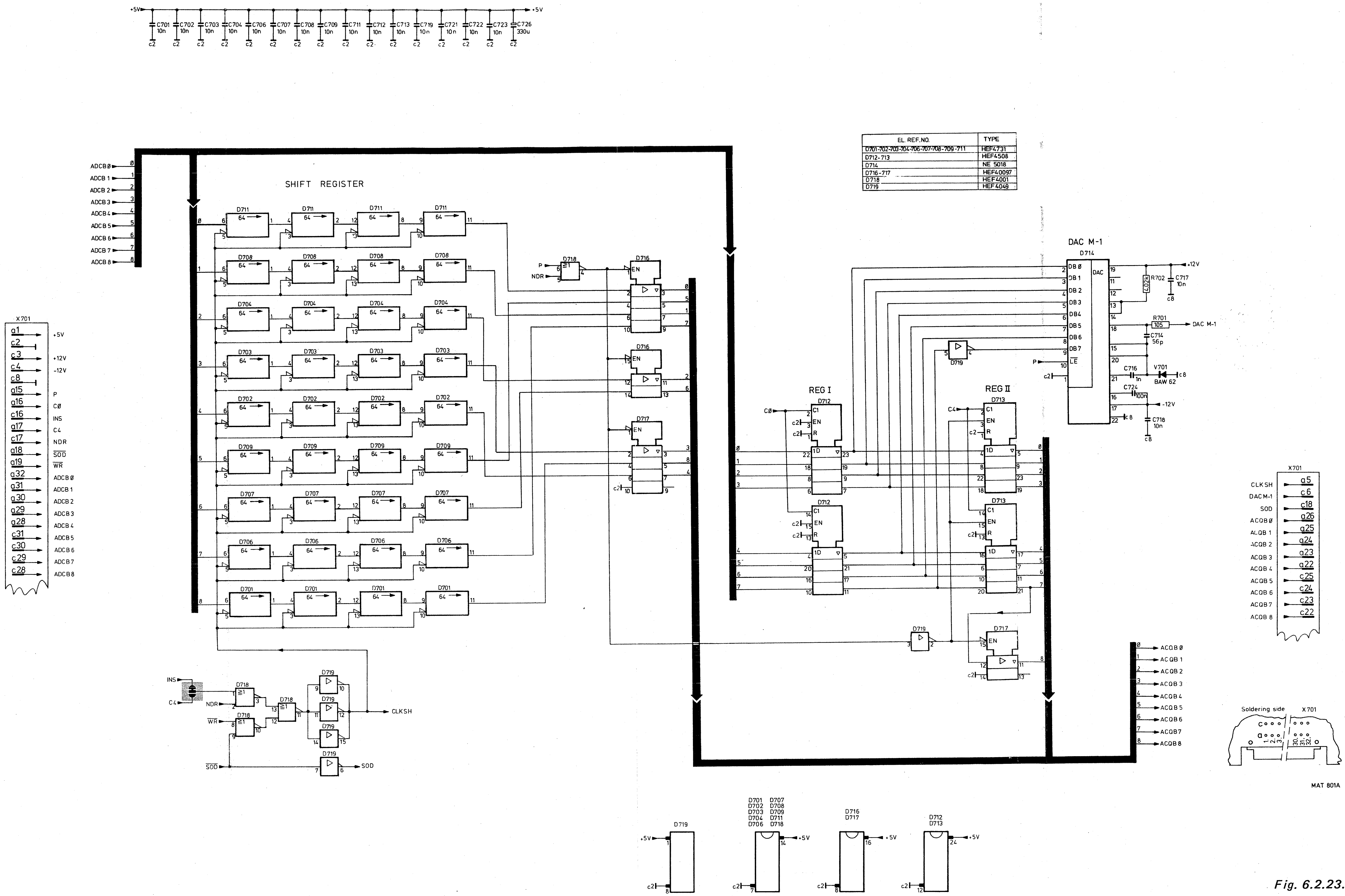


Fig. 6.2.23.

A7 BUFFER UNIT

6.2.8. Conversion unit A8

The conversion unit basically consists of an ADC for converting the input signals into digital form for storing in the shift register on the buffer unit A7, a circuit for signal zero correction, and an overflow detection and marking circuit.

These functions are performed by the following circuit blocks:

- a sample and hold circuit for analog inputs, D822
- analog-to-digital converter (ADC) D821
- AND-gates D801, D813 for controlling inputs to the adder circuit
- exclusive-OR gates D802, D814, D809 for inverting signal to adder for subtraction during correction
- adder circuit D803, D816, D804
- multiplexers D806, D807, D817, D818 on adder outputs for overflow detection, marking, etc.
- result registers D819, D811 for storing multiplexer output signals.

6.2.8.1. Sample and Hold circuit

Analog output signal VOUT from the CCD logic unit (A10), which represents the A and/or B channel input signals in one of the selected modes, is applied to input 3 of the sample and hold circuit D822. This circuit is controlled by the TRACK signal:

TRACK = logic 1 — the circuit only tracks the input signal

TRACK = logic 0 — (= HOLD) the circuit holds the input level that was present at the negative-going edge of the TRACK signal

The output signal of this sample and hold circuit D822 provides an input to the ADC that lies between +5 V and −5 V.

6.2.8.2. Analog-to-digital converter (ADC)

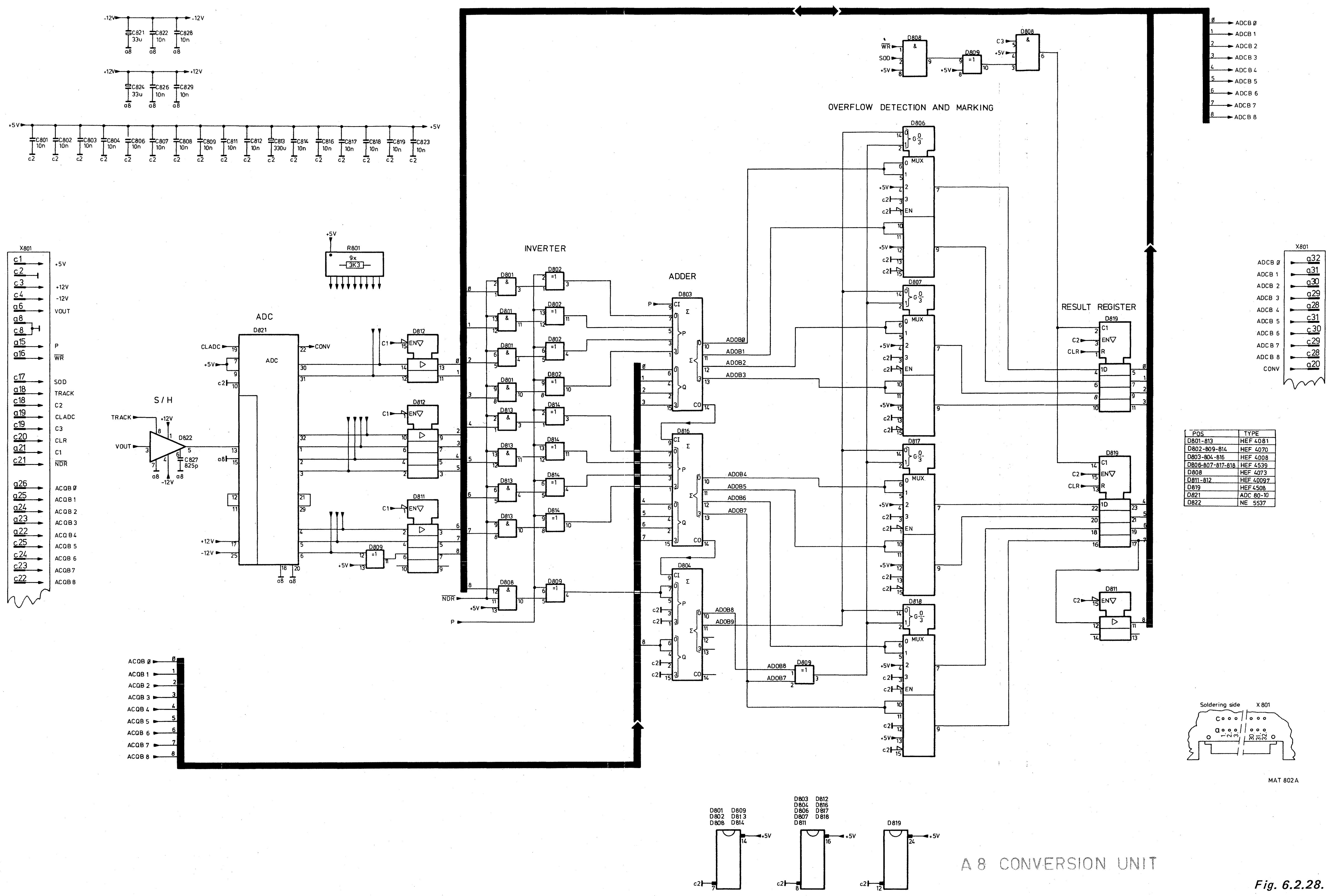
The analog input level from the sample and hold circuit is converted into a digital 9-bit number in the ADC circuit D823.
Conversion is controlled by the clock pulses CLADC. (Nine clock pulses are used to convert to this 9-bit number). As the ADC is a 10-bit type, the least-significant bit being ignored. These clock pulses are only generated by the ACL unit A9 during the period when the CONV signal (conversion) is at logic 1.

The ADC output signal CONV reverts to logic 0 at the end of the conversion period, thus indicating that conversion is complete and that the results can be fed to the ADCBØ ... ADCB8 bus via the tri-state non-inverting buffers D811, D812.

The 9-bit digital output of the ADC is straight binary coded and is converted to 2's complement notation in exclusive-OR gate D809 (11,12,13) by inverting the most-significant (9th) bit, as shown in the following table.

	STRAIGHT BINARY (9-bit) Decimal		2's COMPLEMENT (9-bit) Decimal	
−5 V	+0	0 0 0 0 0 0 0 0 0	−256	1 0 0 0 0 0 0 0 0
		0 0 0 0 0 0 0 0 1	−255	1 0 0 0 0 0 0 0 1
		0 1 0 0 0 0 0 0 0	−128	1 1 0 0 0 0 0 0 0
		0 1 1 1 1 1 1 1 1	−1	1 1 1 1 1 1 1 1 1
		1 0 0 0 0 0 0 0 0	+0	0 0 0 0 0 0 0 0 0
		1 0 1 1 1 1 1 1 1	+127	0 0 1 1 1 1 1 1 1
+5 V	+511	1 1 1 1 1 1 1 1 1	+255	0 1 1 1 1 1 1 1 1

INVERSION OF THE 9th BIT



POS	TYPE
D801-813	HEF 4081
D802-809-814	HEF 4070
D803-804-816	HEF 4008
D806-807-817-818	HEF 4539
D808	HEF 4073
D811-812	HEF 40097
D819	HEF 4508
D821	ADC 80-10
D822	NE 5537

A 8 CONVERSION UNIT

Fig. 6.2.28.

6.2.9. Acquisition control logic unit A9

6.2.9.1. General

Before discussing the timing functions in the various operating modes, the general circuit functions of the Acquisition Control Logic unit are first outlined. The ACL unit contains the timing circuits that generate the signals required to control the conversion unit (A8) and the buffer unit (A7).

A Hold and Convert pulse HOCON starts each analog-to-digital conversion of an input signal sample. In the P-mode, this is signal HOCON P from the CCD logic unit A10; in the Direct, Roll and Sampling modes, this is HOCON DRS from the trigger unit A22.
Depending on the mode selected, one of these hold and convert signal lines is applied to the clock input of D-type flip-flop D909 via multiplexer D911, pin 7. This multiplexer is controlled by the signals P and R, to give the following:

SIGNALS R	P	D911 output pin 7
0	0	HOCON DRS
0	1	HOCON P
1	0	HOCON DRS
1	1	(unavailable input signal combination)

Flip-flop D909 is switched by the HOCON pulse, resulting in the TRACK signal going to logic 0, which brings the Track and Hold circuit on the conversion unit to the HOLD state.
Analog-to-digital conversion is now started and controlled by the nine clock pulses CLADC (pin 11 of NAND-gate D906), which are derived from a 1,25 MHz clock signal. During conversion in the ADC, a signal CONV is at logic 1. After conversion, this signal goes to logic 0, indicating that conversion is finished. Output pin 6 of flip-flop D909 is now switched to 0 by the $\overline{\text{CONV}}$ signal and this zero resets the other two flip-flops in the circuit (RESET inputs D908-12, D909-13). In this way, the CONV signal blocks the CLADC pulses again and switches the TRACK signal. The track and hold circuit now returns to tracking the input signal.

The CHOP output of chopper flip-flop D908 is switched to its opposite state at the end of each conversion by signal $\overline{\text{CONV}}$ on its clock input. Only in the P-mode, where the CHOP signal is not required, is the chopper flip-flop set permanently to its '1'-state, i.e. signal CHOP is logic 1. This is achieved by a zero level on the direct set input of the flip-flop.

During each conversion, a CØ pulse on D906-8 is fed from the CONV signal to control the first buffer stage (D712 on unit A7) after the adder circuit (on unit A8). This is the buffer stage that sends its data to the digital-to-analog converter DAC (M-1).

At the completion of each ADC conversion, counter D928, which has been preset to the value 15, starts counting the 1,25 MHz pulses on its clock input.
The start of counting is initiated by the output signal of flip-flop D927, which is set to logic 1 by the positive-going edge of the $\overline{\text{CONV}}$ signal.

	OD	OC	OB	OA
15 →	1	1	1	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
15	1	1	1	1

ADOB9	ADOB8	ADOB7	MULTIPLEXER OUTPUT
0	0	0	ADDER OUTPUT
0	0	1	+127
0	1	0	+127
0	1	1	NON-EXISTING
1	0	0	COMBINATIONS
1	0	1	−128
1	1	0	−128
1	1	1	ADDER OUTPUT

In case of an overflow, signal ADOB9 indicates whether it is an overflow or an underflow. ADOB8 and ADOB7 together indicate whether there is an overflow condition.
After marking, the multiplexer output signals are stored in the result register D819 under the control of C3.
These output signals are applied to the bus ADCBØ ... 8 via D819 and D811 when signal C2 is logic 0.
C2 = 1 indicates that the buffer outputs are in tri-state.
At the same time, the last bit is copied to re-establish a correct 9-bit 2's complement notation.

The data placed on the bus in this way are the corrected samples and are shifted again into the shift register.
After 256 correction steps the shift register contains the complete corrected signal.

Signal NDR (new data ready) now reverts to logic 1 and the shift register contents are copied into the ACCU memory under the control of the microprocessor and its software.

The contents of the shift register are copied into the ACCU memory including the overflow markings +127 or −128. The overflow markings are detected by hardware when the contents of the ACCU are required to be displayed on the c.r.t. screen. This results then in a flashing trace on the c.r.t. screen to indicate this overflow. The same is possible if the ACCU-memory contents are saved in one of the memories STO1 - STO2 or STO3.

Signal $\overline{\text{CLR}}$ enables zeros to be placed on the bus to reset the shift register contents in case of ACCU-memory clearing.

Data routeing and correction in DRS mode

Refer to description of buffer unit A7.

Note: For timing diagrams and explanation of timing refer to the description of the ACL unit A9.

INCOMING SIGNAL	OUTGOING SIGNAL	GENERATED ON UNIT	USED ON UNIT	DESCRIPTION
ACQBØ ... ACQB8		A7		Acquisition output bits Ø ... 8
	ADCBØ ... 8	A8	A7	ADC output signals bit Ø ... bit 8
C1		A9		Control 1 signal from ACL unit
C2		A9		Control 2 signal from ACL unit
C3		A9		Control 3 signal from ACL unit
CLADC		A9		Clock signal for ADC
$\overline{\text{CLR}}$		A4		Clear signal for shift register
	CONV	A8	A9	Conversion
$\overline{\text{NDR}}$		A9		New data ready
P		A12		P^2CCD-mode
SOD		A7		Microprocessor serial output data
TRACK		A9		Track command from ACL unit
VOUT		A10		CCD logic unit analog output signal
$\overline{\text{WR}}$		A4		Signal WRITE from microprocessor

CONVERSION UNIT A8

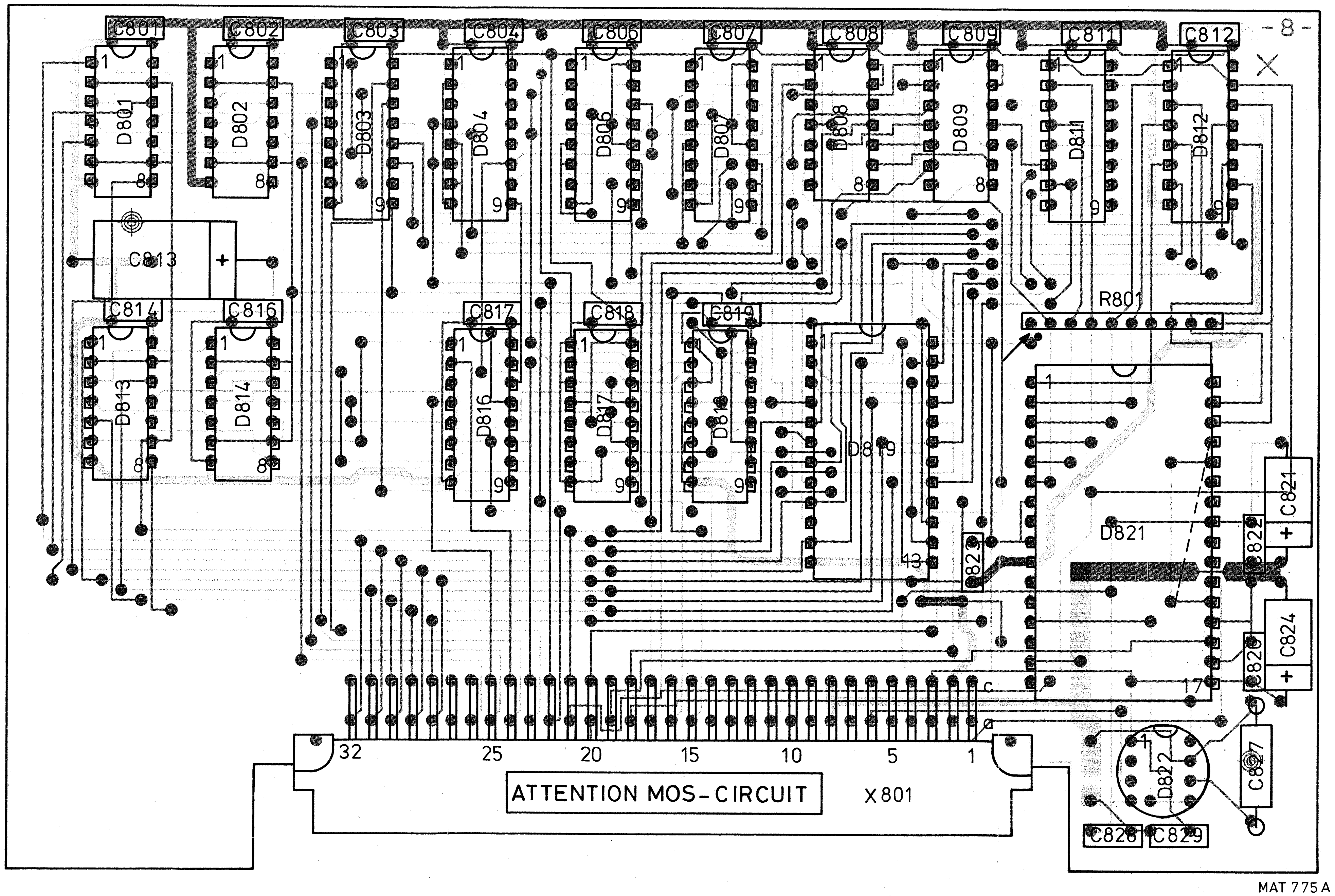


Fig. 6.2.27.

6.2.9.6. Flip-flop FASA

The flip-flop FASA stores the information indicating whether the last sample stored in the shift register was from channel A or channel B.

FASA = 1 : channel A was last sample
FASA = 0 : channel B was last sample

In the P-mode, the flip-flop FASA is set to the level of its D-input signal PDRIVE by the leading edge of every INS pulse on its clock input while the PR signal is logic 1 (CHOP is permanently at logic 1 in the P-mode).

In the DRS modes, flip-flop FASA is switched to the level of its D-input signal CHOP by the leading edge of every INS pulse on its clock input (signals PR and PDRIVE are permanently at logic 1 in the DRS modes).

The state of flip-flop FASA cannot be changed while NDR is logic 1, i.e. during the copying of the shift register contents into the ACCU memory. During this cycle the flip-flop state is read by the software.

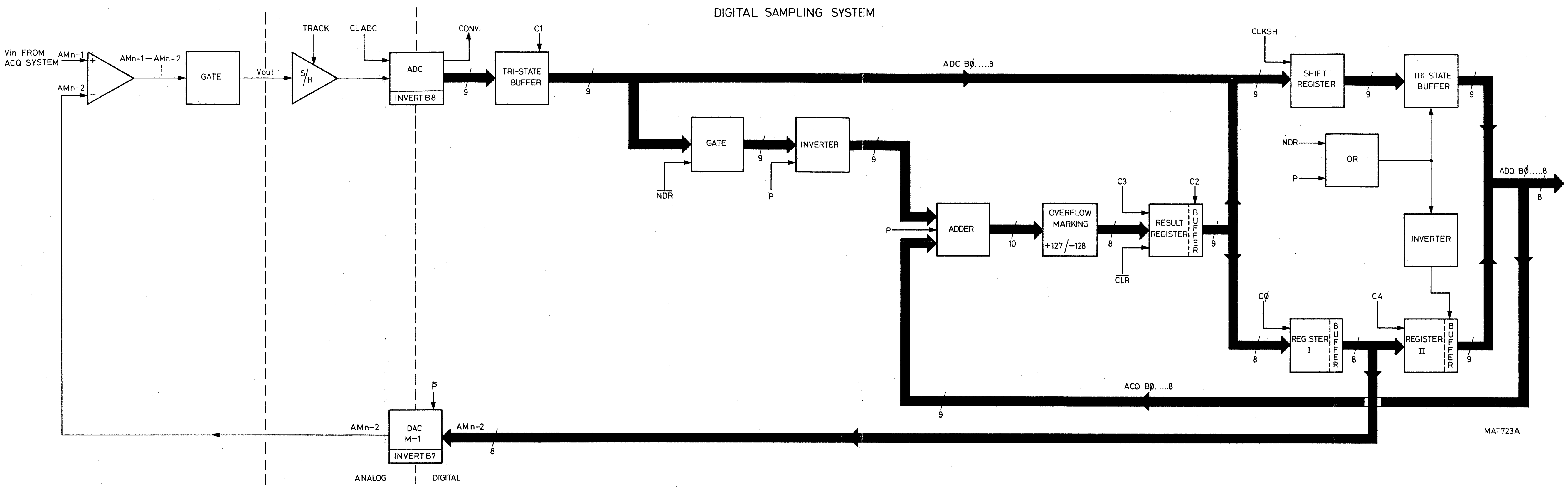


Fig. 6.2.35.

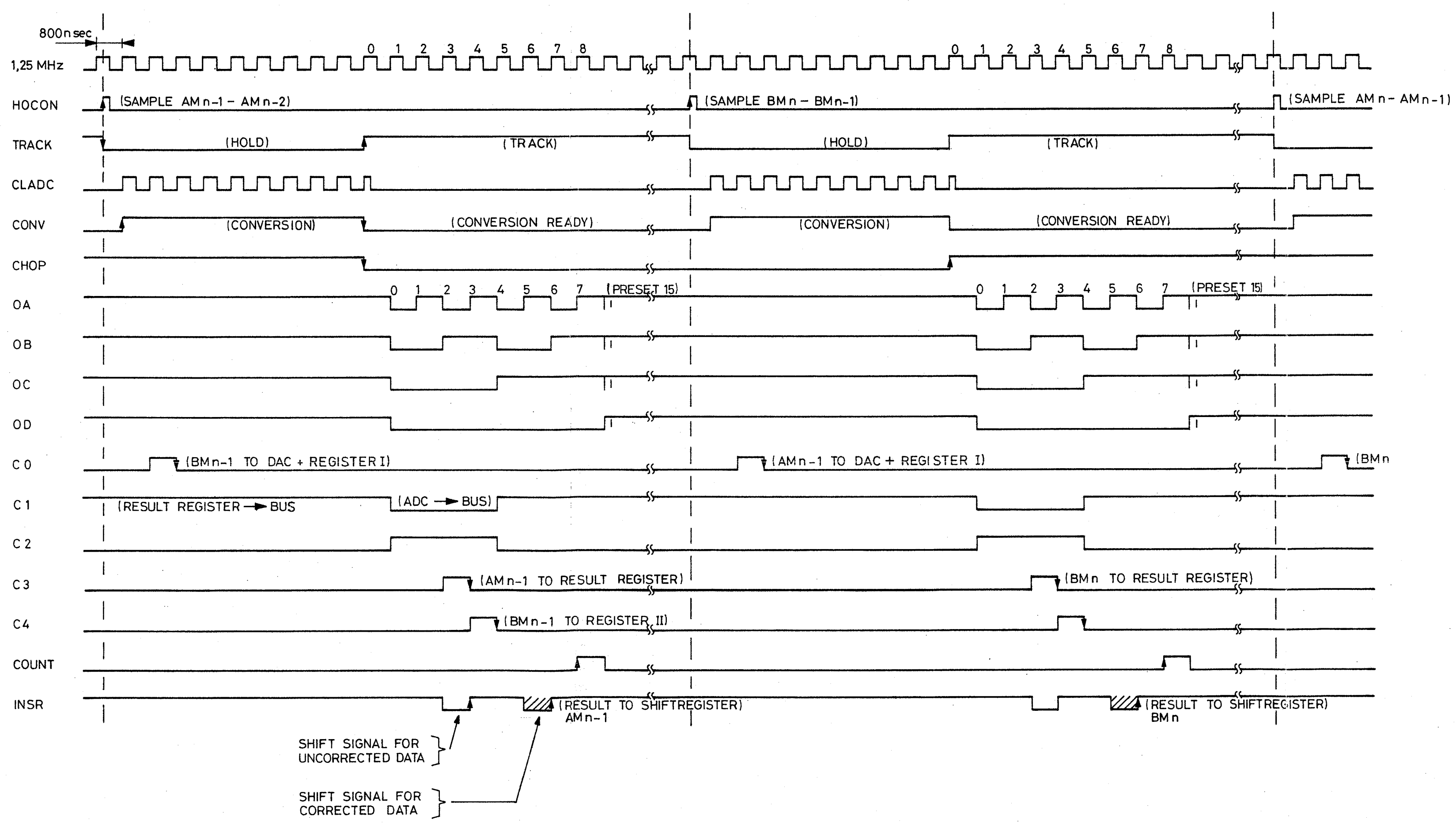
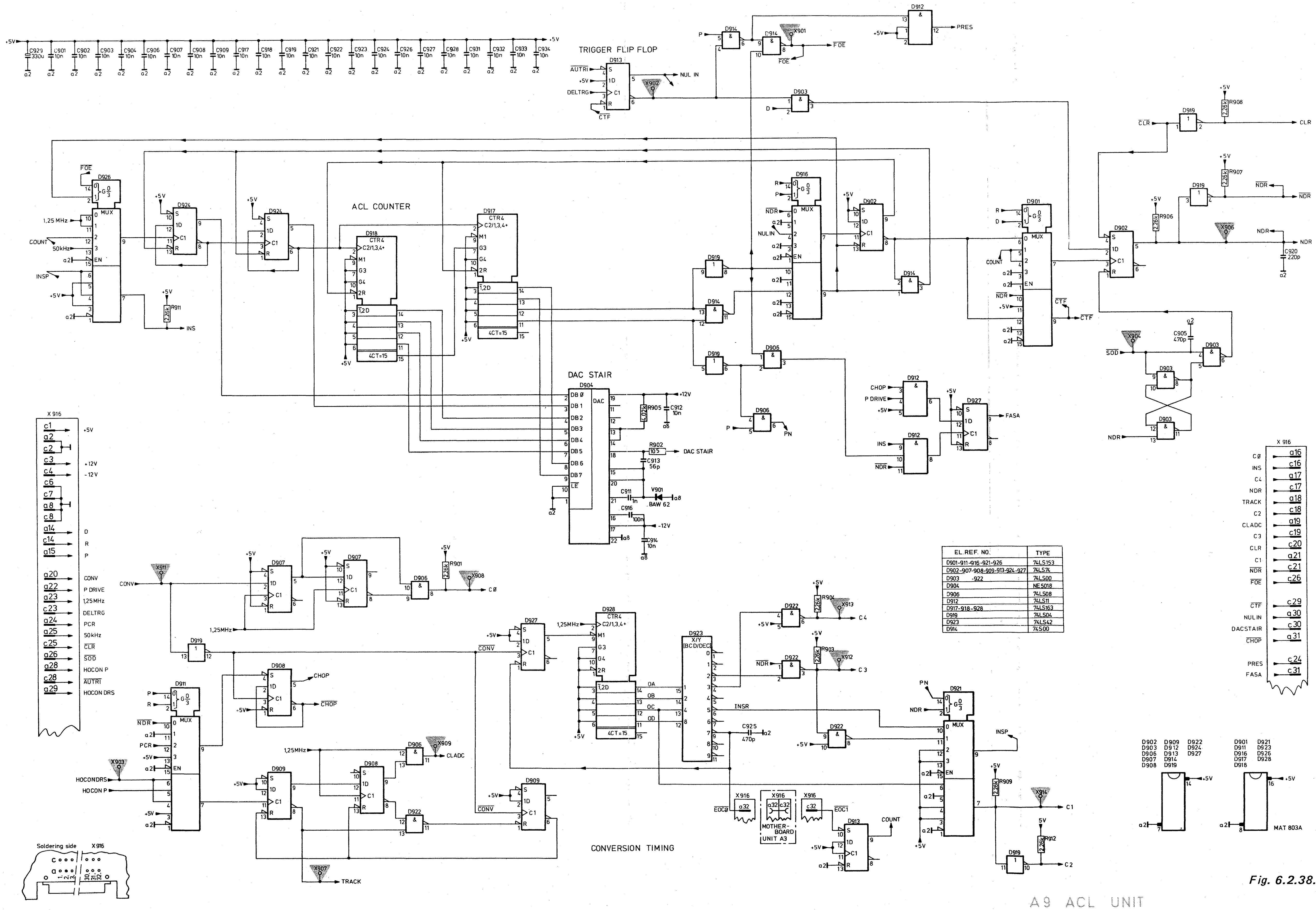


Fig. 6.2.36.



EL.REF. NO.	TYPE
D901-911-916-921-926	74LS153
D902-907-908-909-913-924-927	74LS74
D903 -922	74LS00
D904	NE5018
D906	74LS08
D912	74LS11
D917-918-928	74LS163
D919	74LS04
D923	74LS42
D914	74S00

Fig. 6.2.38.

A9 ACL UNIT

6.2.10. CCD Logic unit A10

6.2.10.1. General

The CCD logic unit controls the correct functioning of the P2CCD circuit on unit 11. The control circuits can be considered under the following headings:

- circuits for various supply voltages
- P2CCD external output circuits
- control signals generator
- clock-pulse generator

6.2.10.2. Circuits for various supply voltages

+11,4 V	From the +12 V supply a stabilised +11,4 V is derived by the circuit consisting of D1016 (1,2,3) and transistor V1018. This +11,4 V supply output can be adjusted by potentiómeter R1080 at the input of D1016.
−11,4 V	A −11,4 V stabilised supply voltage is derived from the −12 V supply by the circuit consisting of D1016 (5,6,7) and transistors V1021 and V1019, The level of the −11,4 V supply is controlled by the stabilised +11,4 V on resistor R1098.
+5B	A +5 V stabilised supply voltage is derived from the +11,4 V at input 1 of D1021.
BIAS	A stabilised bias voltage for the P2CCD input signal circuits is obtained from the stabilised +11,4 V by means of the circuit comprising D1002 (1,2,3) and transistor V1006. Potentiometer R1002 provides for adjusting this bias voltage and is normally set to +7,5 V approx.
DRAIN	A stabilised drain voltage for the P2CCD output circuit is taken from the stabilised +11,4 V by circuit D1002 (5,6,7) and transistor V1007. Adjustment of this drain voltage is by potentiometer R1008 and is normally set to +22 V approx.
P11IN/P22IN	Two adjustable threshold voltages are available for the P2CCD circuit input sections, which are derived from the stabilised +11,4 V. These voltages can be adjusted by potentiometers R1026 and R1007 respectively and are normally set to +6 V approx.
SUB	A voltage applied to the substrate input of the P2CCD, adjustable by means of potentiometer R1027 and normally set to +10 V approx.

6.2.10.3. P2CCD external output circuits

Output signals OUT PA and OUT PB (from the two sections of the P2CCD on unit 11) are applied to two output circuits comprising two multiplexers D1018, D1019 and two integrators consisting of operational amplifiers D1009, D1011 and capacitors C1034, C1036.
Both output circuits serve to elliminate output source-follower drift, noise signals and clock-pulse or reset crosstalk signals that would influence the P2CCD output signals.

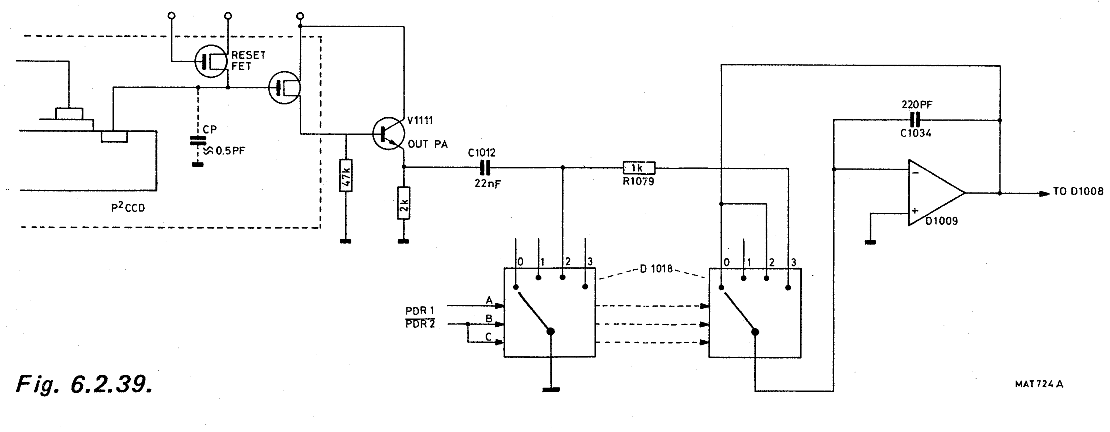


Fig. 6.2.39.

INCOMING SIGNAL	OUTGOING SIGNAL	GENERATED ON UNIT	USED ON UNIT	DESCRIPTION
$\overline{\text{AUTRI}}$		A13		Auto trigger
	CØ	A9	A7	Control Ø signal
	C1	A9	A8	Control 1 signal
	C2	A9	A8	Control 2 signal
	C3	A9	A8	Control 3 signal
	C4	A9	A7	Control 4 signal
	$\overline{\text{CHOP}}$	A9	A21	Chopper signal
	CLADC	A9	A8	Clock signal for ADC
$\overline{\text{CLR}}$		A4		Clear signal for shift register
	CLR	A9	A8	Inverted CLR signal
CONV		A8		Conversion
	$\overline{\text{CTF}}$	A9	A13	Clear signal for trigger flip-flop
D		A12		D-mode signal
	DACSTAIR	A9	A22	Output signal of DAC STAIR
DELTRIG		A13		Delayed trigger signal
	$\overline{\text{EOCØ}}$	A9	A9	Enable output COUNT Ø
$\overline{\text{EOC1}}$		A3		Enable output COUNT 1
	FASA	A9	A202	Output phase flip-flop
	$\overline{\text{FOE}}$	A9	A10	Frequency output enable
HOCON DRS		A22		Hold and convert signal in D-R and S mode
HOCONP		A10		Hold and convert signal in P-mode
	INS	A9	A7	Shift command for shift register
	NDR-$\overline{\text{NDR}}$	A9	A4-7-8	New data ready
	NULIN	A9	A21	Signal to switch vert. ampl. input to zero
P		A12		P-mode signal
PDRIVE		A10		Phase signal in P-mode
	PRES	A9	A10	Enable signal in P-mode.
R		A12		R-mode signal
S		A12		S-mode signal
$\overline{\text{SOD}}$		A4		Microprocessor serial output data
	TRACK	A9	A8-A22	Track command for S/H circuit
50 kHz		A12		50 kHz pulse
1,25 MHz		A12		1,25 MHz pulse
+5 V		A15		
−12 V		A15		
+12 V		A15		
⏚		A15		

TEST POINTS	
X901	$\overline{\text{FOE}}$
X902	NUL IN
X903	HOCONDRS
X904	$\overline{\text{SOD}}$
X906	NDR
X907	TRACK
X908	CØ
X909	CLADC
X911	CONV
X912	C3
X913	C4
X914	C1
X916	EOCØ/EOC1

ACL UNIT A9

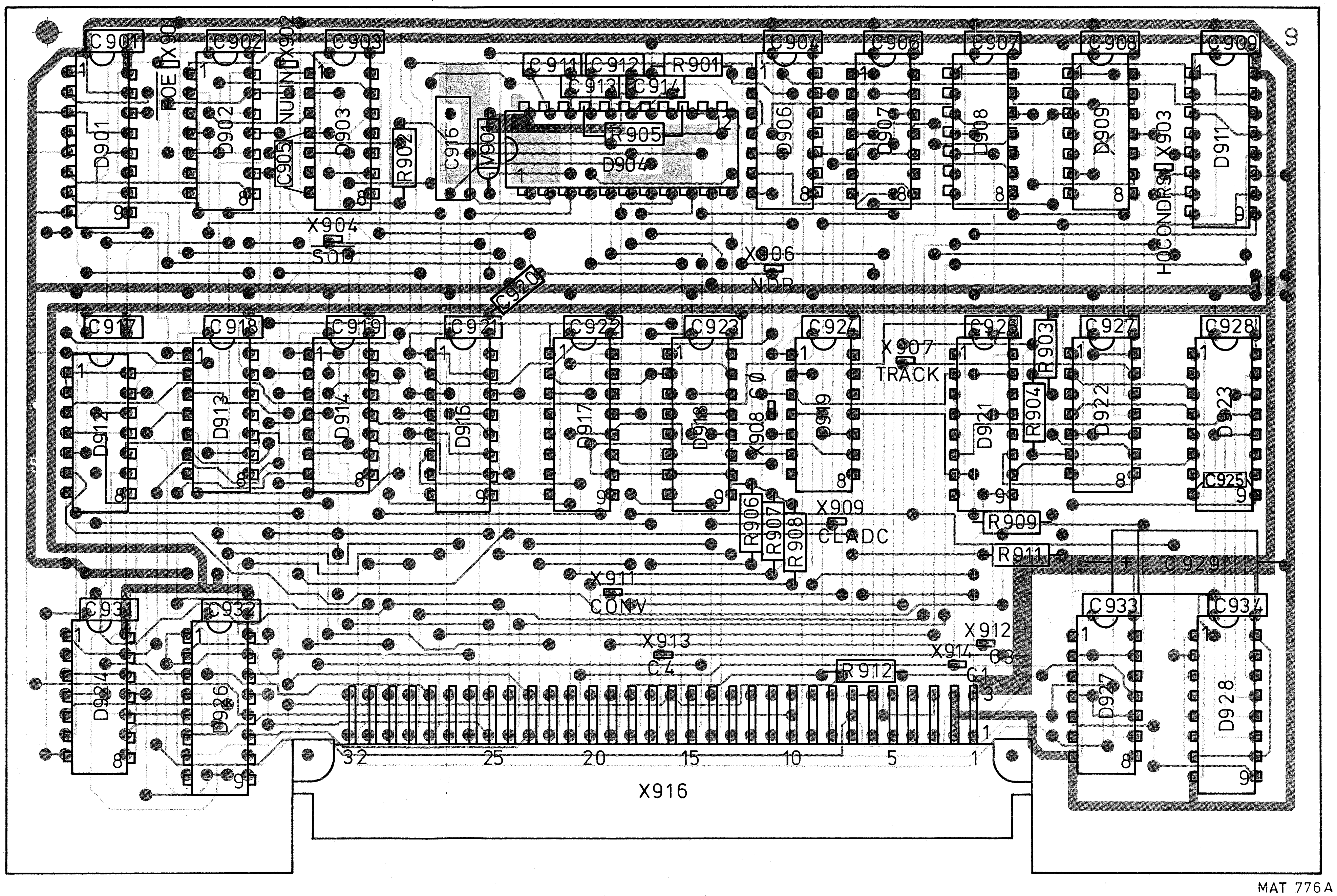


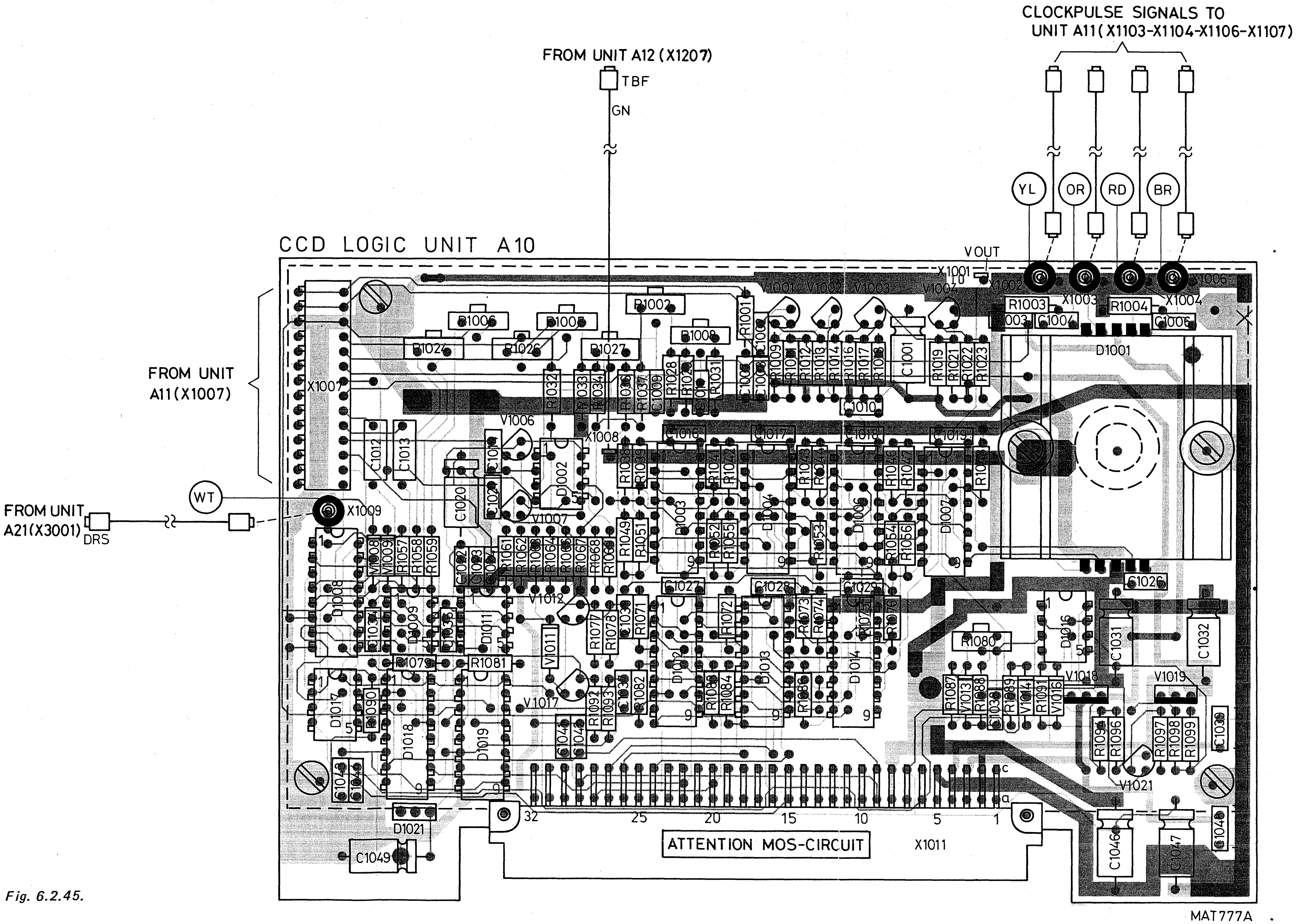
Fig. 6.2.37.

Signals P2/A2 are 180° phase-shifted with P1/A1. The delay between the filter sections is approximately 4 nsec.

For correct sampling of the input signal by the P^2CCD, it is necessary that the low level (+2 V) of the clock signals P2 and P1 remains constant. To achieve this, the clock-signals P2 and P1 are measured on unit 10, which results in a feedback signal CLAFB of approximately +3,6 V (clock-pulse amplitude feedback signal).

This voltage is applied to the base of transistor V1001 via low-pass filter R1001/C1002. A stable reference voltage of +3,6 V is applied to the base of transistor V1003. In this way, variations of the low level (+2 V) of the clock-signals P2 and P1 result in a variation of the signal level on the collector of transistor V1003. This variation is then fed back via emitter-follower V1004 to a current source pin 1 of the clock-pulse generator D1001.
The clock-pulse generator is driven by a signal CLKDR from pin 2 of flip-flop D1006.

INCOMING SIGNAL	OUTGOING SIGNAL	GENERATED ON UNIT	USED ON UNIT	DESCRIPTION
	BIAS	A10	A11	Bias voltage
CLAFB		A11		Clock-pulse amplitude feedback
	DRAIN	A10	A11	Drain voltage
$\overline{FOE}$		A9		Frequency output enable
OUTPA		A11		P^2CCD output signal section I
OUTPB		A11		P^2CCD output signal section II
P		A12		P-mode signal
$\overline{PECL}$		A12		P-mode signal for ECL circuits
PRES		A9		Enable signal in P-mode
	P11 IN	A10	A11	Threshold voltage
	P22 IN	A10	A11	Threshold voltage
	RES1	A10	A11	Reset signal 1
	RES2	A10	A11	Reset signal 2
	SUB	A10	A11	Substrate voltage
78 kHz		A12		78 kHz pulse
	+11,4 V	A10	A11	
	+40 V	A10	A11	
–5,2 V		A15		
+6 V		A15		
–6 V		A15		
+12 V		A15		
–12 V		A15		
+40 V		A15		
DRS		A21		Signal from T & H gate
TBF		A12		Time-base fast
	VOUT	A10	A8	CCD logic unit analog output signal
	HOCONP	A10	A9	Hold and convert in P-mode


CLOCKPULSE SIGNALS TO
UNIT A11 (X1103-X1104-X1106-X1107)
FROM UNIT A12 (X1207)
TBF
GN
YL
OR
RD
BR
CCD LOGIC UNIT A10
VOUT
FROM UNIT
A11 (X1007)
FROM UNIT
A21 (X3001)
DRS
WT
ATTENTION MOS-CIRCUIT
X1011
MAT777A

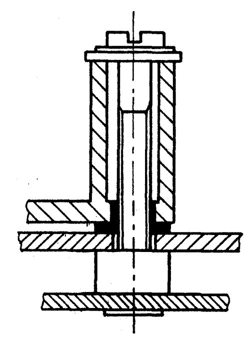
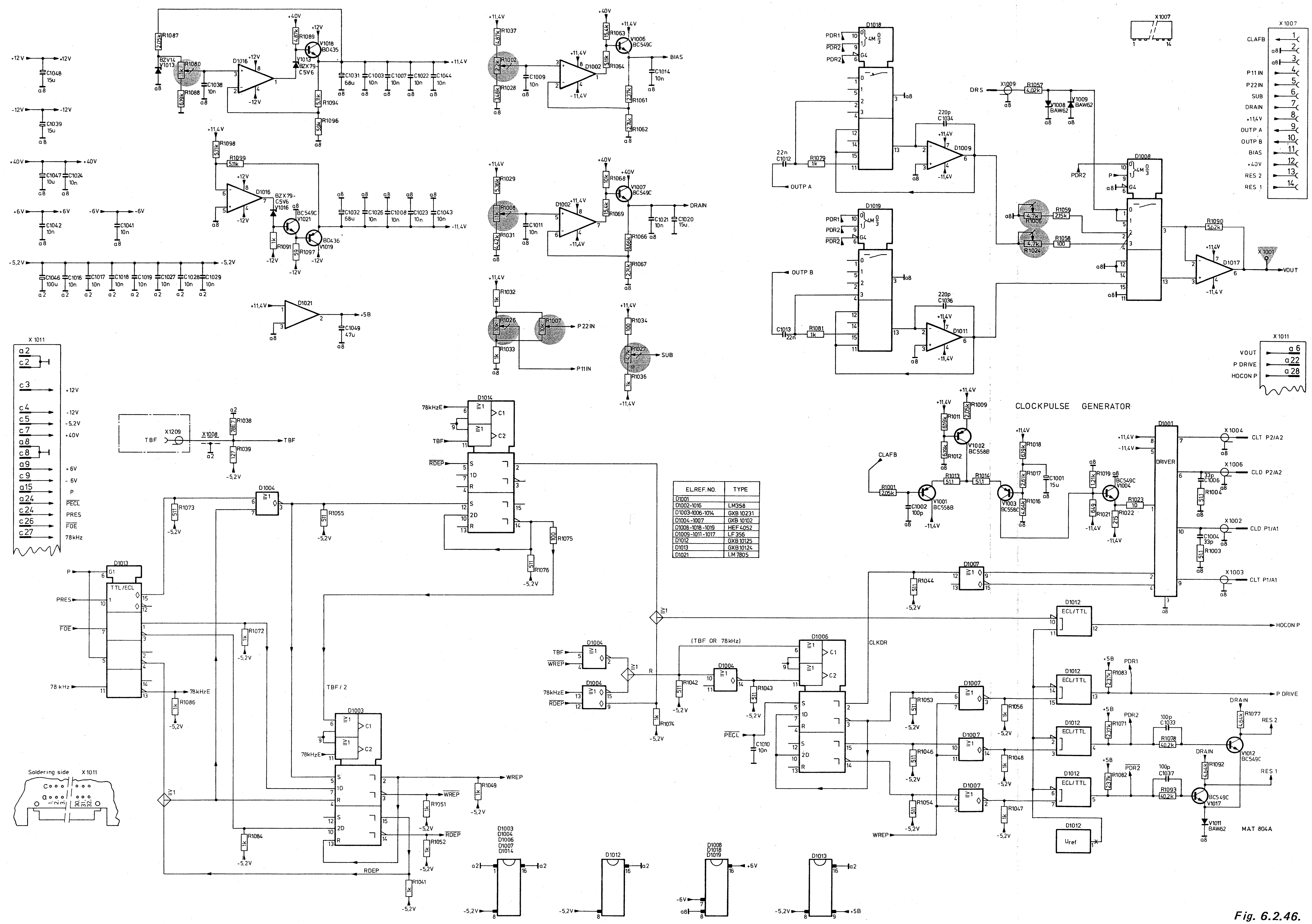


Fig. 6.2.45.



EL.REF.NO.	TYPE
D1001	
D1002-1016	LM358
D1003-1006-1014	GXB 10231
D1004-1007	GXB 10102
D1008-1018-1019	HEF 4052
D1009-1011-1017	LF 356
D1012	GXB 10125
D1013	GXB 10124
D1021	LM 7805

Fig. 6.2.46.

A 10 CCD LOGIC UNIT

6.2.11. P2CCD unit A11

6.2.11.1. General

The P^2CCD circuit (Profiled Peristaltic Charged Coupled Device) is used in this digital storage oscilloscope as an analog shift register. Using this circuit, different time conversions can be realised in the TIME/DIV switch positions 500 ns/DIV up to 0,2 ms/DIV to digitise fast input signals with a relatively slow (12,8 μs approx.) analog-to-digital converter.
The P^2CCD circuit D1101 located on unit A11 consists of two CCD sections in parallel. These two sections are required in order to take samples of the input signal on the 0^o phase and on the 180^o phase of the clock signal.

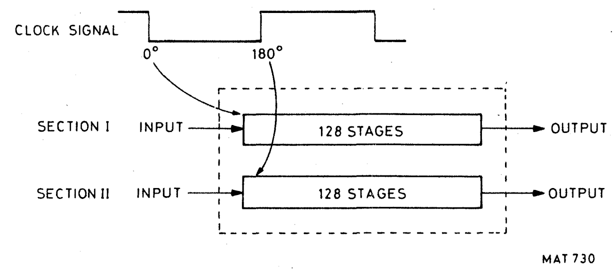


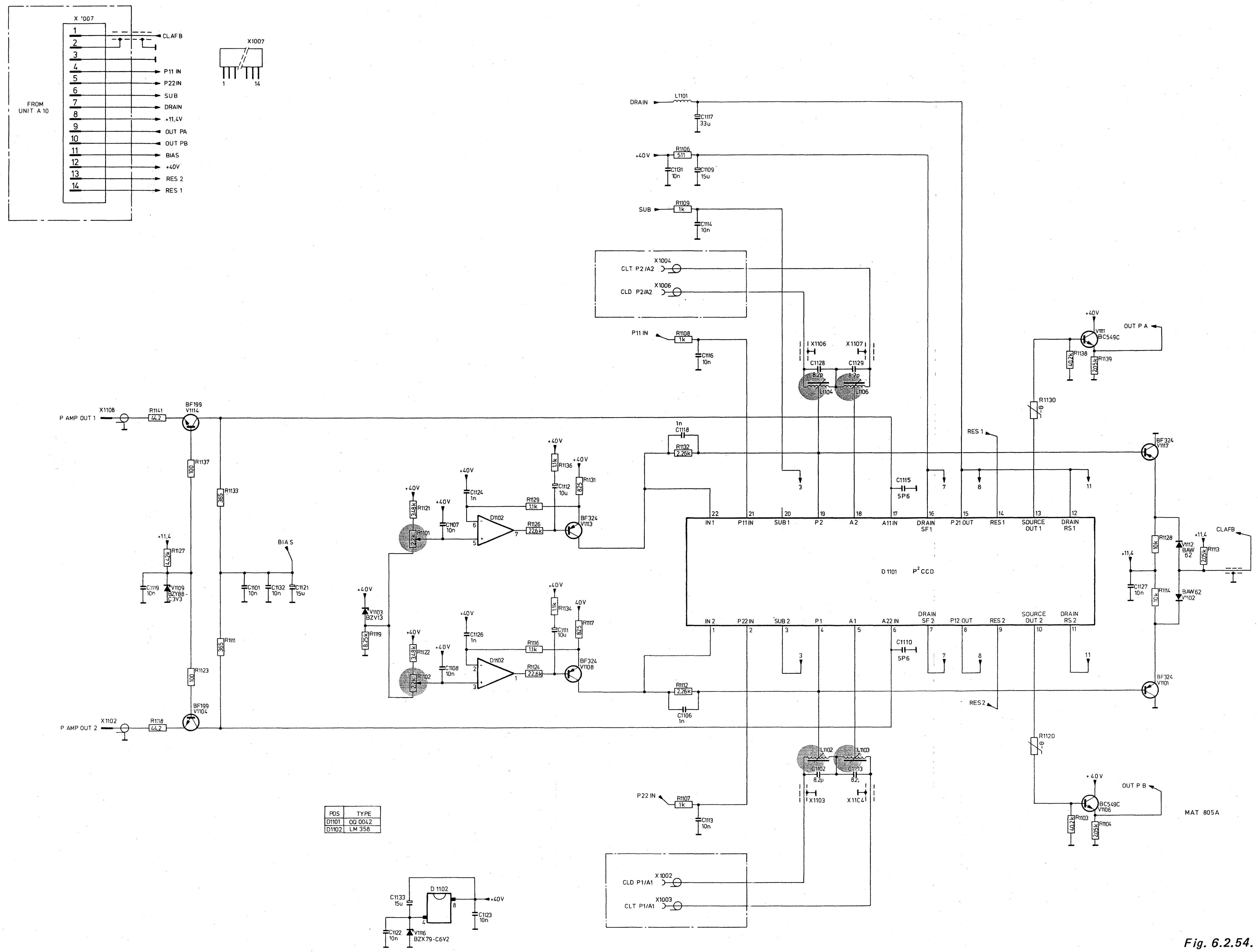
Fig. 6.2.47.

Each section consists of 128 stages, i.e. the complete circuit D1101 contains 256 stages in which a total of 256 samples can be stored.
In addition, each section consists of a system for the transport of charges, an input circuit that accepts the charges from the vertical channel switch signals P AMP OUT I and P AMP OUT 2, and an output section which measures the sizes of the charges and produces corresponding output signals.

Samples can be taken from the analog input signal at a high sample rate, which varies between 125 kHz and 50 MHz depending on the TIME/DIV switch setting. These samples are shifted into the P^2CCD.

After the reading in of information in all the 256 stages, the reading out cycle is started. The entire operation is carried out under the control of the acquisition control logic and the CCD logic unit.

The P^2CCD circuit contents are read out with a lower frequency of 78 kHz approx.
This frequency remains the same for the different TIME/DIV switch settings and is low enough to guarantee perfect ADC conversion by the ADC on unit A8.
The frequency must not be too low otherwise loss of information could occur in the P^2CCD circuit.



POS	TYPE
D1101	OQ 0042
D1102	LM 358

Fig. 6.2.54.

A11 P²CCD UNIT

INCOMING SIGNAL	OUTGOING SIGNAL	GENERATED ON UNIT	USED ON UNIT	DESCRIPTION
BIAS		A10		Bias voltage
	CLAFB	A11	A10	Clock-pulse amplitude feedback
DRAIN		A10		Drain voltage
	OUTPA	A11	A10	P^2CCD output signal section I
	OUTPB	A11	A10	P^2CCD output signal section II
P11IN		A10		Threshold voltage
P22IN		A10		Threshold voltage
RES1		A10		Reset signal 1
RES2		A10		Reset signal 2
SUB		A10		Substrate voltage
+11,4 V		A10		
+40 V		A10		
⏚		A10		
PAMPOUT1		A21		Output signal of amplifier
PAMPOUT2		A21		Output signal of amplifier

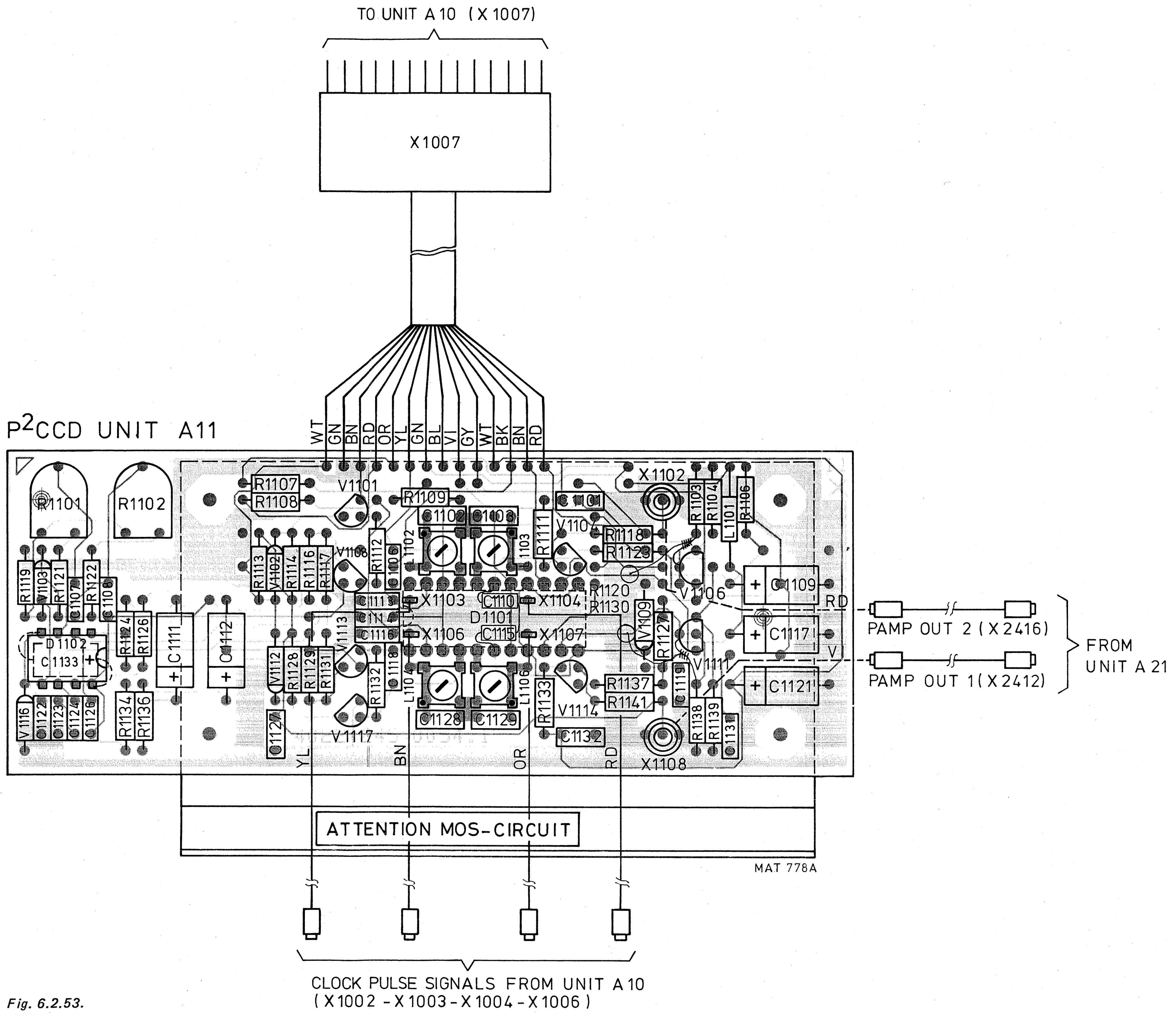

TO UNIT A10 (X1007)
X1007
P²CCD UNIT A11
WT GN BN RD OR YL GN BL VI GY WT BK BN RD
PAMP OUT 2 (X2416)
PAMP OUT 1 (X2412)
FROM UNIT A21
YL BN OR RD
ATTENTION MOS-CIRCUIT
MAT 778A
CLOCK PULSE SIGNALS FROM UNIT A10
(X1002 - X1003 - X1004 - X1006)

Fig. 6.2.53.

INCOMING SIGNAL	OUTGOING SIGNAL	GENERATED ON UNIT	USED ON UNIT	DESCRIPTION
	D	A12	A9	DIRECT-mode signal
DØ ... D7		A4		Data bits from system data bus
$\overline{\text{IO6}}$		A4		Address decoding signal TB select
	R	A12	A9	ROLL-mode signal
	S	A12	A9-A22	SAMPLE-mode signal
	P	A12	A7-8-9-10-21	P^2CCD-mode signal
	$\overline{\text{PECL}}$	A12	A10	P-mode signal from ECL circuits
	TBF CCD	A12	A10	Time-base fast for CCD unit
	TBF TRIGGER	A12	A13	Time-base fast for TRIGGER unit
	TBS	A12	A13-A22	Time-base slow signal
	50 kHz	A12	A9	
	78 kHz	A12	A10	
	2.5 kHz	A12	A20	2.5 kHz for CAL voltage
	156 kHz	A12	A15	
	1.25 MHz	A12	A9-13	
$\overline{\text{WR}}$		A4		Signal WRITE from microprocessor
2.5 MHz		A4		Microprocessor clock-pulse output signal
+5 V		A15		
–5.2 V		A15		

TEST POINTS	
X1201	RESET
X1202	LOW
X1203	5 Hz
X1204	156 kHz
X1207	TBF
X1208	VC_x

TIME-BASE UNIT A12

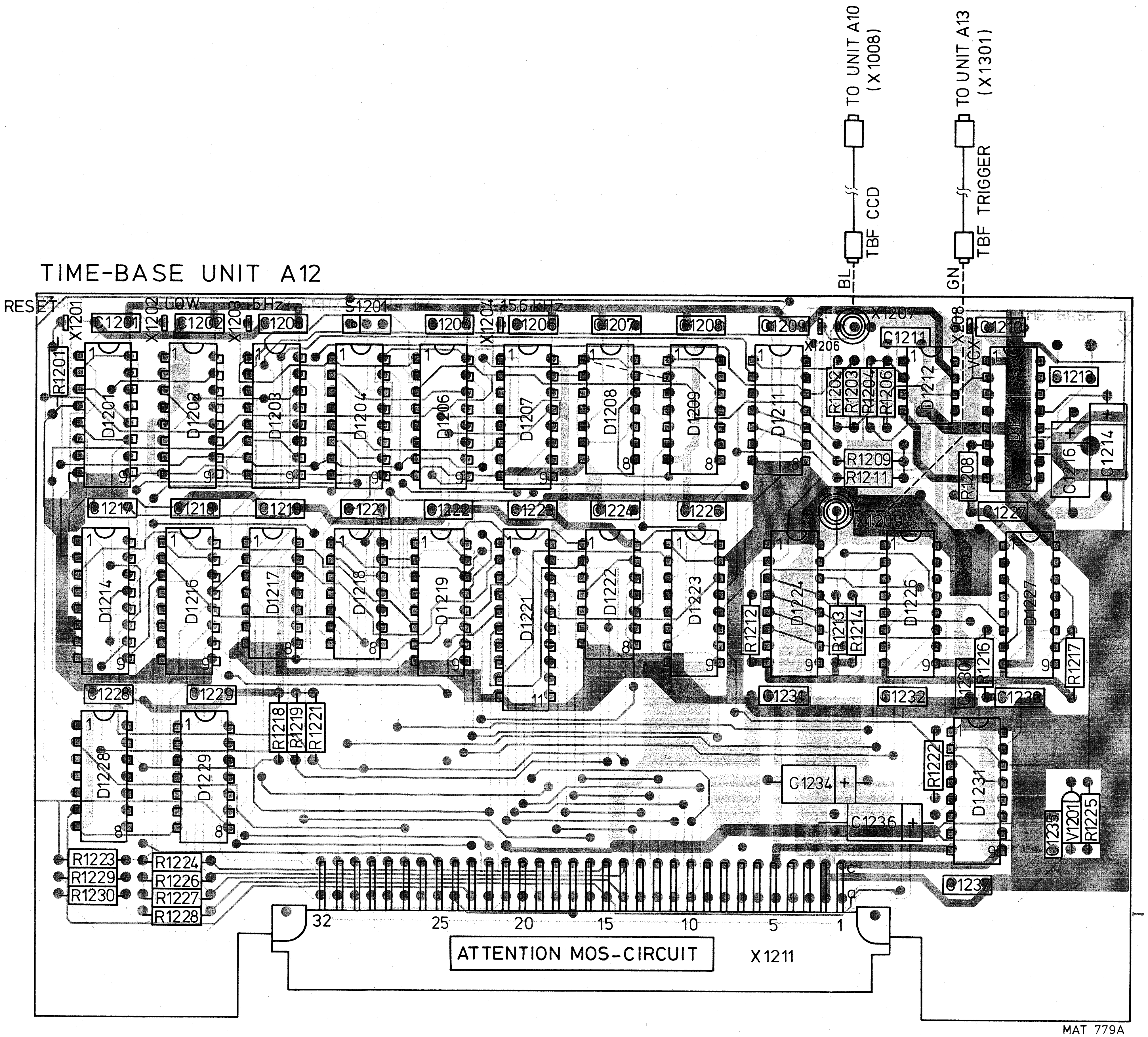
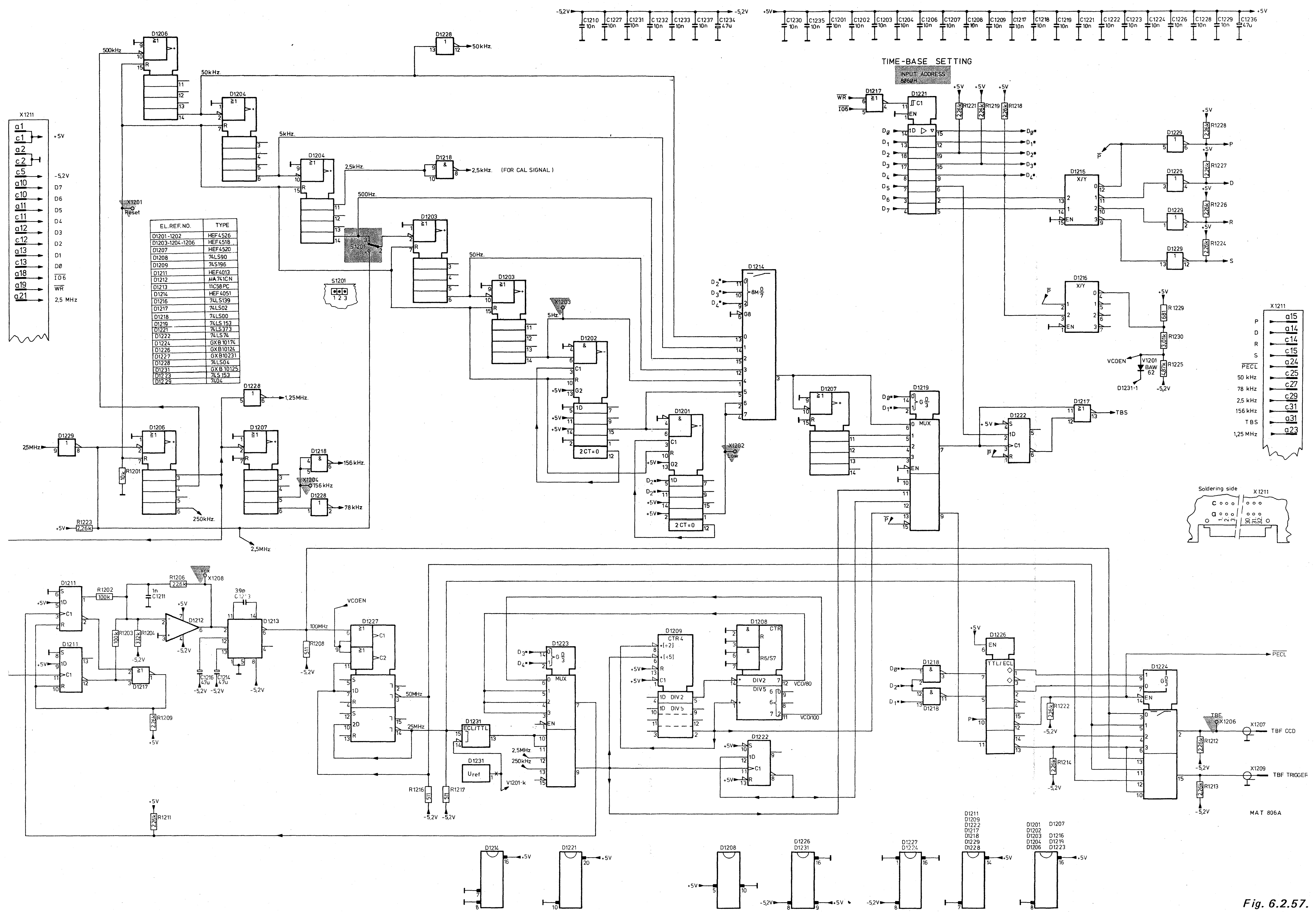


Fig. 6.2.56.



EL.REF.NO.	TYPE
D1201-1202	HEF4526
D1203-1204-1206	HEF4518
D1207	HEF4520
D1208	74LS90
D1209	74S196
D1211	HEF4013
D1212	μA741CN
D1213	11C58PC
D1214	HEF4051
D1216	74LS139
D1217	74LS02
D1218	74LS00
D1219	74LS153
D1221	74LS373
D1222	74LS74
D1224	GXB10174
D1226	GXB10124
D1227	GXB10231
D1228	74LS04
D1231	GXB10125
D1223	74S153
D1229	7404

Fig. 6.2.57.

A12 TIME BASE UNIT

INCOMING SIGNAL	OUTGOING SIGNAL	GENERATED ON UNIT	USED ON UNIT	DESCRIPTION
A0 - A1 - A2		A4		Address bits from system address bus
AUTO TB		A22		Auto signal from AUTO switch
	$\overline{\text{AUTRI}}$	A13	A9	Auto trigger
	$\overline{\text{AVSB}}$	A13	A4-6-20	logic "0" in X= A/Y= B mode
$\overline{\text{CTF}}$		A9		Clear signal for trigger flip-flop
DØ. . . D7		A4		Data bits from system data bus
	DACDEL	A13	A22	Output signal of DAC delay
	DELTRG	A13	A9-A202	Delayed trigger signal
	DJ	A13	A20	Dot join signal
DT		A4		Display timing
	ENKEL	A13	A20	Single channel mode
	FAS DI	A13	A6	Phase on display level
	FRUN	A13	A22-A202	Freerun signal
$\overline{\text{IO8}}$		A4		I/O address decoding signal
	PEN LFT	A13	OUTPUT	Penlift
	QØ - Q1	A13	A20	Control signals for dot join
	RESDJ	A13	A20	Reset dot join
TBF		A12		Time-base fast
TBS		A12		Time-base slow
TRIST		A22		Trigger signal for strecher
	TRSH	A13	A20	Trigger for dot join sample & hold
$\overline{\text{WR}}$		A4		Signal WRITE from microprocessor
X OUT		A20		Horizontal output signal
	X PLOT	A13	OUTPUT	Horizontal plot output signal
	Y EX	A13	A20	Y-expand
Y OUT		A20		Vertical output signal
	Y PLOT	A13	OUTPUT	Vertical plot output signal
	ZDJ	A13	A4-A20	Z dot join
1.25 MHz		A12		
2.5 MHz		A4		
+5V		A15		
–5.2V		A15		
+12V		A15		
–12V		A15		
⊥		A15		

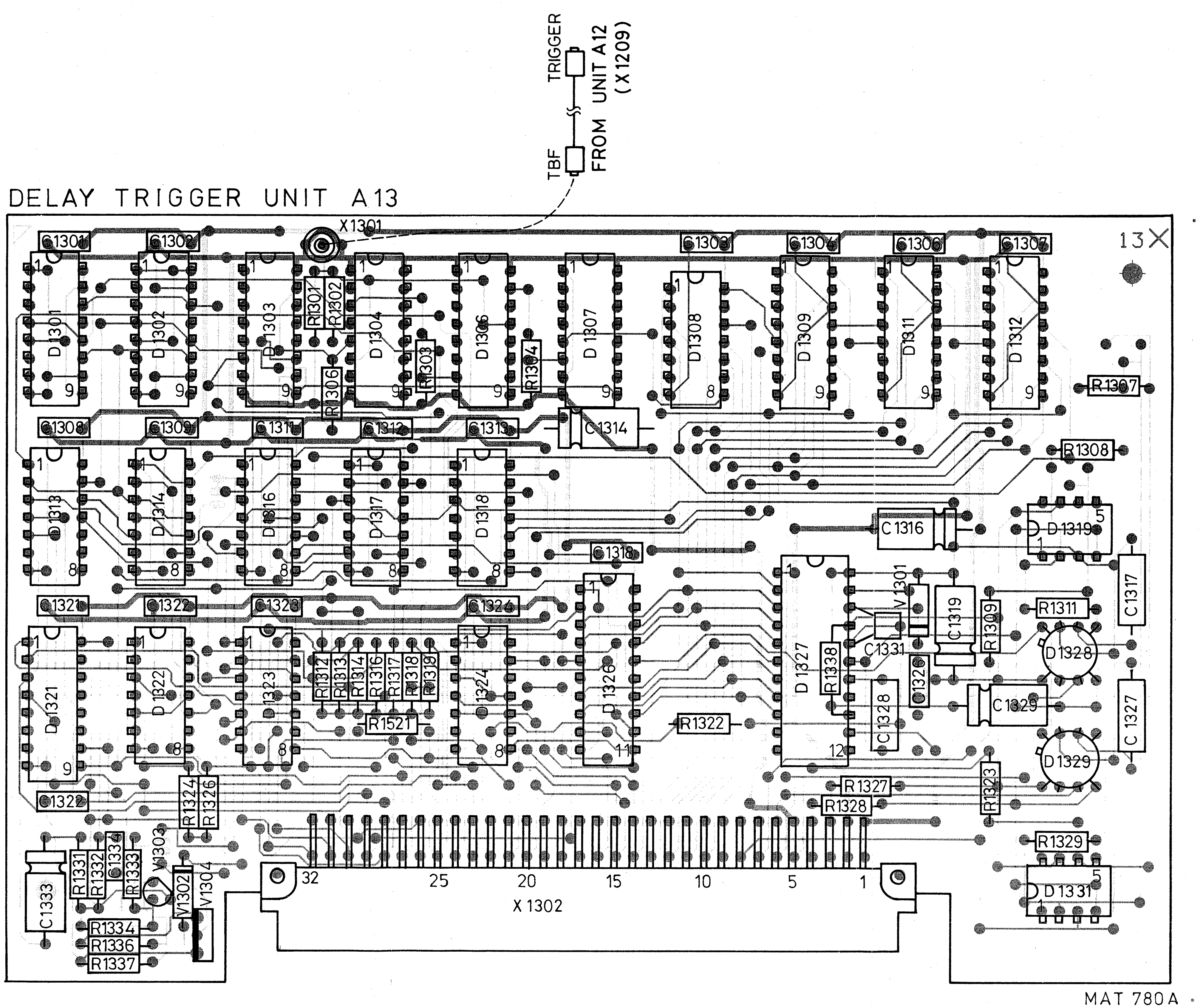
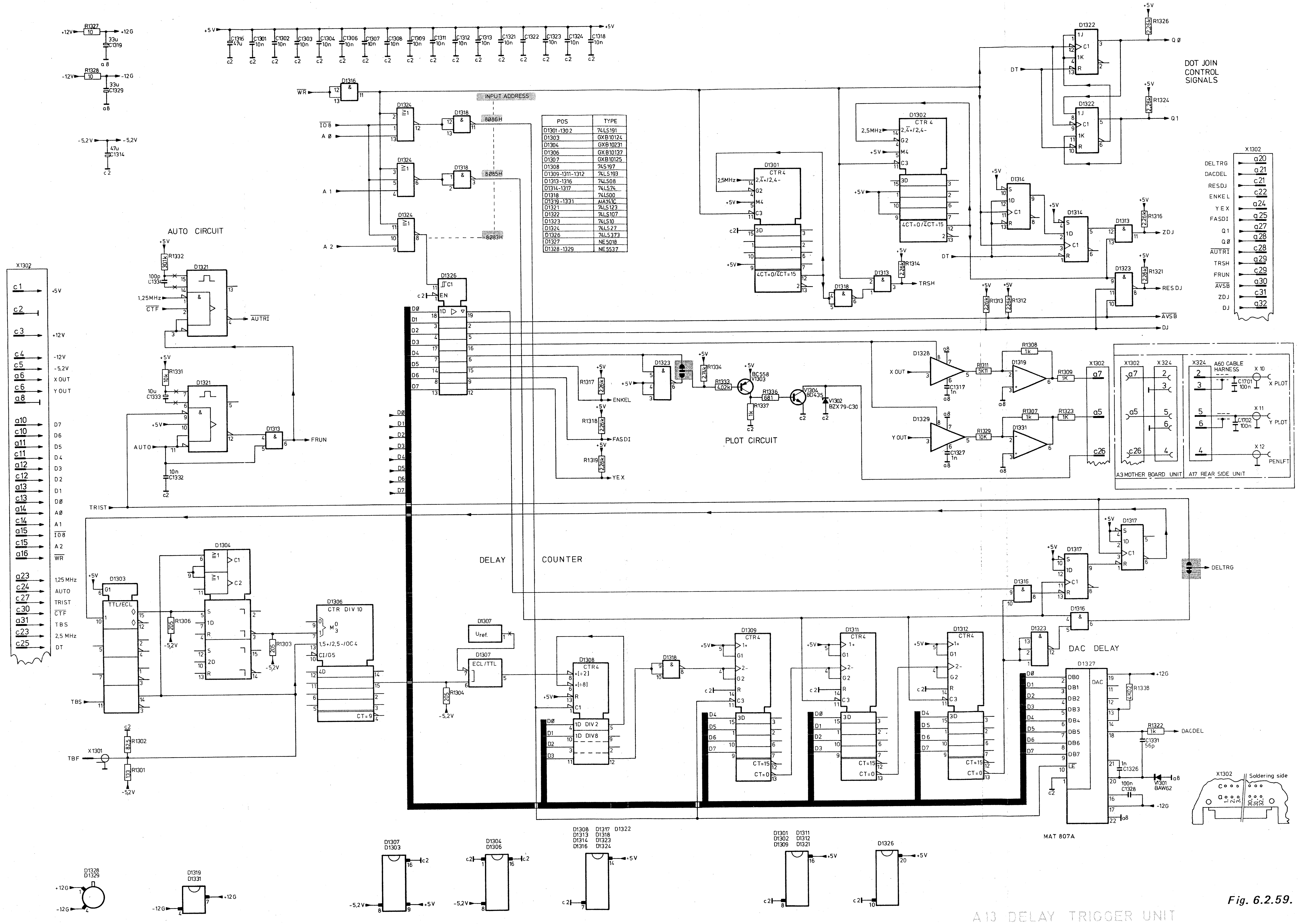

TRIGGER
TBF
FROM UNIT A12 (X1209)
DELAY TRIGGER UNIT A13
X1301
13X
X 1302
MAT 780A

Fig. 6.2.58.



POS	TYPE
D1301-1302	74LS191
D1303	GXB10124
D1304	GXB10231
D1306	GXB10137
D1307	GXB10125
D1308	74S197
D1309-1311-1312	74LS193
D1313-1316	74LS08
D1314-1317	74LS74
D1318	74LS00
D1319-1331	μA741C
D1321	74LS123
D1322	74LS107
D1323	74LS10
D1324	74LS27
D1326	74LS373
D1327	NE5018
D1328-1329	NE5537

Fig. 6.2.59.

A13 DELAY TRIGGER UNIT

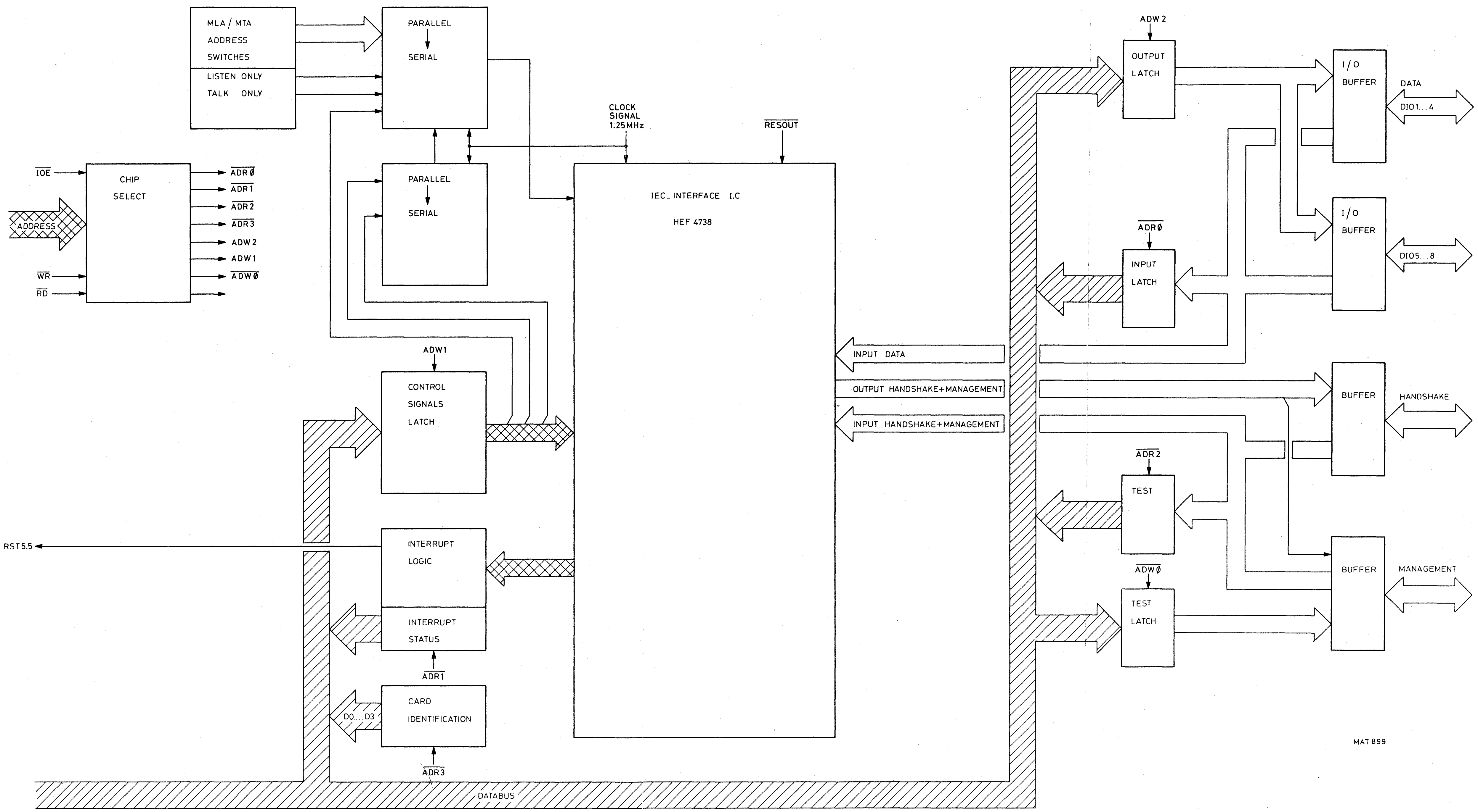
6.2.14. I.E.C. unit A14

There is a connector X1401 available on the motherboard unit A3 in which no plug-in unit is placed.

Here the I.E.C. bus interface option PM 3325 can be placed.

For mounting instructions refer to the sheet which is delivered with the PM3325.

– PM3310C instruments are already provided with an I.E.C. unit A14.
– For service spare parts refer to chapter 12 "PARTS LISTS".

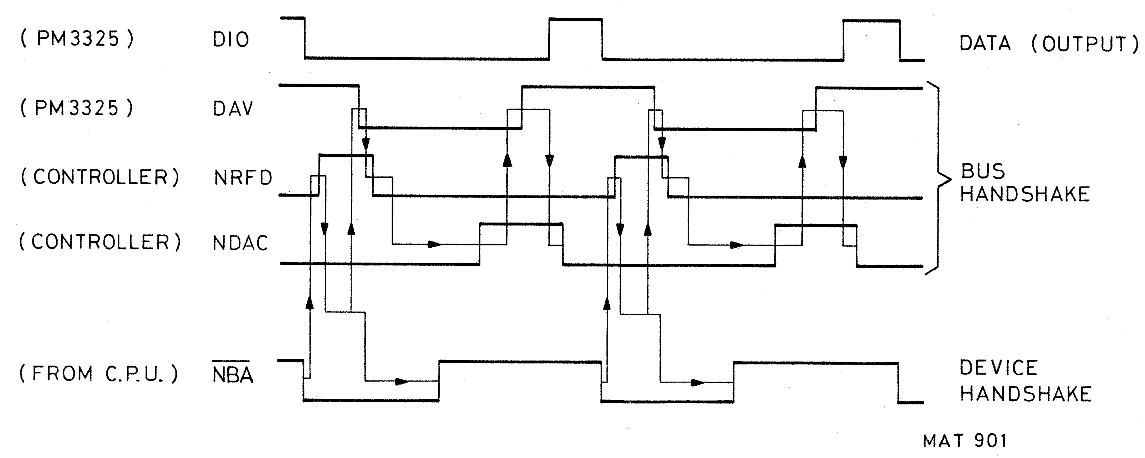

MLA / MTA
ADDRESS
SWITCHES
LISTEN ONLY
TALK ONLY
PARALLEL
SERIAL
PARALLEL
SERIAL
CHIP
SELECT
IOE
ADDRESS
WR
RD
ADRØ
ADR1
ADR2
ADR3
ADW2
ADW1
ADWØ
CLOCK
SIGNAL
1.25MHz
RESOUT
IEC_ INTERFACE I.C
HEF 4738
ADW1
CONTROL
SIGNALS
LATCH
RST5.5
INTERRUPT
LOGIC
INTERRUPT
STATUS
ADR1
CARD
IDENTIFICATION
D0...D3
ADR3
DATABUS
INPUT DATA
OUTPUT HANDSHAKE+MANAGEMENT
INPUT HANDSHAKE+MANAGEMENT
ADW 2
OUTPUT
LATCH
ADRØ
INPUT
LATCH
ADR2
TEST
ADWØ
TEST
LATCH
I/O
BUFFER
DATA
DIO1...4
I/O
BUFFER
DIO5...8
BUFFER
HANDSHAKE
BUFFER
MANAGEMENT
MAT 899

Transmitting:

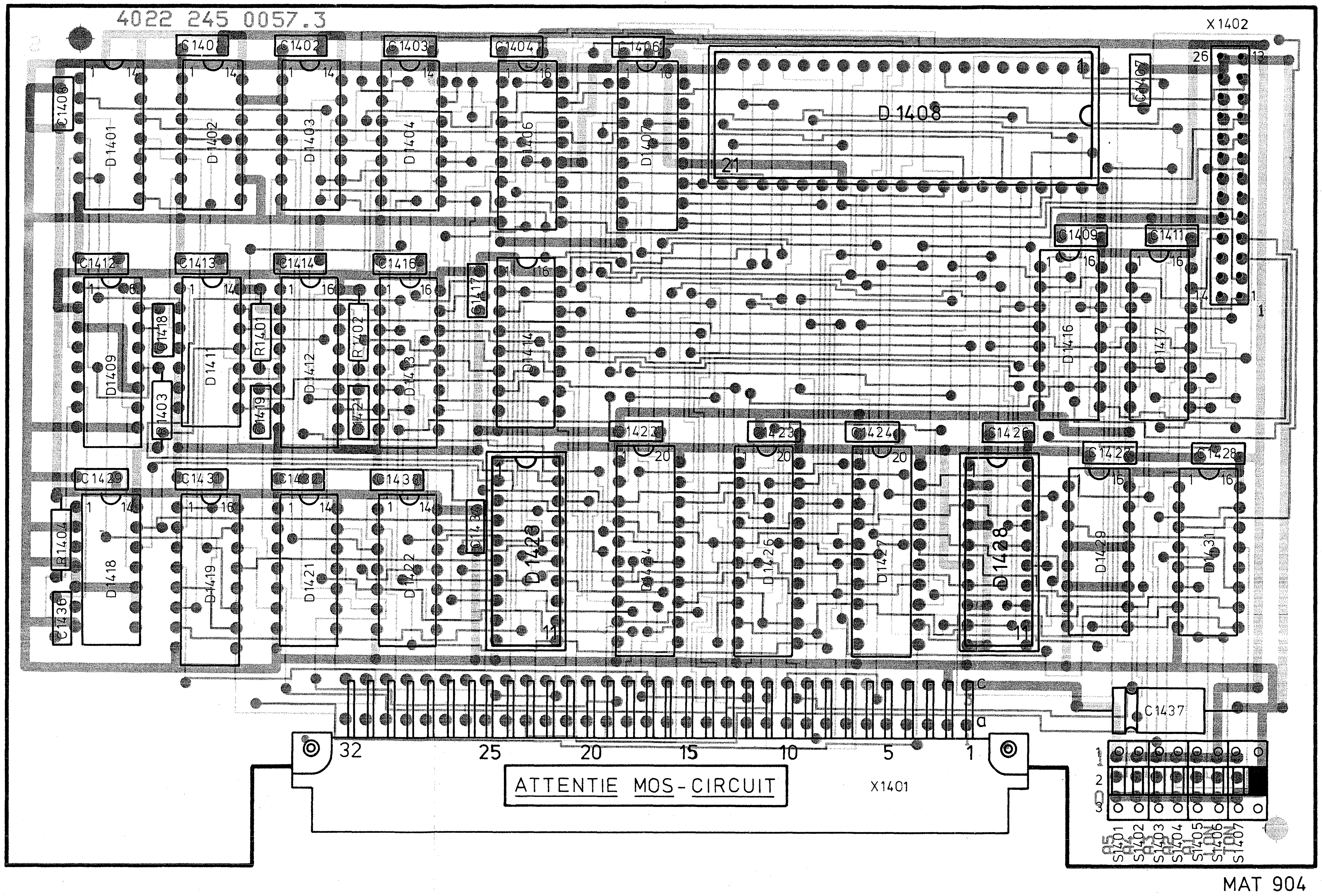
The PM3310 in combination with th PM3325 is capable to send status messages to a controller in case of an error condition. If the oscilloscope has such a message, it asks the attention of the controller by means of the Service Request (SRQ) line on connector X1402-pt11. The SRQ line becomes active after the C.P.U. has set the request for service bit of the control-signals latch D1426. All the connected instruments use the same SRQ line so the controller must check which of the instruments has caused the service request. This is called SERIAL POLLING therefore the controller must address the instruments one by one as talker and read the status-byte: The seventh bit of the status-byte indicates that the corresponding instrument has asked for service, the other bits give the status condition of the instrument.
The status word is built-up as follows:

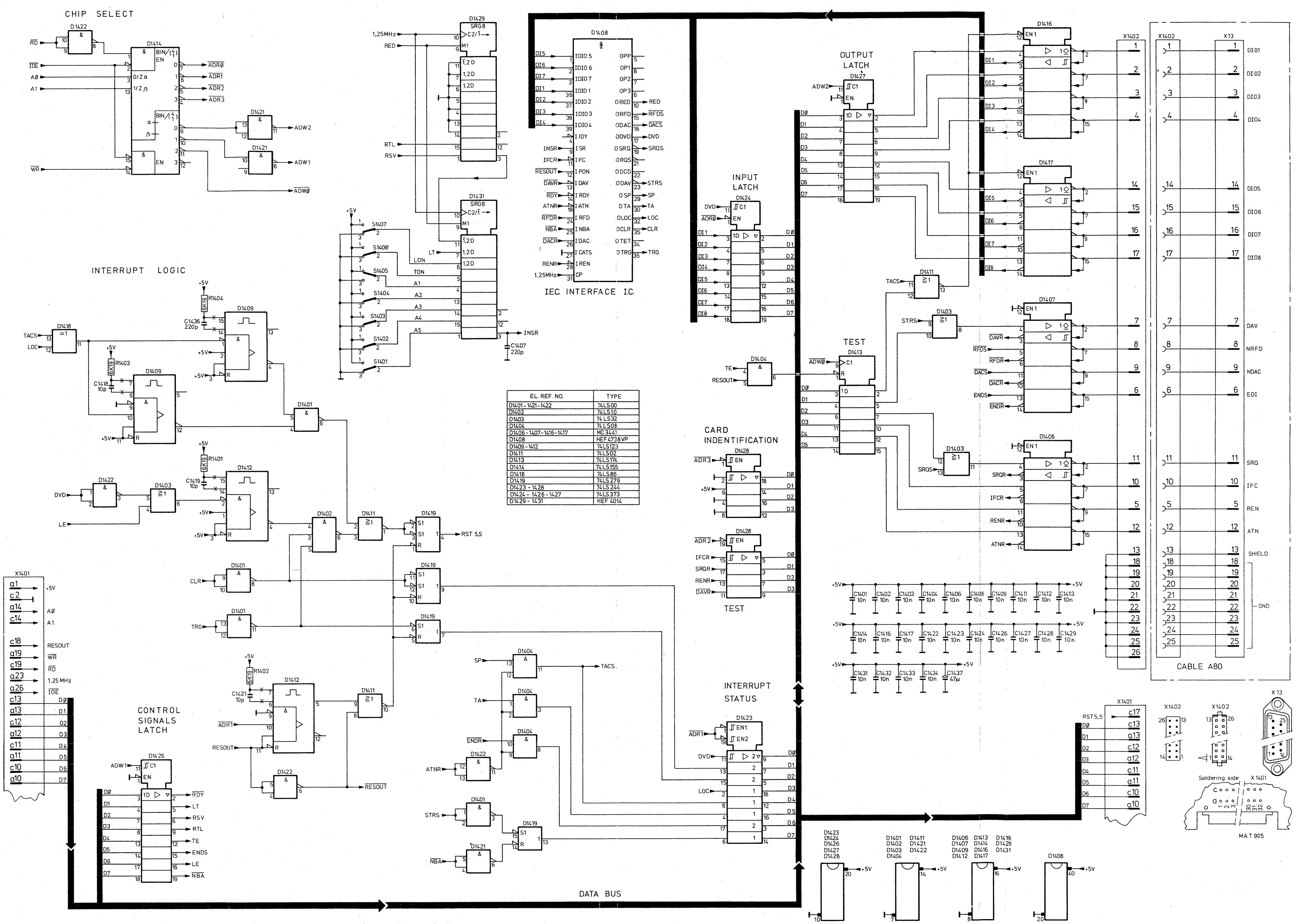
bit 8	Not used
bit 7... "1"	A SRQ has been given by the PM3310
"0"	No SRQ is given
bit 6 ..."1"	An ALARM is given to indicate that there is a fault condition.
"0"	No ALARM is given
bit 5 ..."1"	The PM3310 is busy with the programmed action
"0"	The PM3310 is ready with the programmed action
bit 4 ..."1"	Data on bus valid } not used for PM3310
'0"	Data on bus not valid
bit 3, bit 2, bit 1	Not used

The sequence of signals during an error condition is as follows.
First the C.P.U. activates the request for service signal of integrated circuit D1426 pin 6. The result is an active SRQ signal on connector X1402-pt11. The controller sends talk addresses, once become talker the C.P.U. puts the status-byte in the output latch and activates the signal new byte available (D1426 pin 19). Subsequently the PM3325 waits till NRFD (X1402-pt8) becomes high and then DAV (X1402-pt7) is made active (= low) and NRFD is reset by the controller.
When the controller has received the data, it makes the signal NDAC (X1402-pt9) high, the PM3325 answers with setting the DAV high and then the controller resets the NDAC signal.



I.E.C. BUS INTERFACE UNIT A14





EL. REF. NO.	TYPE
D1401 - 1421 - 1422	74LS00
D1402	74LS10
D1403	74 LS32
D1404	74 LS08
D1406 - 1407 - 1416 - 1417	MC 3441
D1408	HEF 4738VP
D1409 - 1412	74LS123
D1411	74LS02
D1413	74LS174
D1414	74LS155
D1418	74LS86
D1419	74LS279
D1423 - 1428	74LS244
D1424 - 1426 - 1427	74LS373
D1429 - 1431	HEF 4014

b. Focussing control

The electron beam is focussed using internal focus potentiometer R1588, which controls the emitter voltage of transistors V1539 and V1536. The signal is modulated by a frequency of 156 kHz applied to V1539 via diode V1552. On the collector of V1536 a signal is produced, the amplitude of which depends on the position of potentiometer R1588 (and R15 INTENS).

The a.c. voltage on the collector of V1536 is applied via symmetrical emitter-follower V1524, V1532, to a peak detector. This peak detector (C1521, V1514, V1513, R1516 and C1514) rectifies the a.c. voltage. Finally, this rectified voltage is added to the voltage set by potentiometer R1506 (part of a voltage divider network across the high-voltage converter output) and then applied to the focussing anode g3 of the c.r.t. In this way, the focus voltage also depends on the position of the INTENS potentiometer, which determines the voltage across the divider network R1502, R1506, R1509. This provides a measure of compensation, so that the focus of the electron beam is automatically adapted when the intensity of the trace is varied.

Illumination circuit

The graticule can be illuminated by the indicator lamps E1 and E2. The intensity can be varied by the front-panel ILLUM potentiometer R14, which controls the base, and hence the collector current of transistor V1561, which flows through the lamps. Note that the illumination circuit is not short-circuit proof.

Line signal circuit

The line signal circuit produces a sine-wave voltage for mains triggering that is derived from the input mains voltage.

Photocoupler D1602 on unit A16, which provides isolation between the mains voltage and the oscilloscope circuits, drives the V1564 circuit into saturation, which means that the square-wave voltage appearing on its collector has the same amplitude value for all mains voltages.

The original sine-wave is re-constructed by means of an integrator network R1553, R1551, R1536 and C1546, C1543, C1541.

This signal, LINE, is applied via V1523 and V1531 to the trigger selector.

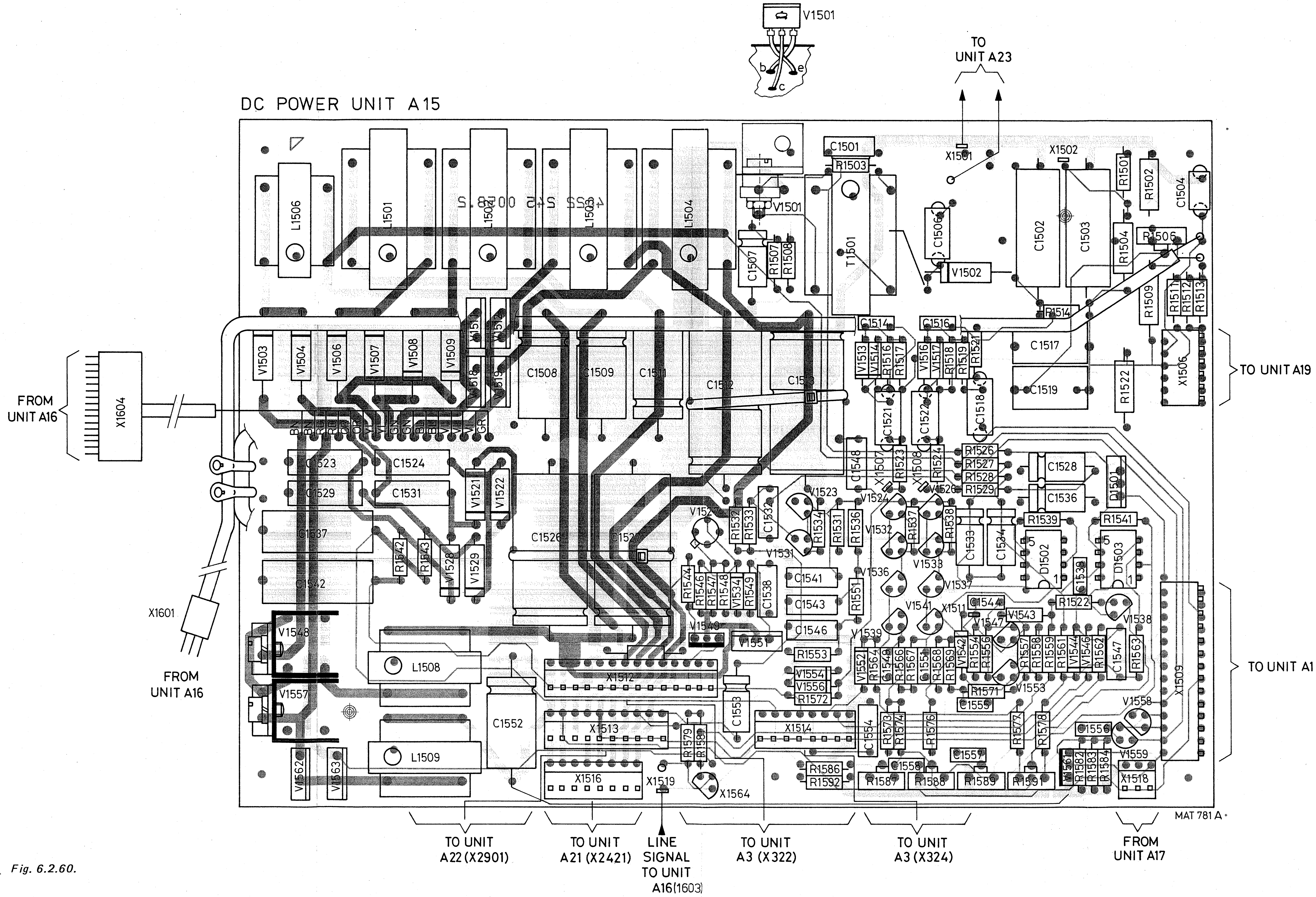

V1501
b
e
c
TO
UNIT A23
DC POWER UNIT A15
X1501
X1502
FROM
UNIT A16
X1604
TO UNIT A19
TO UNIT A1
X1601
FROM
UNIT A16
MAT 781 A
TO UNIT
A22 (X2901)
TO UNIT
A21 (X2421)
LINE
SIGNAL
TO UNIT
A16(1603)
TO UNIT
A3 (X322)
TO UNIT
A3 (X324)
FROM
UNIT A17

Fig. 6.2.60.

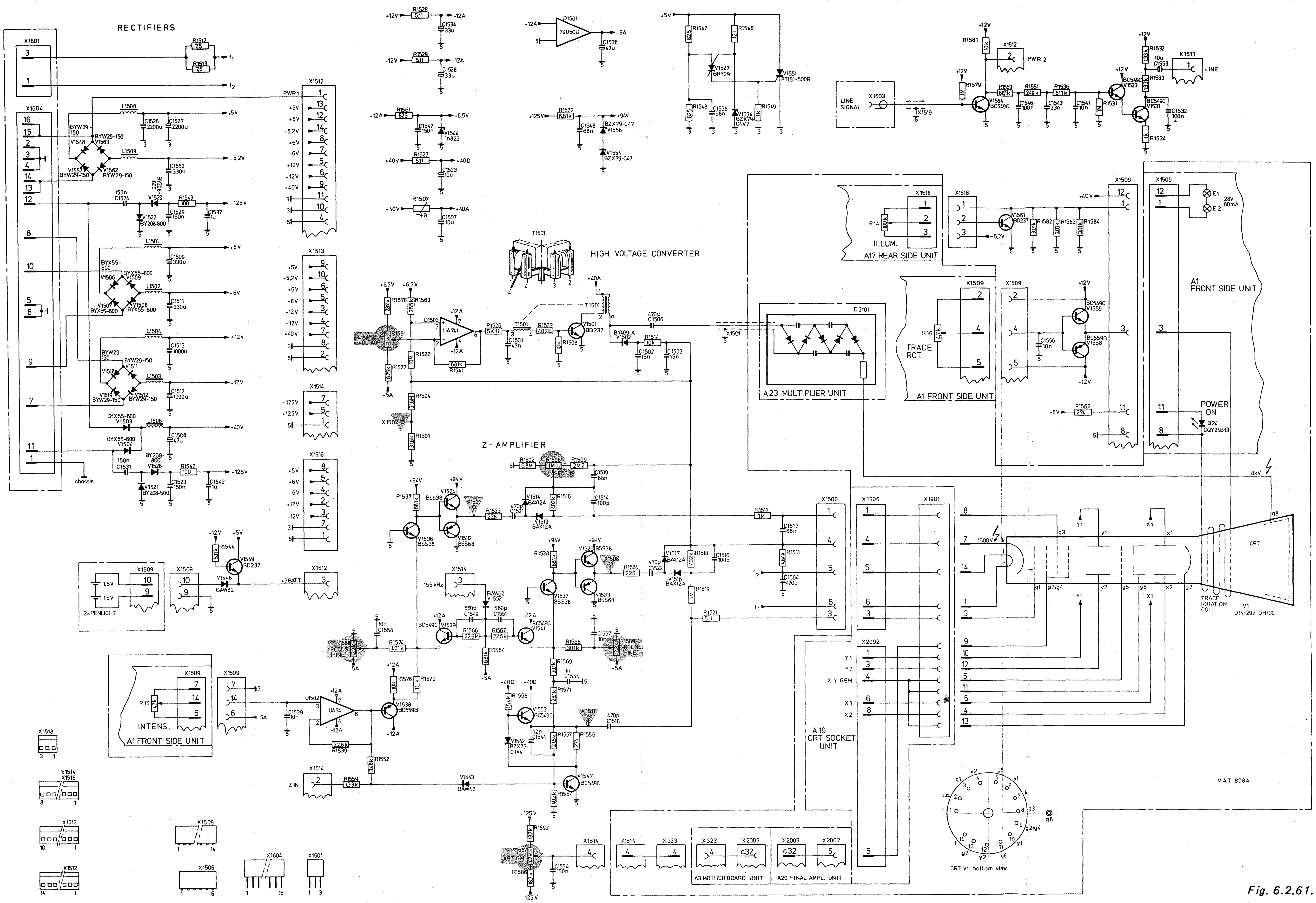

RECTIFIERS
HIGH VOLTAGE CONVERTER
Z-AMPLIFIER
CATHODE VOLTAGE
FOCUS
FOCUS (FINE)
INTENS (FINE)
ASTIGM.
ILLUM.
A17 REAR SIDE UNIT
TRACE ROT.
A1 FRONT SIDE UNIT
A23 MULTIPLIER UNIT
POWER ON
LINE SIGNAL
LINE
PWR 2
INTENS.
2×PENLIGHT
Z IN
CRT
TRACE ROTATION COIL
V1 D14-292 GH/39
A19 CRT SOCKET UNIT
X-Y GEM
A3 MOTHER BOARD UNIT
A20 FINAL AMPL. UNIT
CRT V1 bottom view
MAT 808A

Fig. 6.2.61.

6.2.16. A.C. power unit A16

The A.C. POWER UNIT comprises a bridge rectifier, a d.c. to a.c. converter regulator and a transformer. Rectifier circuits for the different supply voltages are located on D.C. POWER UNIT A15.

Input circuit

The incoming mains voltage is fed via a double-pole POWER ON/OFF switch S40, fuse F1701 (2 A delayed-action) and mains filter D1701 to the mains rectifier circuit.

This mains rectifier circuit can be matched to one out of two input voltage ranges (115 V or 230 V range) with the MAINS ADAPTER SWITCH S45 on the rear panel of the instrument.

The two-position switching enables the instrument to operate at any mains voltage between 100V and 120V ± 10 % (115 visible in MAINS ADAPTER SWITCH window) and between 220 V and 240 V ± 10 % (230 V visible in window).

Note: The same 2A delayed-action fuse is applicable for both settings of the mains adaptor switch.

The mains voltage is rectified with the diode bridge V1602 and smoothed by capacitors C1606 and C1604, which form a voltage doubler in the 115 V range of S45 and a standard bridge rectifier circuit in the 230 V range of S45.
The voltage across the series circuit of C1606 and C1604 is 250 V to 400 V for both mains voltage ranges.

Switching circuit

The unregulated d.c. voltage is applied in the form of pulses to a resonant circuit consisting of the primary coil of the converter transformer T1602, combined with C1602 and C1603, via switching transistor V1618.
The sine-wave voltage (approx. 800 V_{p-p}) across the primary coil of T1602 is kept constant by regulating the duty cycle of the base current of V1618.
The primary coil of T1601, which is in series with the switching transistor, limits the current through this transistor.
The energy stored in T1601 is fed back to the mains rectifier circuit, during the cut-off time of V1618, via diode V1601.
Diodes V1608 and V1609 eliminate the dissipation through transistor V1618 during the switching period; instead of this, these losses are dissipated in R1604 and R1603.
Diode V1617 improves the base drive for V1618.

Regulator circuit

The regulator circuit consists of integrated circuit D1601 (type TDA 1060), the output (pin 15) of which supplies a square-wave current with a variable duty-cycle to the base of transistor V1616. The signal on the collector of this transistor is applied to switching transistor V1618 via transformer T1603.
The regulator circuit is controlled by the following:

- Feedback voltage (pin 3)
  This is the regulator control voltage derived from the rectifier circuit in the feedback winding of T1602. The value of this control voltage depends on the setting of R1646.

- Feed-forward voltage (pin 16)
  This voltage is derived from the mains voltage and provides direct compensation for mains variation.

- Overvoltage protection (pin 13)
  A voltage is also derived from the mains voltage, via zener diode V1613, to inhibit the regulator output at excessive mains voltages (the level on pin 13 is 600 mV).

- Current limiting (pin 11)
  The voltage drop across the current-sense resistor R1627 controls the regulator circuit in the event of overload.

- Frequency adjustment (pin 7)
  The value of resistance between pin 7 and earth determines the converter frequency. Preset R1647 should be adjusted for a frequency of 20 kHz approximately, i.e. the resonant frequency of C1602, C1603 and the primary coil of T1602.

During normal working, the power supply for the regulator circuit is provided by the rectifier connected to the feedback winding of T1602. Transistor V1622 then conducts, therefore V1621 does not give any current output.

Switching-on and switch-on protection

At the moment of switching-on the instrument, no supply voltages are immediately available in the regulator circuit from T1602. Transistor V1622 is not yet conducting, therefore transistor V1621 is fully conducting and the regulator derives its current via R1616 and R1631. As soon as the converter circuit is working, transistor V1622 conducts and V1621 blocks.

In the event of the instrument giving no converter voltage at switch-on (due to a possible defect), the PTC resistor R1631 warms up and so reduces the current through transistor V1621 to a safe level.

Output circuits

Various supply voltages are derived from the secondary windings of transformer T1602. These supplies are generated on D.C. POWER UNIT A15.

Photocoupler circuit

To enable triggering on a mains signal, this circuit produces a signal derived from the mains voltage. Photocoupler D1602 provides isolation between the mains voltage and the oscilloscope circuits to produce a safe triggering signal. This output signal is applied to transistor V1564 on unit A15, which is driven into saturation to give a square-wave voltage on its collector. This square-wave has a constant amplitude for all mains voltages.

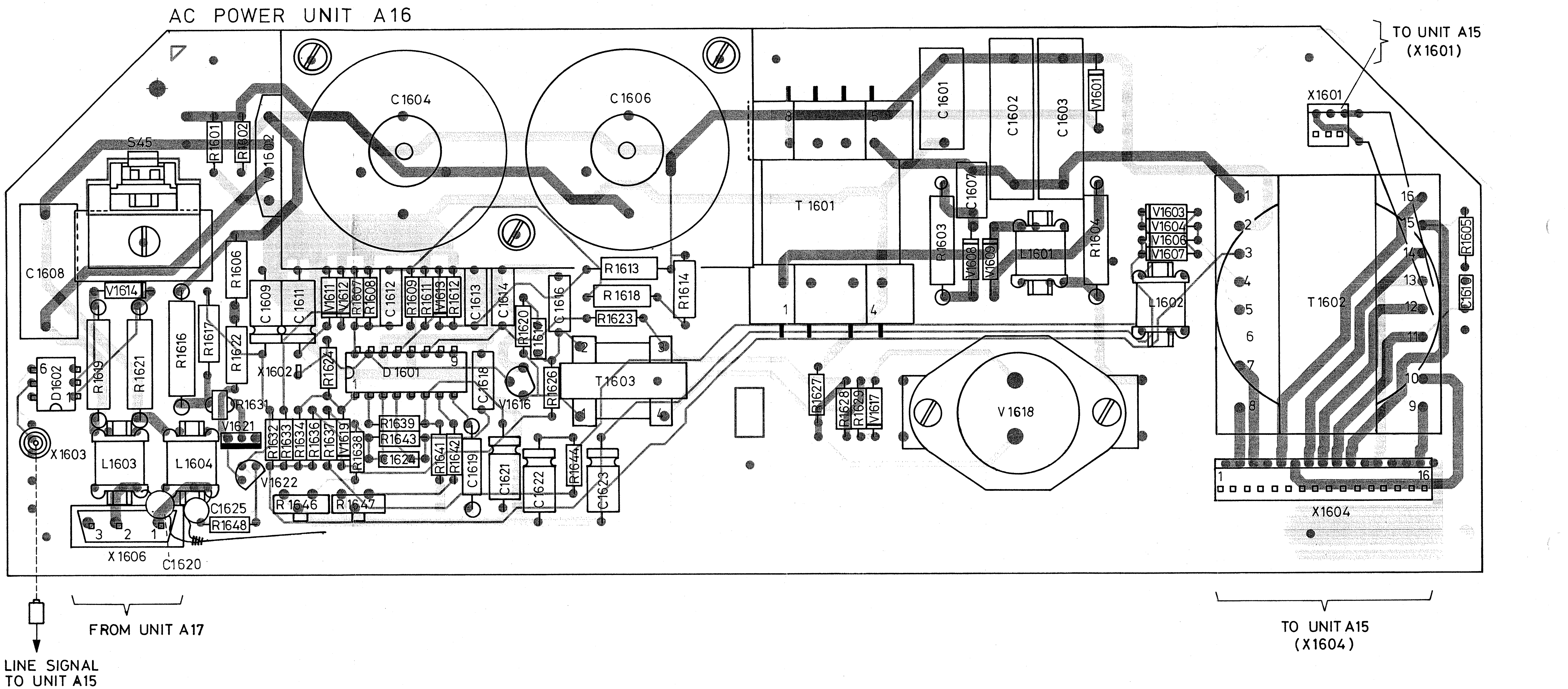
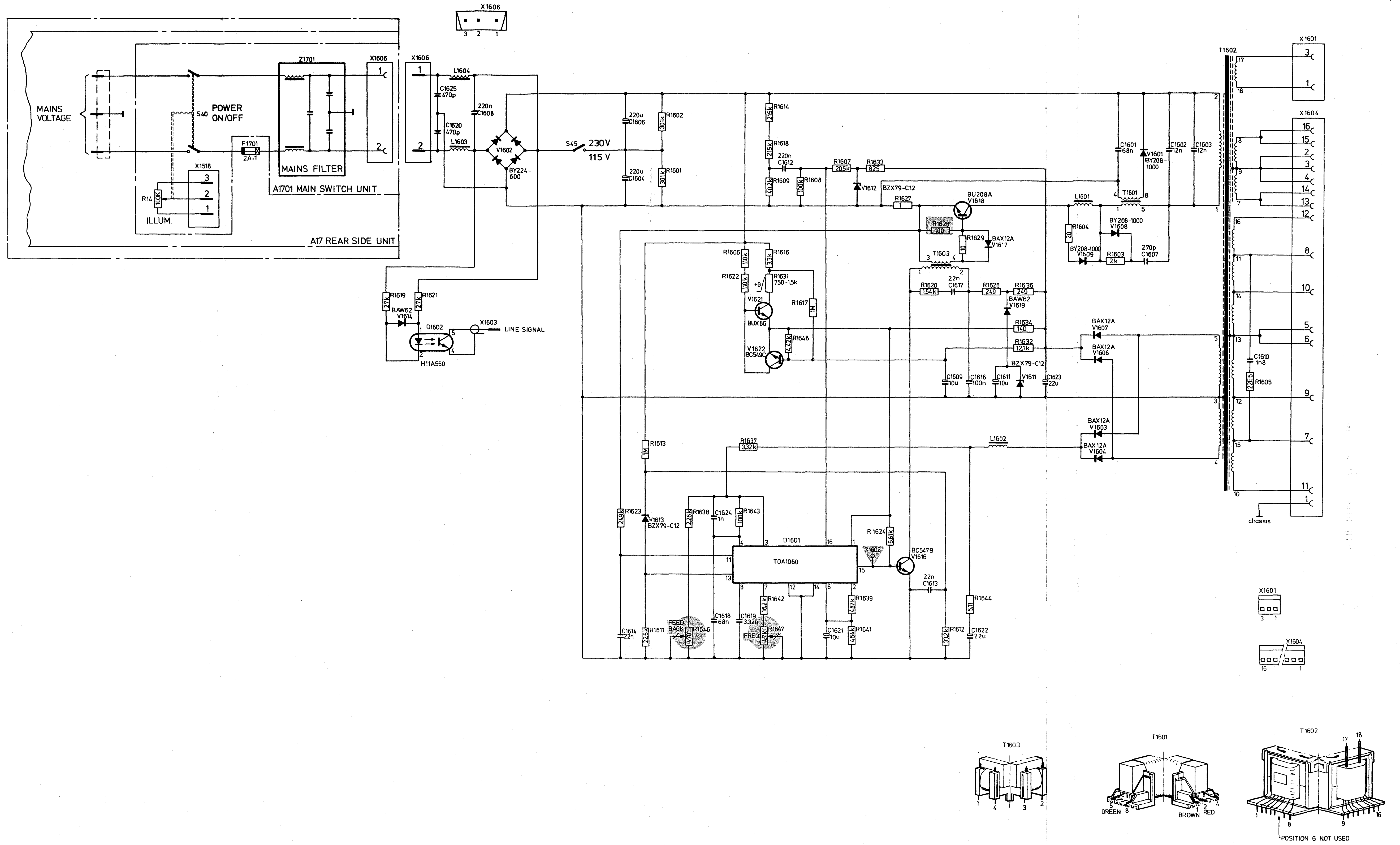

AC POWER UNIT A16
TO UNIT A15 (X1601)
X1601
C1604
C1606
C1601
C1602
C1603
V1601
T 1601
T 1602
X1604
TO UNIT A15 (X1604)
V 1618
T1603
D 1601
C1608
S45
X1603
L1603
L1604
X1606
C1620
FROM UNIT A17
LINE SIGNAL TO UNIT A15

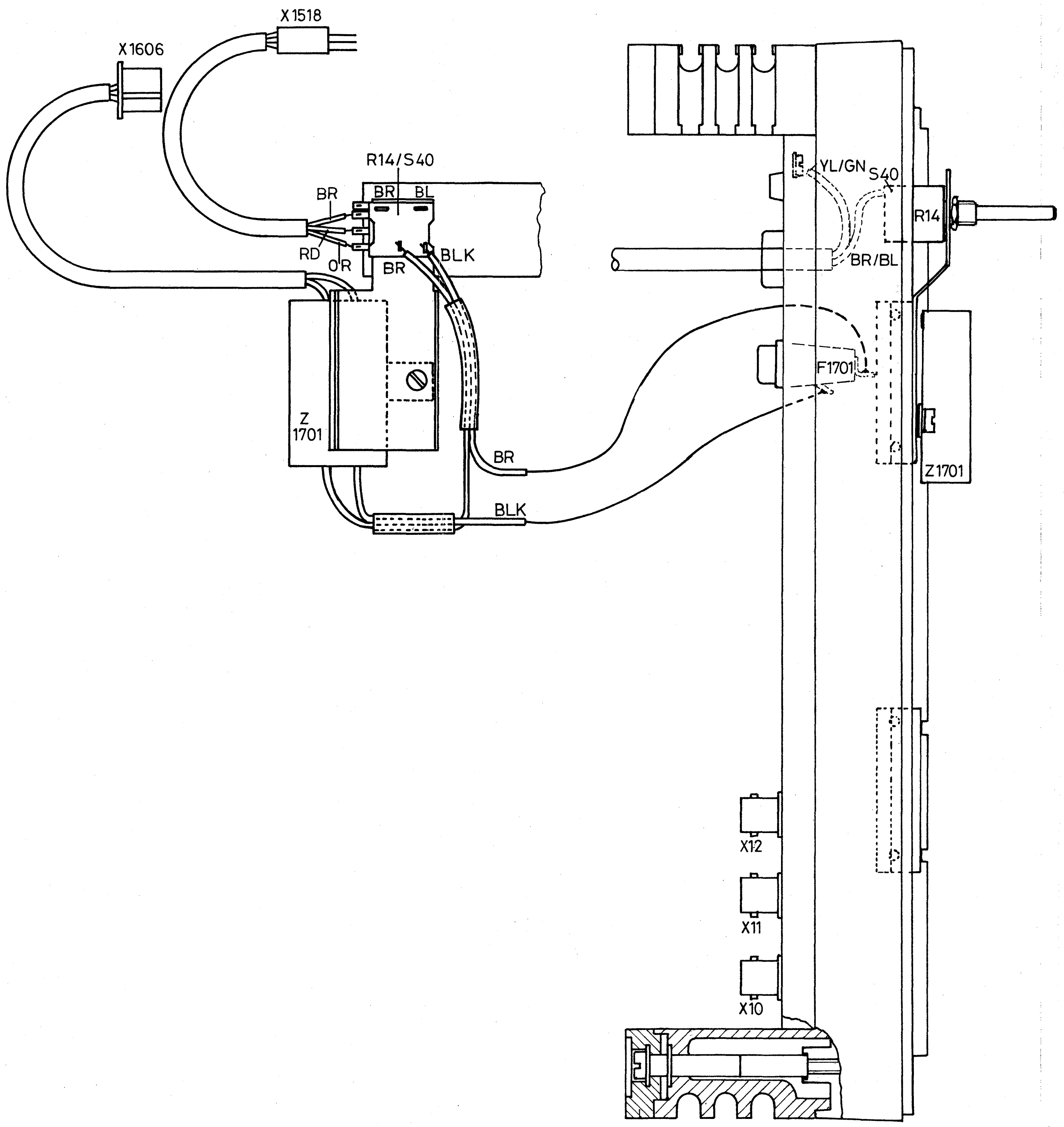
Fig. 6.2.62.



MAT 809A

Fig. 6.2.63.

A16 AC POWER UNIT



6.2.17. Rear side unit A17

The rear side unit consists of an aluminium rear cast on which the following items are mounted.

- ILLUM. control R14 - ON/OFF switch S40
- Mains filter Z1701
- BNC output sockets X10-X11-X12 for PLOT output signals
- Fuseholder F1701 and fuse.

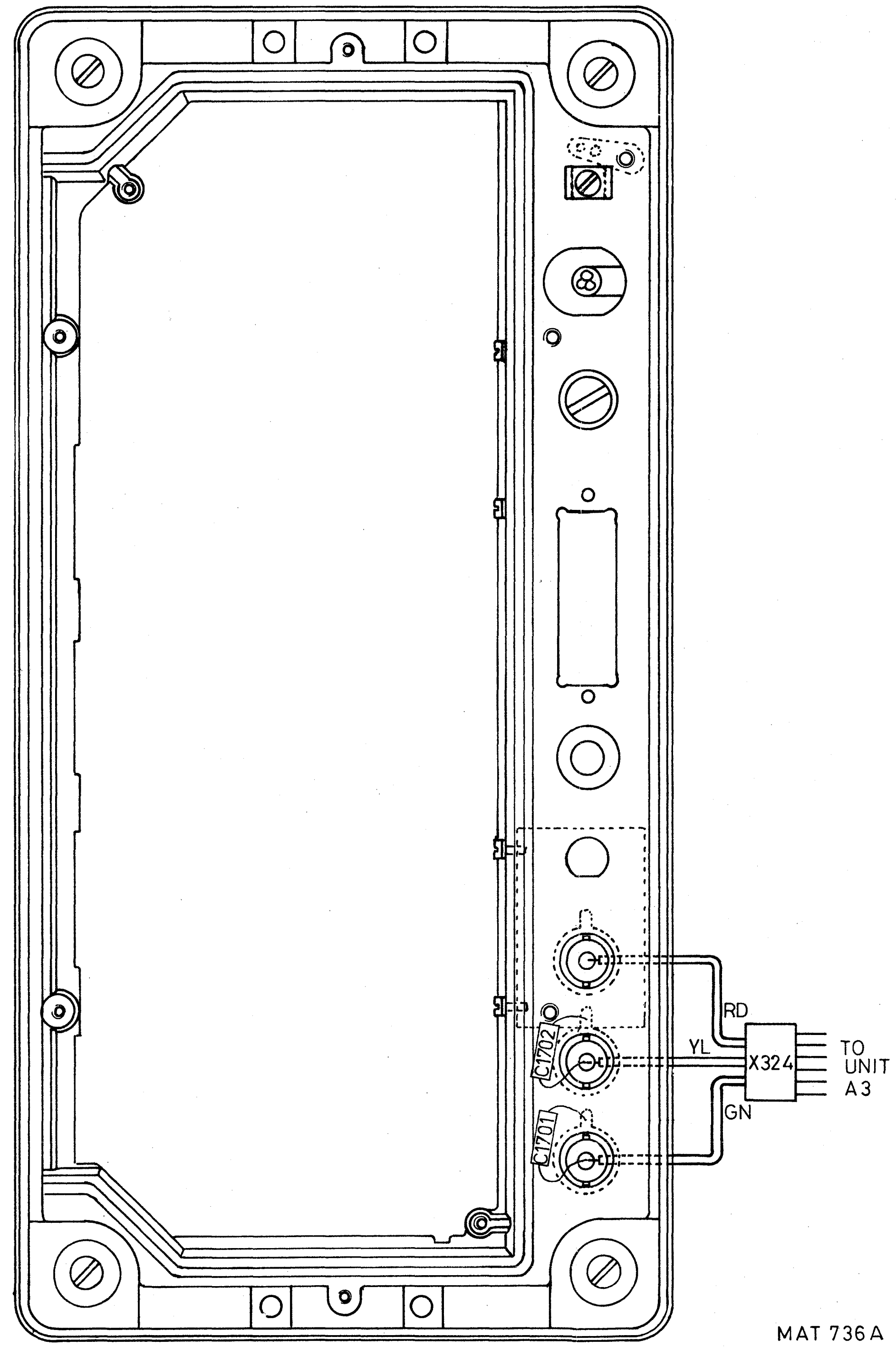


Fig. 6.2.64.

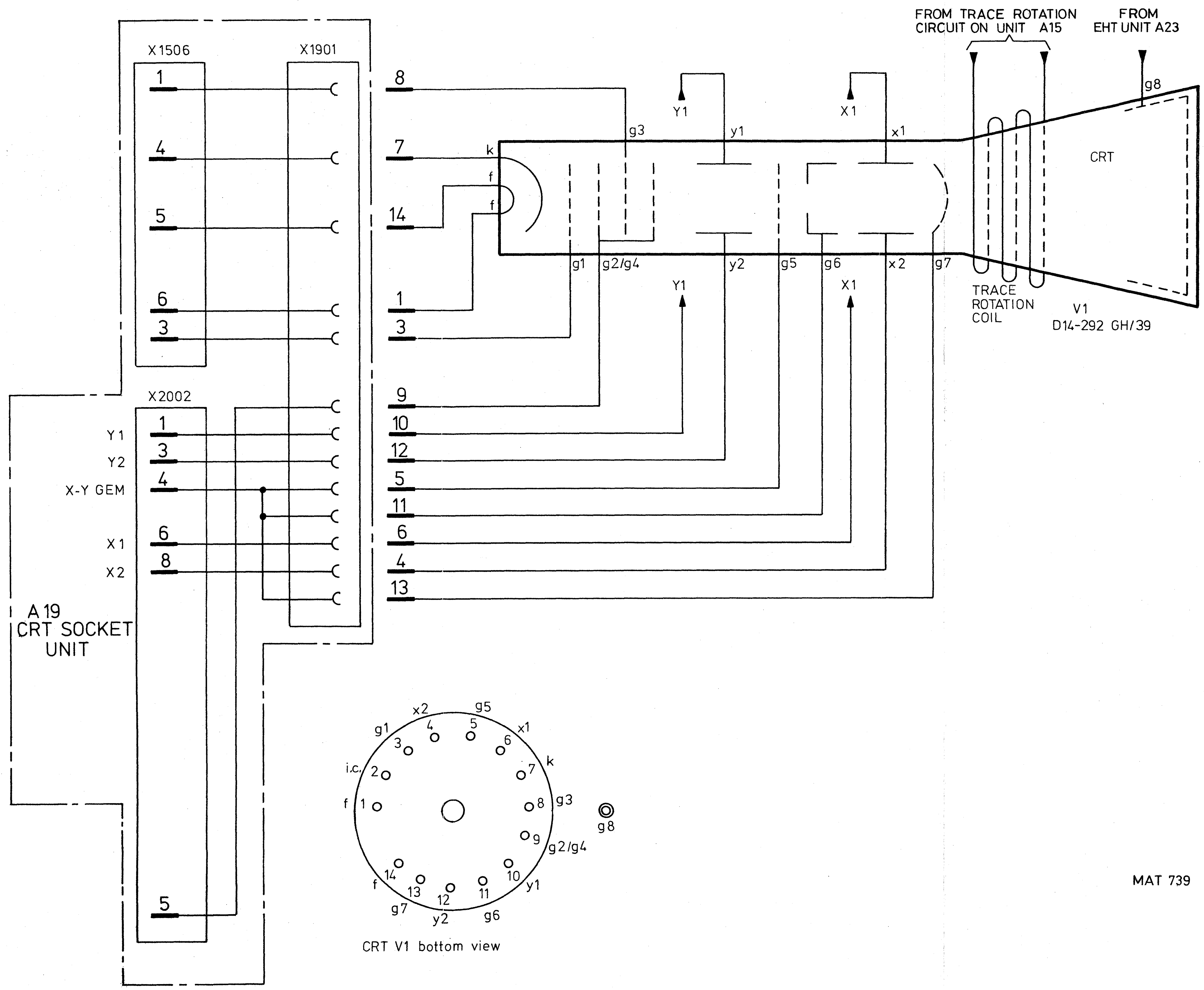

FROM TRACE ROTATION CIRCUIT ON UNIT A15
FROM EHT UNIT A23
X1506
X1901
X2002
Y1
Y2
X-Y GEM
X1
X2
A19 CRT SOCKET UNIT
CRT
TRACE ROTATION COIL
V1 D14-292 GH/39
g1
g2/g4
g3
g5
g6
g7
g8
y1
y2
x1
x2
k
f
i.c.
CRT V1 bottom view
MAT 739

Fig. 6.2.68.

INCOMING SIGNAL	OUTGOING SIGNAL	GENERATED ON UNIT	USED ON UNIT	DESCRIPTION
ASTIGM	ASTIGM	A15	A20	Astigmatism
$\overline{\text{AVSB}}$		A13		Logic 0 in X = A/Y = B mode
DJ		A13		Dot join signal
ENKEL		A13		Single channel mode
$\overline{\text{OERØ}}$		A6		Output enable RAMØ
$\overline{\text{OER1}}$		A6		Output enable RAM1
$\overline{\text{OER2}}$		A6		Output enable RAM2
POSØ		A202		Slider of ACCU position control
POS1		A202		Slider of STO1 position control
POS2		A202		Slider of STO2 position control
POS3		A202		Slider of STO3 position control
QØ		A13		Control signal for dot join
Q1		A13		Control signal for dot join
RESDJ		A13		Reset dot join
TRSH		A13		Trigger for dot join sample and hold
	X1	A20	A19	Horizontal deflection signal
	X2	A20	A19	Horizontal deflection signal
XDAC		A6		Horizontal DAC output signal
XMAGN		A202		Slider of X MAGN control
	XOUT	A20	A13	Horizontal output signal
XPOS		A202		Slider of X POSITION control
	X-Y GEM	A20	A19	Geometry control signal
	Y1	A20	A19	Vertical deflection signal
	Y2	A20	A19	Vertical deflection signal
YDAC		A6		Vertical DAC output signal
YEX		A13		Y-expand
	YOUT	A20	A13	Vertical output signal
ZDJ		A13		Z dot join
2.5 kHz		A12		
+5 V		A15		
+6 V		A15		
−6 V		A15		
+12 V		A15		
−12 V		A15		
+40 V		A15		
+135 V		A15		
−135 V		A15		
⏚		A15		

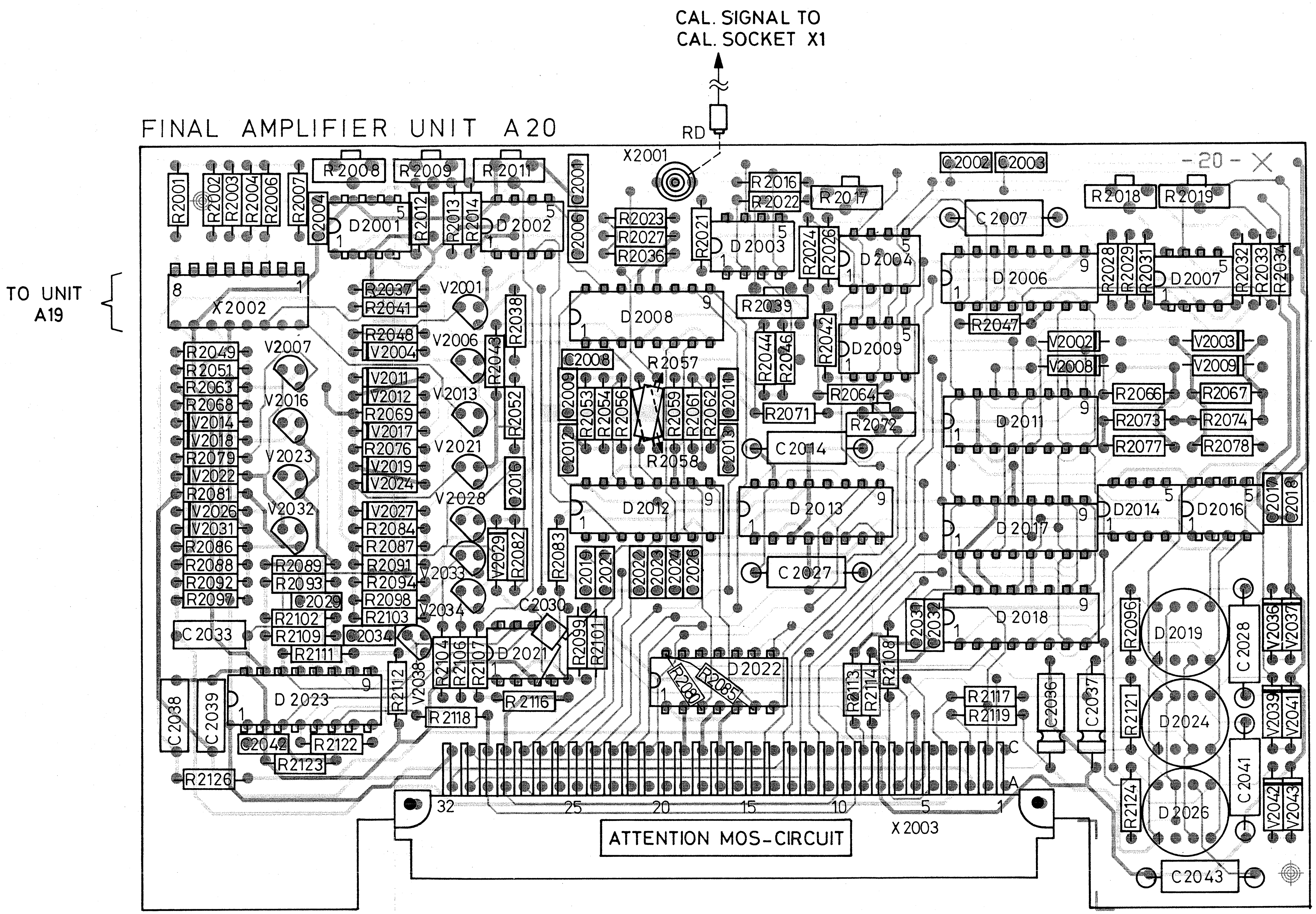
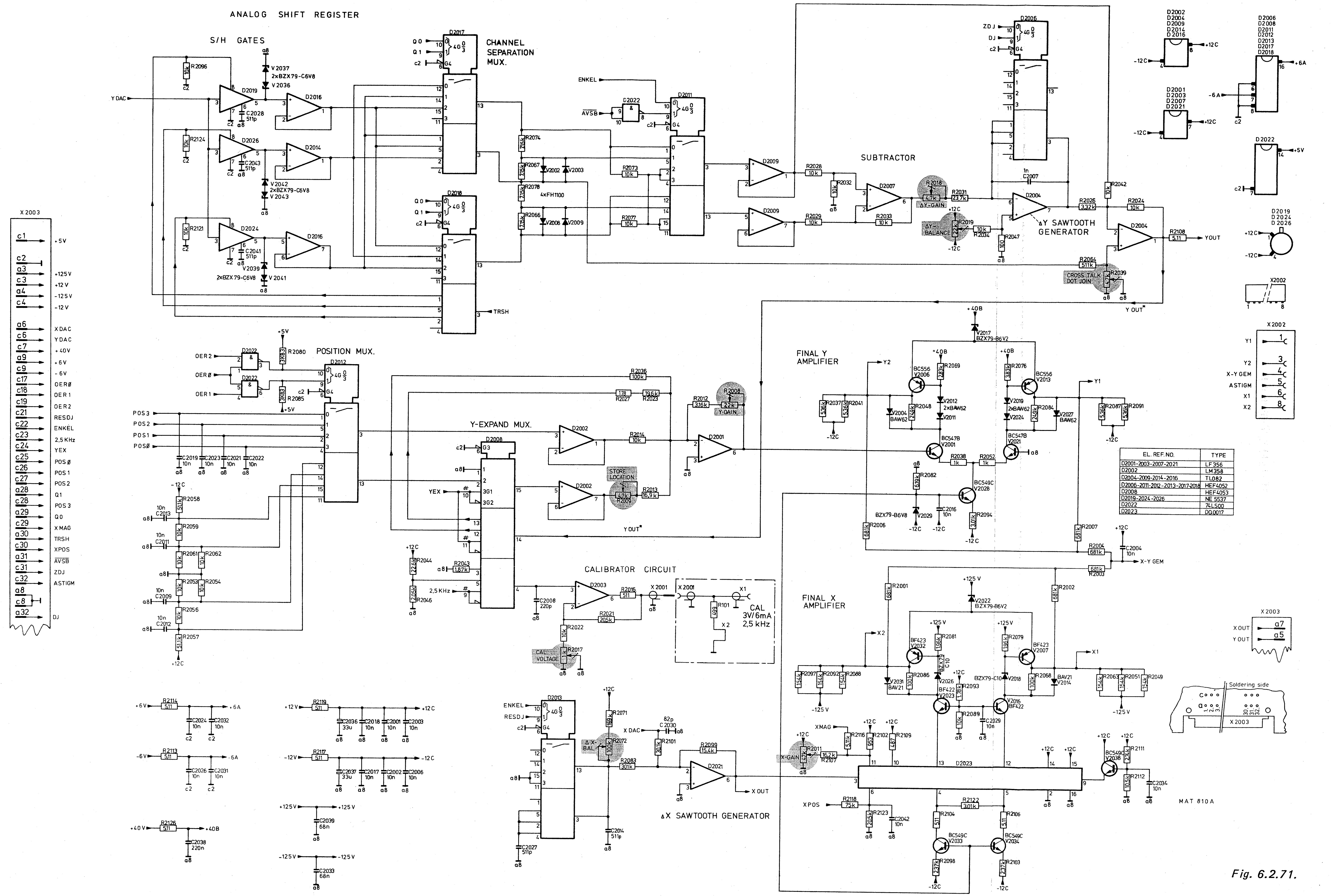


Fig. 6.2.70.

MAT 784 A



EL. REF. NO.	TYPE
D2001-2003-2007-2021	LF356
D2002	LM358
D2004-2009-2014-2016	TL082
D2006-2011-2012-2013-2017-2018	HEF4052
D2008	HEF4053
D2019-2024-2026	NE 5537
D2022	74LS00
D2023	DQ0017

Fig. 6.2.71.

6.2.21. Input amplifier unit A21

6.2.21.1. General

The input amplifier unit is sub-divided into the following sections, as shown in the block diagram.
- Input attenuator
- Amplifier
- Channel switch and mode switch
- Delay line compensation/Track & Hold gate
- Logic circuits (control interfaces)

Briefly, the channel input attenuator reduces the input signal according to the front-panel switch settings or remote signals, and converts it from high to low impedance.
The asymmetrical output signal is applied to the amplifier section to give a symmetrical output, an amplified trigger pick-off and an offset facility. A buffer stage provides for signal inversion and offset before feeding the channel and mode switch section. Here the logic control signals are used to switch the appropriate channels and display modes to the ADC in the storage section of the oscilloscope.

6.2.21.2. Input attenuator

The input stage comprises two identical attenuator circuits. For convenience, only the channel A attenuator is described.

The input signal can be either a.c. or d.c. coupled (via C2476 or K2412) to the attenuators.

Basically, the input attenuator comprises a triple high-ohmic voltage divider and an impedance converter in conjunction with a drift correction circuit. The impedance converter (V2451, V2448) provides a zero level output, adjusted by potentiometer R2643, which feeds a low-ohmic attenuator.

Overall, the attenuation of the input stage is determined by the combination of the selected sections of the two attenuators, according to the setting of the front-panel AMPL/DIV switch. The control sequence is as follows:

The position of the AMPL/DIV switch, the AC/DC switch and the '0' switch are decoded and applied to the reed relays and FET switches (D2411) via the microprocessor system. The reed relays and the FET switches determine the position of the attenuators and are controlled from two 8-bit output ports (D2424, D2426) in the logic circuit. These output ports are controlled via the data-bus and can also be controlled by the IEC-bus interface for remote operation.

The three sections of the high-ohmic voltage divider have an attenuation factor of 1.25, 12,5 and 125 times.

If the front-panel pushbutton '0' is depressed, reed switch K2411 closes and all other reed switches are open. Control for this action is via the output ports of the microprocessor system. With K2411 closed, the input signal is not connected to the attenuator and the impedance converter, via R2668 and R2578, is switched to zero level.

The low-ohmic voltage divider, following the input impedance converter, attenuates 1, 2 or 5 times. Taking the overall combinations, together with the 1 or 10 times gain of the intermediate amplifier, twelve different deflection coefficients can be chosen.

To obtain the correct frequency characteristic, the attenuator sections are shunted by capacitors. Trimming capacitors provide for the adjustment of the capacitive divider sections for a.c. voltages to the same ratio of the resistive dividers for d.c. voltages. In this way, the divider sections are independent of frequency.
A diode clipper in the gate circuit of the field-effect transistor (FET V2451) protects it against excessive negative swings, the FET being inherently protected against excessive positive swings.

The high frequency path for the input signal consists of series capacitor C504 and the FET connected in a source-follower configuration. The low-frequency path comprises an operational amplifier and an error amplifier, which corrects the output signal related to the input signal of the impedance converter over a frequency range from d.c. to 1 kHz. The output of the error amplifier (D2416) is fed to the input of the operational amplifier to replace the missing low frequency portions of the signal. In this way, the drift is reduced to a minimum.

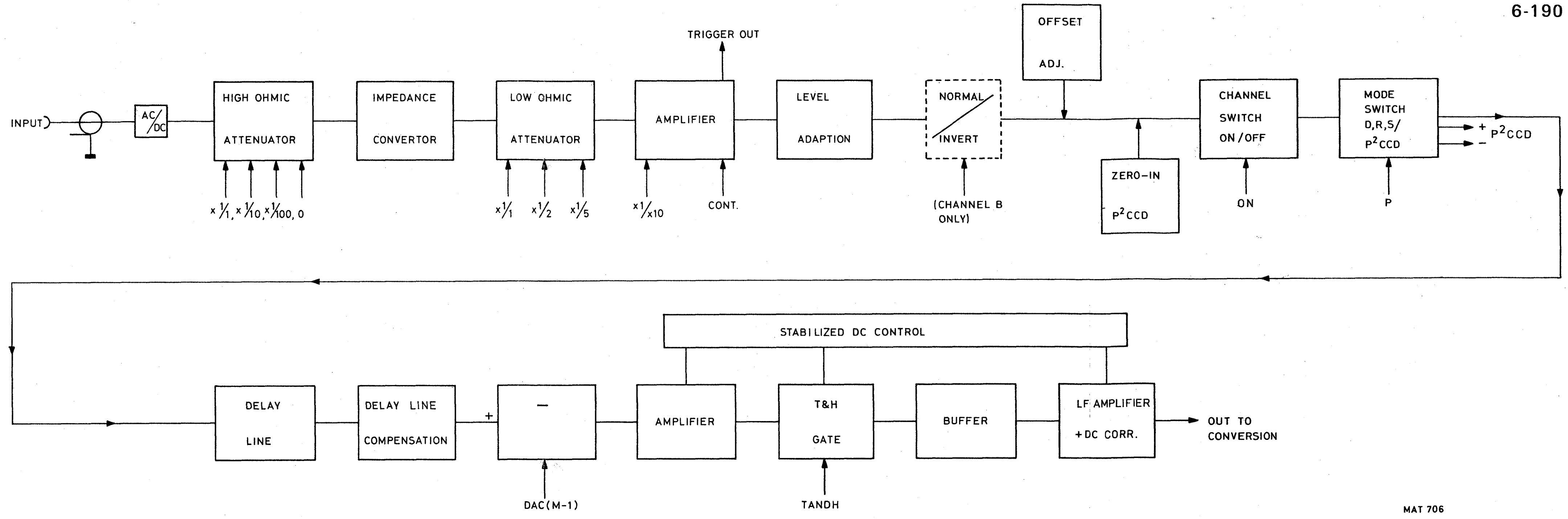


Fig. 6.2.72.

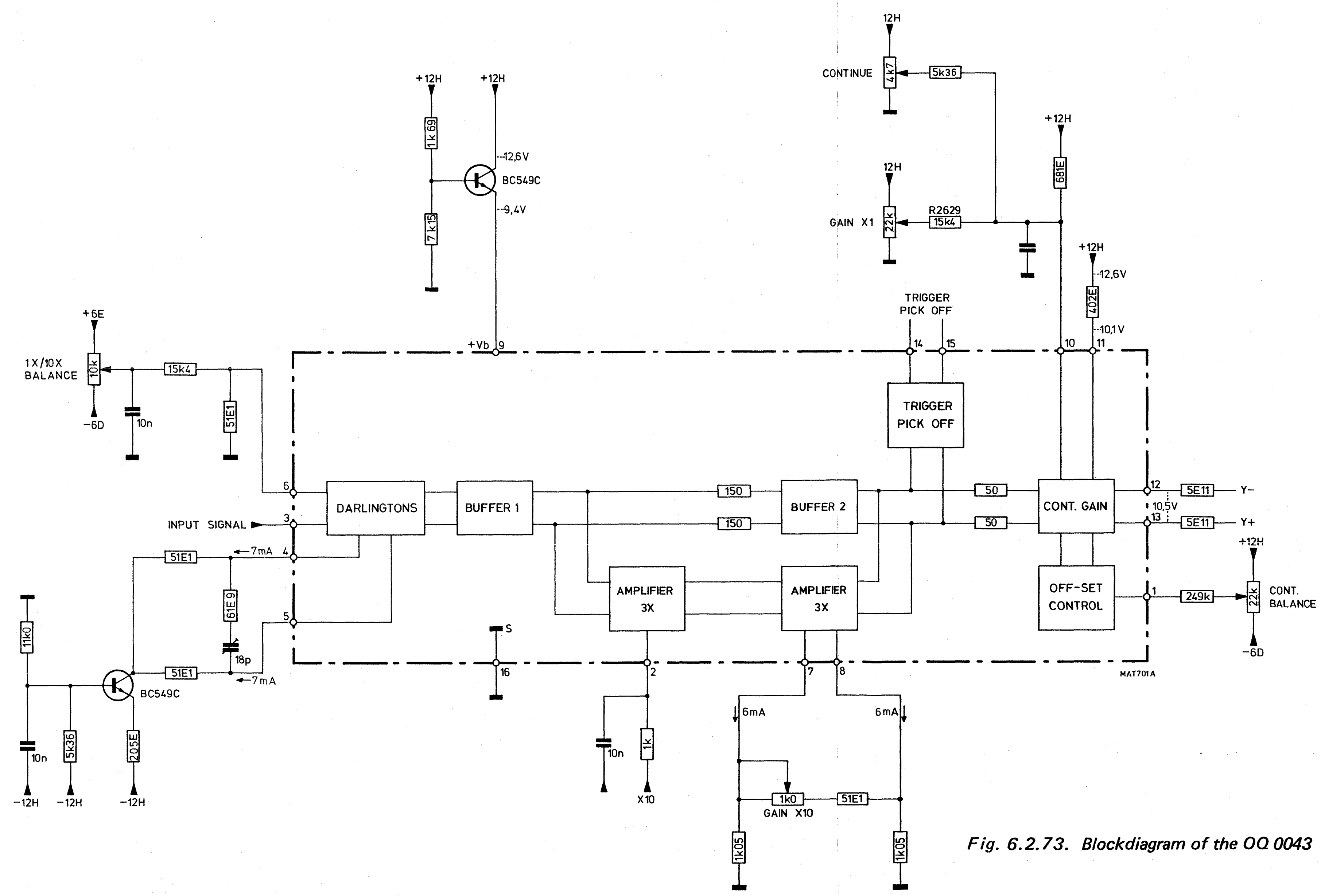


Fig. 6.2.73. Blockdiagram of the OQ 0043

The output of the impedance converter is applied to the 1, 2 or 5 times voltage divider. The dividing factors are controlled by FET switches (D2411), which in turn are controlled, via operational amplifiers (D2421), by the output ports of the microprocessor system.

6.2.21.3. Amplifier

a. Pre-amplifier

The output of the 1-2-5 divider stage is asymmetrically applied to pin 3 of pre-amplifier D2413 (OQ 0043) The block diagram of the OQ 0043 is given in the figure and is drawn with the relevant components as mounted in this oscilloscope.

The supply voltage is routed via a temperature-compensating circuit connected to pin 9. The OQ 0043 consists of input Darlington pairs to provide a symmetrical signal from the asymmetrical input; a buffer stage; two x3 amplifiers in series and switched in parallel to a buffer stage; trigger pick-off after amplification; a continuous gain adjustment facility and an offset adjustment for the continuous control.

b. Buffer stage

The output of the OQ 0043 is symmetrically applied to a buffer stage. In order to obtain the inverting mode for Channel B (PULL FOR –B), the buffer stage in this channel is provided with two extra transistors (V2419, V2424).
If the channel B invert switch is pulled, the microprocessor system decodes this setting and applies a high voltage to the base of V2408, which conducts.
Consequently, transistors V2418 and V2426 switch off and V2419 and V2424 now conduct so that the signal path is inverted.

After this stage, an offset stage, adjustable from the front panel, adapts the current so that an offset adjustment of four times the voltage range is possible (OFFSET A - V2456; OFFSET B - V2414).

To obtain the facility for switching both A and B channels to zero, necessary in the P^2CCD mode (see Section 6.2.8.3), both current flows are switched to the supply voltage via transistors V2469 and V2473. To control the zero switching, the Acquisition Control Logic and the time-base system generate the signals NUL IN and P respectively. These signals are applied to a NAND gate, the output of which is fed to operational amplifier D2422 (pins 8, 9 and 10). A zero on the negative input results in a high level on the output and the transistors conduct, thus interrupting the signal current flow.

6.2.21.4. Channel switch and mode switch

The principle of this oscilloscope is such that the channel A and channel B signal is always stored in the chopped mode. The CHOP signal, which is derived from the acquisition control logic (A9), is applied to the channel switch via NAND gates (D2428, D2429 on the logic circuit) to determine the positions of the ON/OFF switches. The signals derived from the control gates are called A ON and B ON, these signals being applied via V2468 (V2428) to pins 9 and 11 of D2412 (D2404). If the signal ON is high, the transistor blocks, and via V2474 (V2433), the outer transistors on the right-hand side of D2412 (D2404) become conductive. If the signal ON is low, V2468 (V2428) is conductive and the inner right transistors become conductive, the signal current flow of Y+ and Y– is shunted via pins 13 and 15 of D2412 (D2404), so the channel is switched off.

The following switching modes are indicated in the figures:

– Channel A ON: similar to channel A P^2CCD mode } except for switching in D2409
– Channel B ON: similar to channel B P^2CCD mode }
– Channel A and B ON in ADD mode
– Dual channel P^2CCD mode (chopping is effected in P^2CCD)

In all modes except P^2CCD, chopping is effected by the channel switch.

To obtain a constant load for the supply voltages of the channel switch, it is necessary that the current remains the same, irrespective of the mode selected. Hence the reason for the alternative transistor loads. The relevant current paths are shown in the figures.

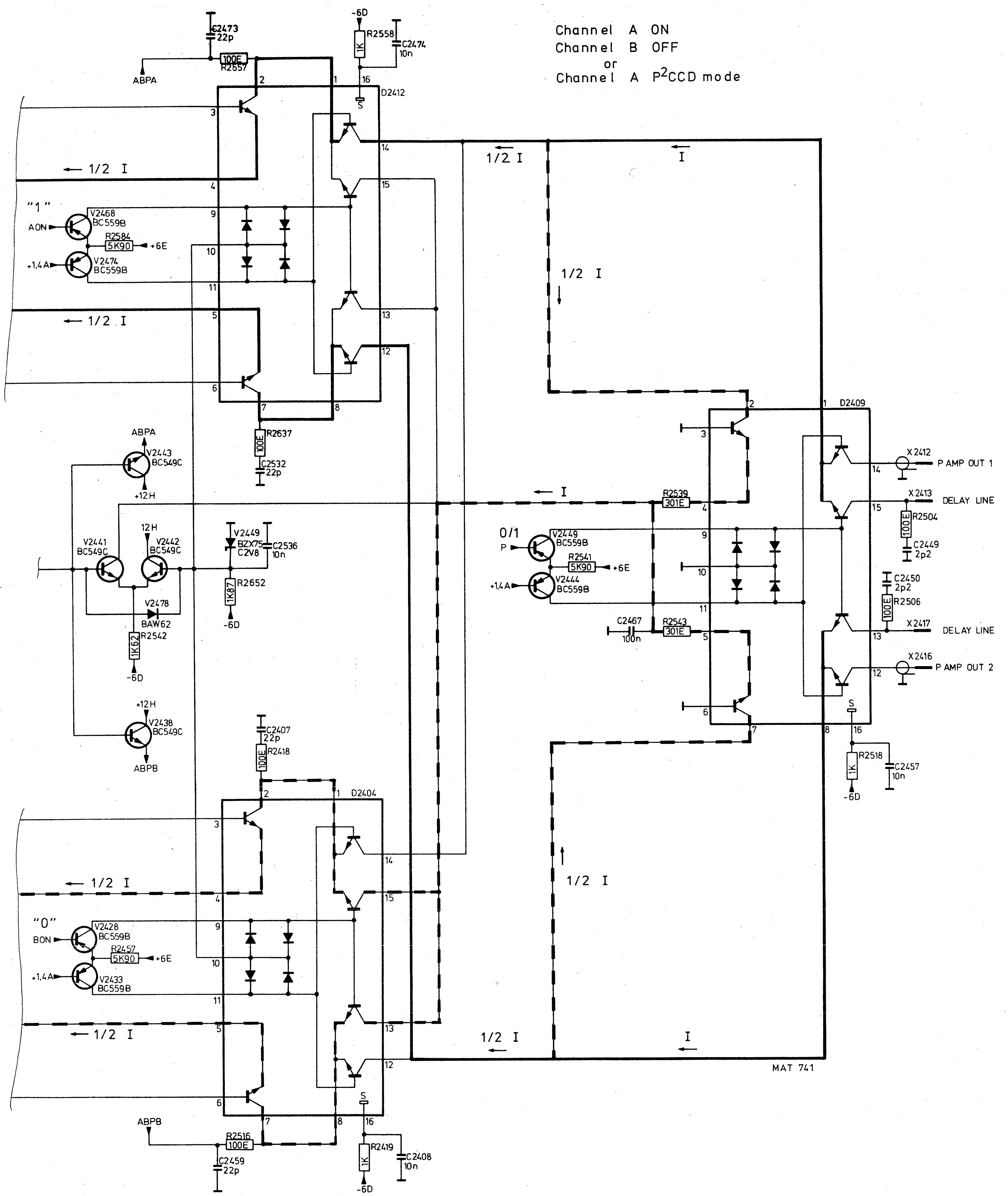


Fig. 6.2.75.

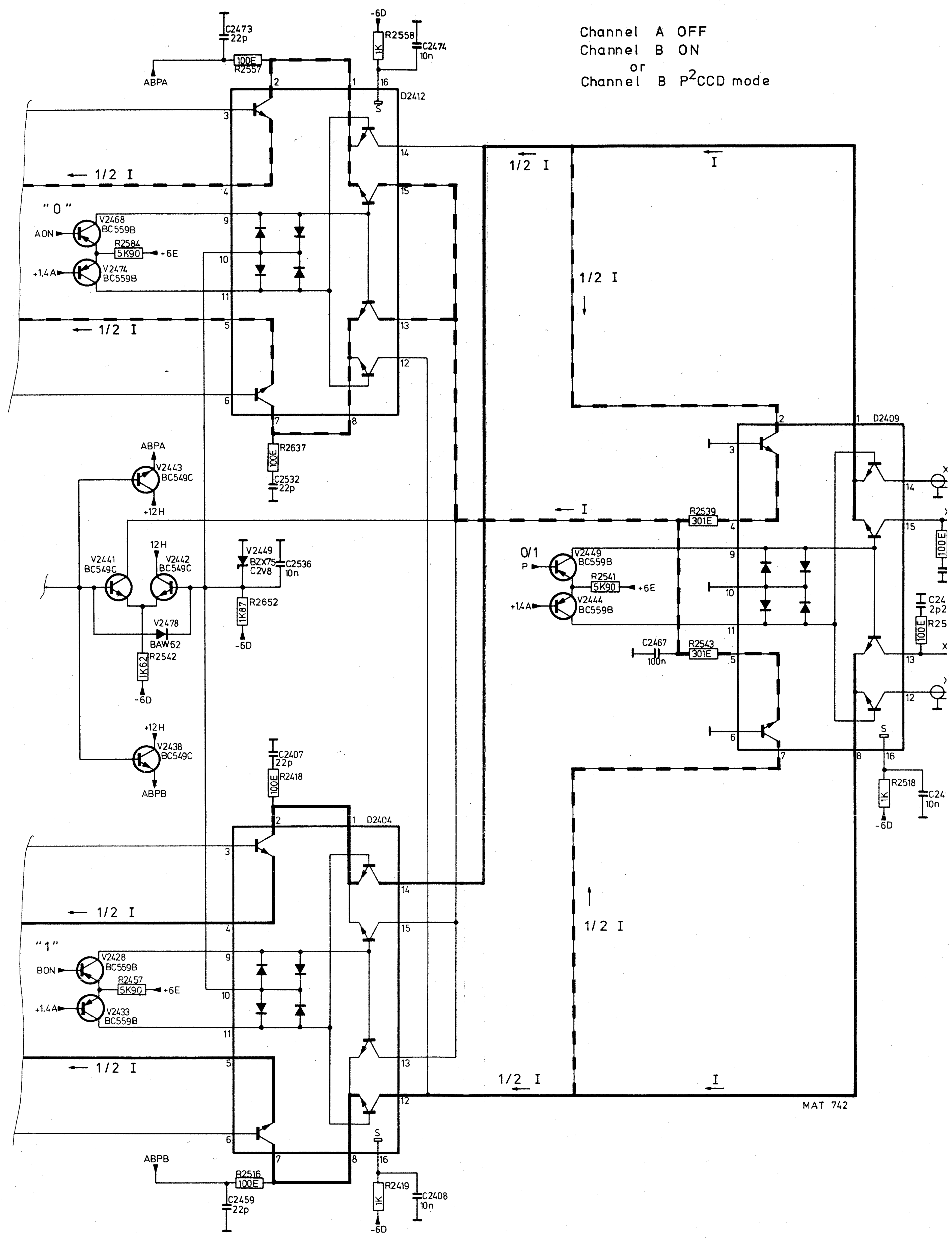


Fig. 6.2

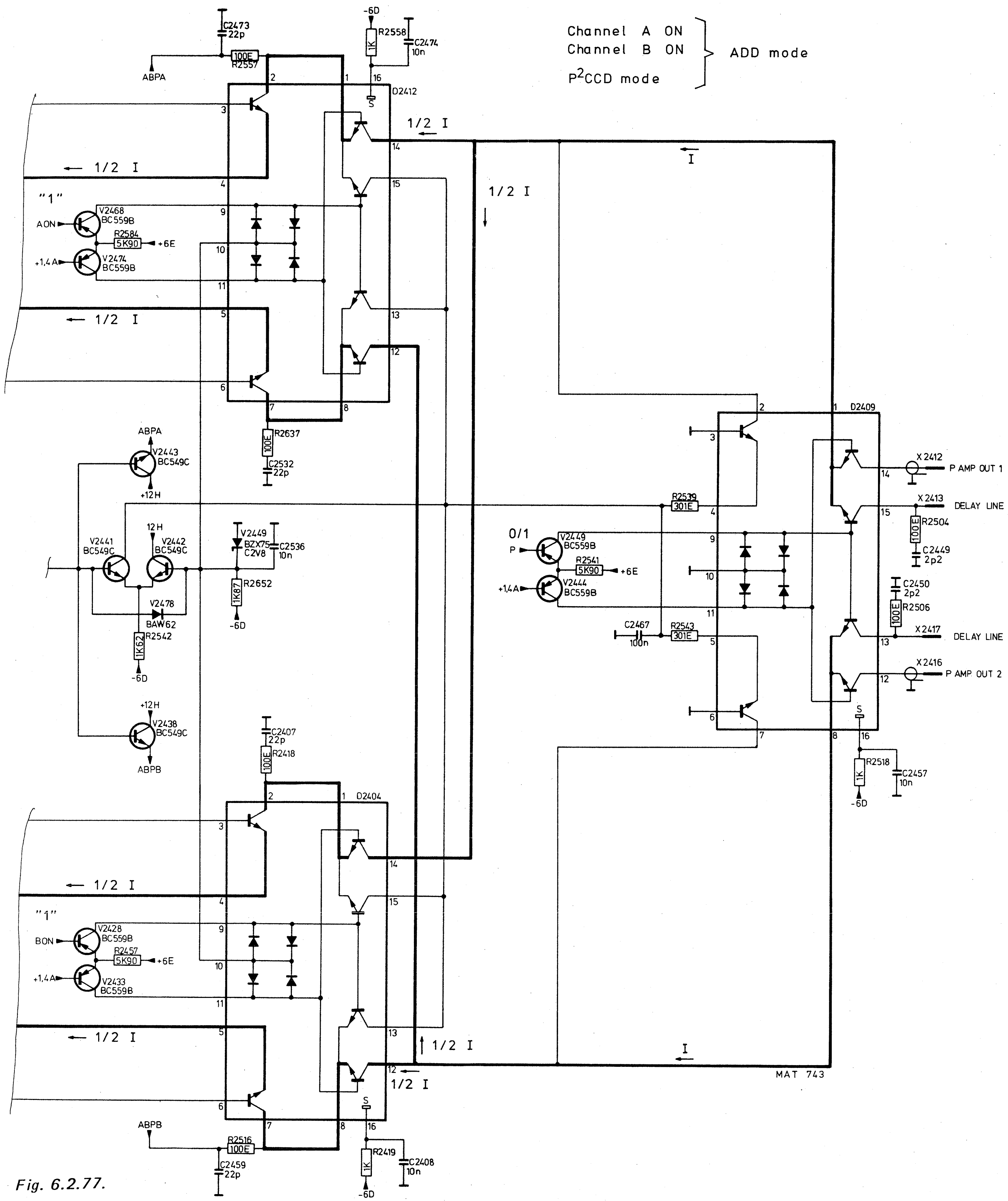


Fig. 6.2.77.

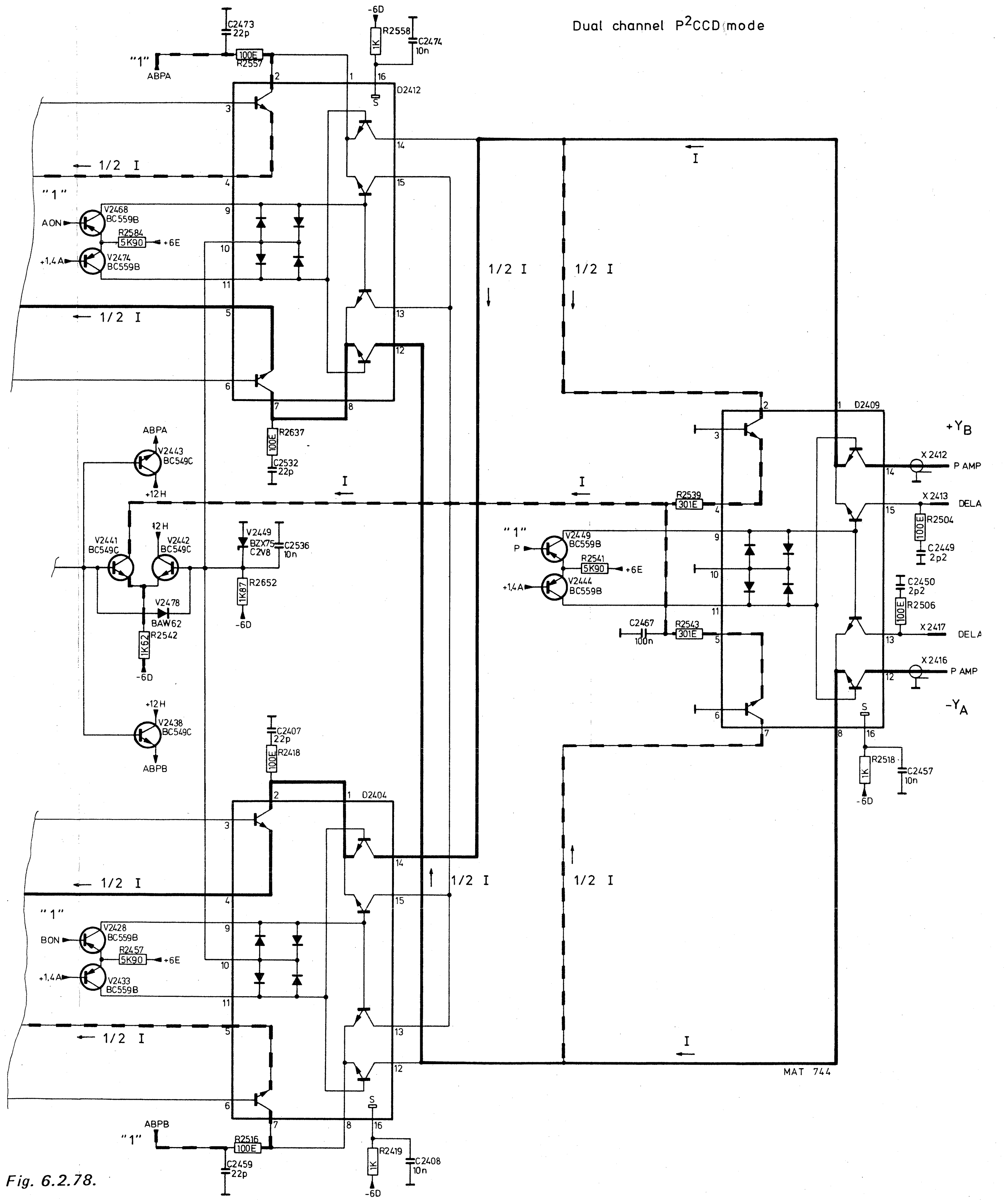


Fig. 6.2.78.

Integrated circuit D2409 serves to switch the signal either to the P2CCD amplifier or to the delay line.
If the signal P is high, the transistor V2449 blocks and V2444 becomes conductive. Consequently, the two outer right transistors of D2409 conduct and the signal is fed to the P AMP OUT 1 and P AMP OUT 2.
If the signal P is low, the two inner right transistors conduct and the signal is fed to the delay line. This occurs in the direct, roll and sampling mode.

6.2.21.5. Delay line compensation/Track and Hold Gate

A symmetrical delay line is mounted between the channel switch (via D2409) and a series feedback push-pull amplifier in combination with a shunt feedback push-pull amplifier.
The delay line is an symmetrically-mounted spiralled cable with characteristic impedance of 150 Ω and a delay of approximately 60 ns. The output is terminated by two series resistors, each of 75 Ω.

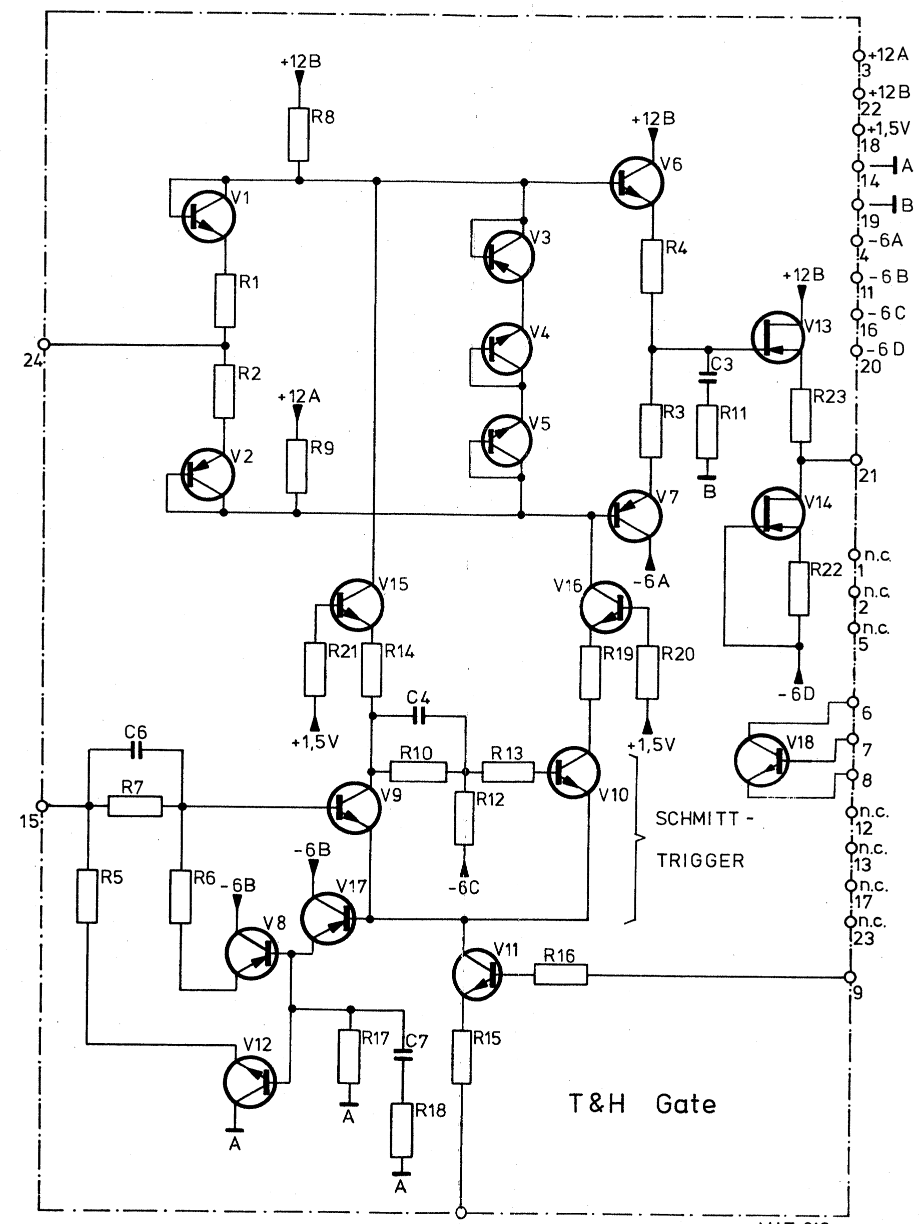
The emitter impedance of the series feedback stage (D3004) consists of RC frequency compensation networks.

For greater accuracy, it is preferable to measure the difference between an instantaneous analog signal sample and the previous signal sample rather than measuring each signal value separately.
This is done by recovering the previous sample that has been digitised, using a digital-to-analog converter and subtracting this value from the existing value to obtain the analog difference δV.

Transistors V3004 and V3003 are used to subtract the previous sample from the existing one. The sample to be subtracted, re-converted from the digital section, is called the DAC M-1. This voltage is converted into current and is applied to the emitter of the series feedback stage, D3004. As this signal is in antiphase it will be subtracted.

Because of the asymmetrical input to the Track and Hold (T & H) gate, the common-mode signal in addition to the supply voltage variation must be suppressed. For these reasons, the transistors V3001 and V3002 are introduced. The emitters are driven by a constant-current supply derived from the current source built up by an operational amplifier D3006 (pins 1, 2 and 3), which measures the voltage across resistor R3058 and drives V3008 to maintain constant current. The constant current drives transistors V3001, V3002 in such a way that the bias current is always constant.

The Track and Hold gate will now take a sample controlled by the signal TAND H. This signal is generated on the Trigger Unit A22. If the signal is low, the input signal is tracked. If the signal is high, the instantaneous value of the input signal is held momentarily. This gate is incapable of holding the sample long enough, without voltage droop, to convert it into a digital value. For this reason, a Sample and Hold gate is added on the Conversion Unit A8. The output signal of the Track and Hold gate is applied via a buffer amplifier to D3003, an operational amplifier (x5 gain approx.), which compensates the offset voltage. The output of the offset compensation circuit is applied via a multiplexer on the CCD logic unit A10 to the Sample and Hold gate on the Conversion Unit A8.



MAT 910

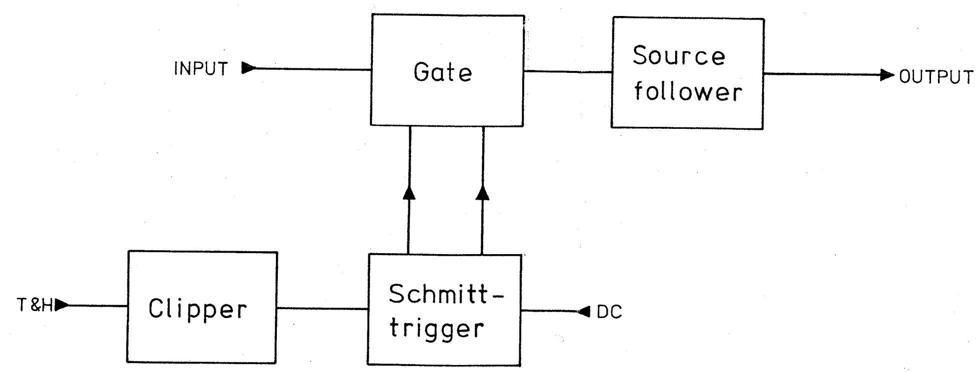
6.2.21.6. Logic circuits (control interfaces)

In order to activate the correct combination of reed relays, the microprocessor scans the following switches of both channel A and channel B:

AC/DC; 0 and AMPL/DIV switches.

To read the positions of the switches, an eight-input/four-output multiplexer (D2418) is addressed, each main loop by $\overline{IO\emptyset}$ together with read pulse $\overline{RD}$.
Address line AØ ensures that D2418 is addressed by address 8Ø1E for channel A switching and 8Ø1F for channel B switching.
The output of multiplexer D2418 and D2419 is connected to the data-bus lines DØ ... D7 and read by the microprocessor system.

The switch settings are converted by the microprocessor system and are applied, via the data-bus, to the latches D2424. These outputs ports are enabled by the combination of the write pulse $\overline{WR}$; the input/output pulse IOØ, and for each port an address line (A1 and A2) Address D2424 is 8ØØ3. Address D2426 is 8ØØ5; address D2427 is 8ØØ6.
The outputs of these ports are fed to the reed relays; the following table indicates the reed relays that are active in relationship to the position of the switches:



MAT 911

RANGE (x10 probe)	RANGE (x1 probe)	K2412	K2413	K2414	K2416	K2418	K2409	K2411
.1 V	10 mV	I/O	1	1	0	0	0	0
.2 V	20 mV	I/O	1	1	0	0	0	0
.5 V	50 mV	I/O	1	1	0	0	0	0
1 V	.1 V	I/O	1	1	0	0	0	0
2 V	.2 V	I/O	1	1	0	0	0	0
5 V	.5 V	I/O	1	1	0	0	0	0
10 V	1 V	I/O	0	0	1	1	0	0
20 V	2 V	I/O	0	0	1	1	0	0
50 V	5 V	I/O	0	0	1	1	0	0
.1 kV	10 V	I/O	0	0	0	0	1	1
.2 kV	20 V	I/O	0	0	0	0	1	1
.5 kV	50 V	I/O	0	0	0	0	1	1
0	0	I/O	0	0	0	0	0	1

The complete output of D2424 (and D2426) with the corresponding attenuator, AC/DC and 0 switch positions is given in the table below (D2426 is for channel B and is analog):

RANGE (x10 probe)	RANGE (x1 probe)	A-DC	x1A	x^1/10A	x^1/100A	x^1/100A*	x^1/1A	x^1/2A	x^1/5A	x10A
.1 V	10 mV	–	1	0	0	0	1	0	0	1
.2 V	20 mV	–	1	0	0	0	0	1	0	1
.5 V	50 mV	–	1	0	0	0	0	0	1	1
1 V	.1 V	–	1	0	0	0	1	0	0	0
2 V	.2 V	–	1	0	0	0	0	1	0	0
5 V	.5 V	–	1	0	0	0	0	0	1	0
10 V	1 V	–	0	1	0	0	1	0	0	0
20 V	2 V	–	0	1	0	0	0	1	0	0
50 V	5 V	–	0	1	0	0	0	0	1	0
.1 kV	10 V	–	0	0	1	1	1	0	0	0
.2 kV	20 V	–	0	0	1	1	0	1	0	0
.5 kV	50 V	–	0	0	1	1	0	0	1	0
0	0	–	0	0	0	1	0	0	0	0
AC	AC	0	–	–	–	–	–	–	–	–
DC	DC	1	–	–	–	–	–	–	–	–

Range indication

When using a probe with range indication, the microprocessor system calculates the attenuation of the probe, which is then displayed on the scale rings of the AMPL/DIV switches and also in the alphanumeric display. The microprocessor system obtains the information of the probe, via D2417, by the signals $\overline{\mathrm{PA}\emptyset}$, $\overline{\mathrm{PA1}}$, $\overline{\mathrm{PB}\emptyset}$, $\overline{\mathrm{PB1}}$ for channels A and B respectively.
These signals are decoded in the microprocessor system and then applied to the displays.

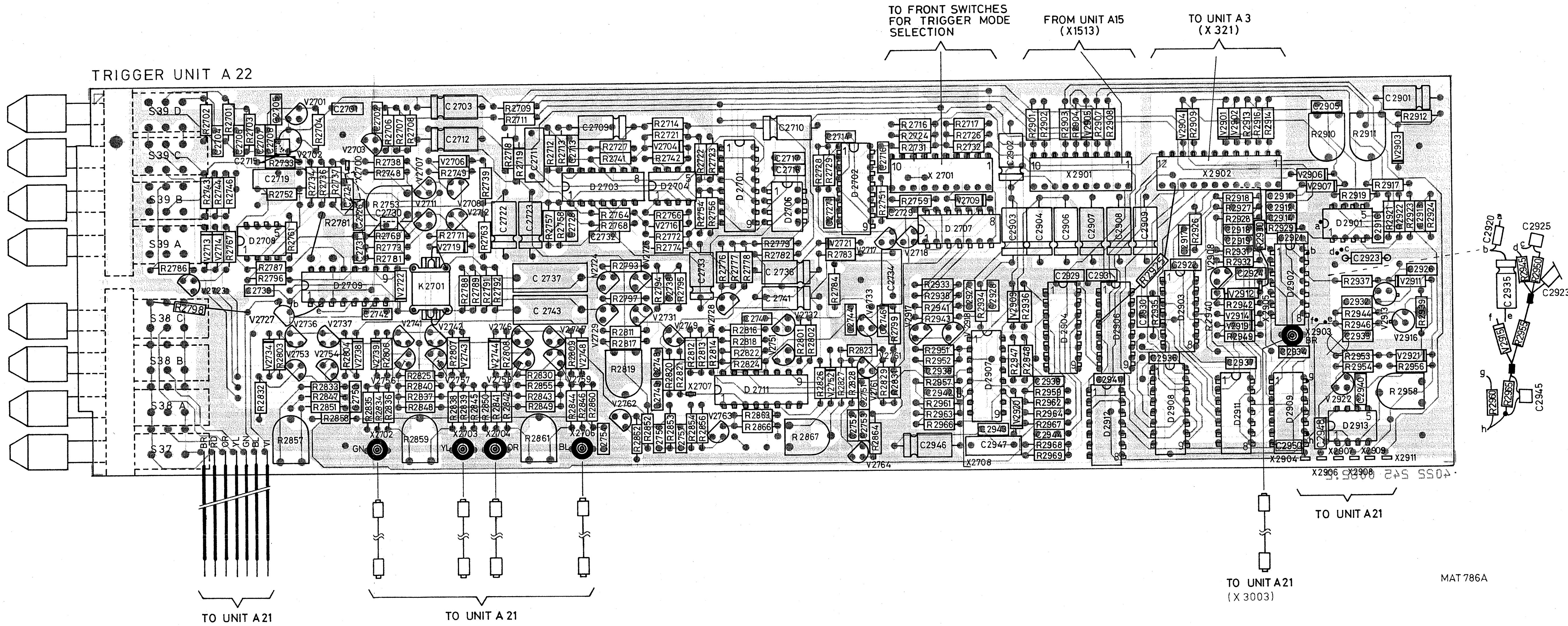
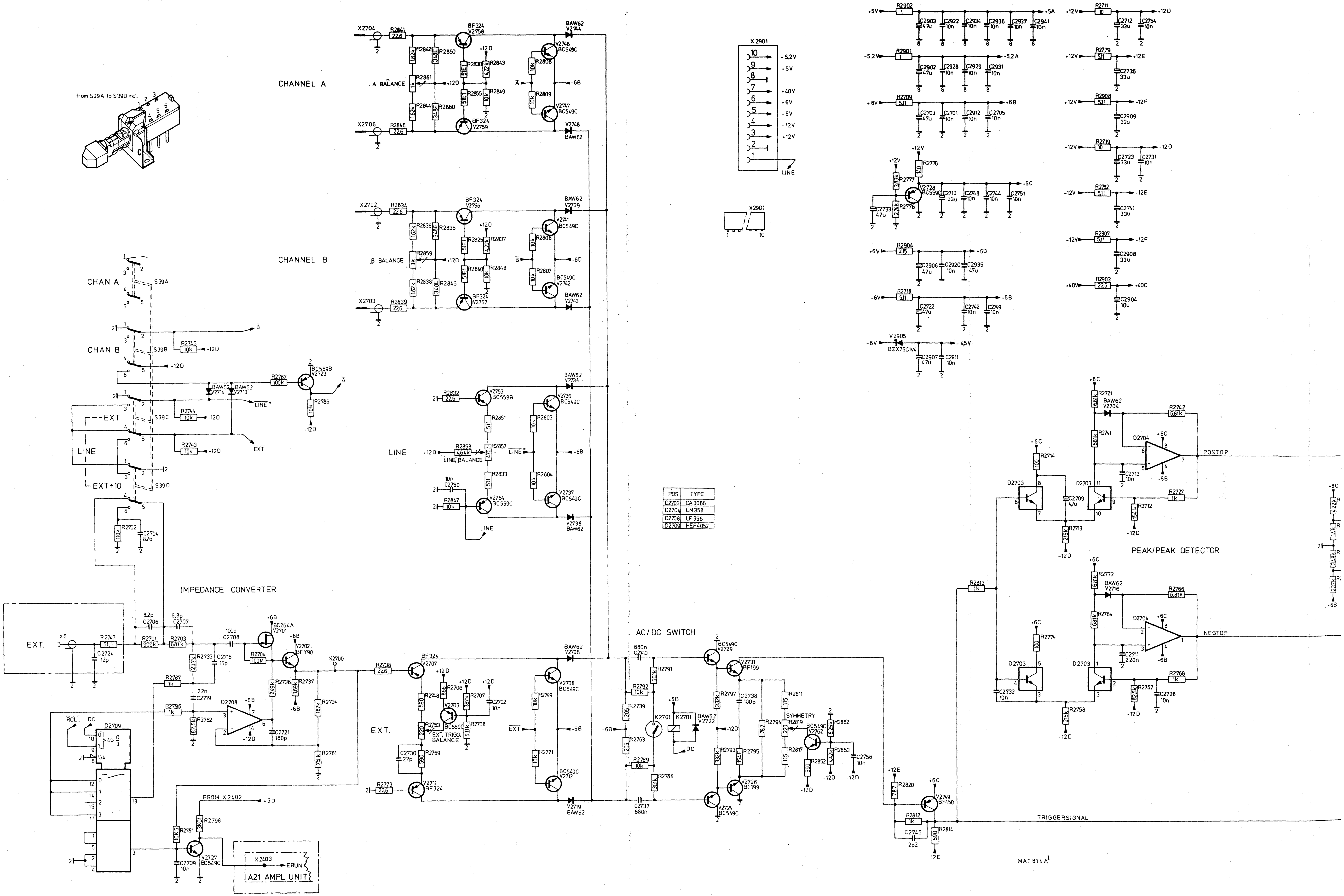
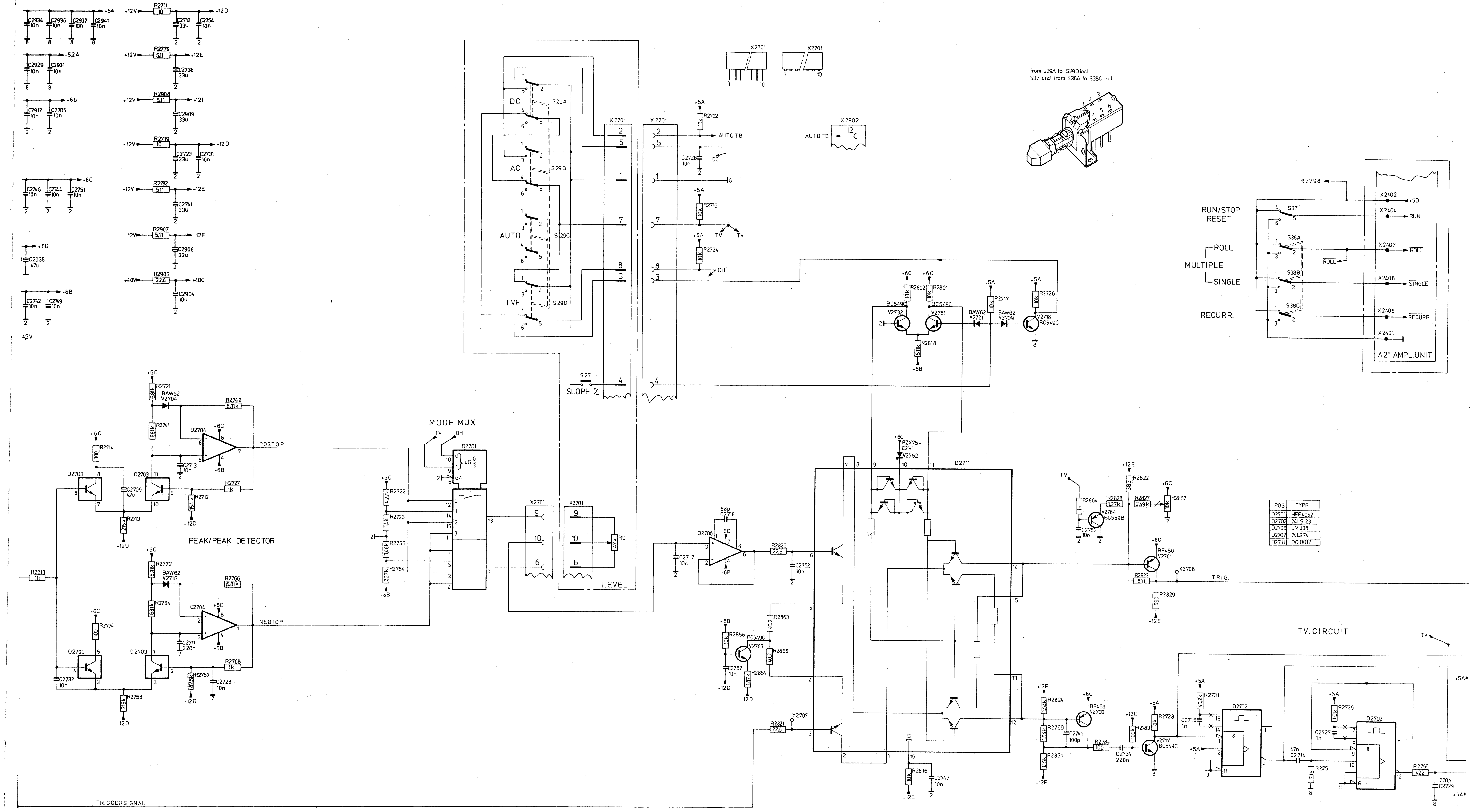

TO FRONT SWITCHES FOR TRIGGER MODE SELECTION
FROM UNIT A15 (X1513)
TO UNIT A 3 (X 321)
TRIGGER UNIT A 22
TO UNIT A21
TO UNIT A 21
TO UNIT A21 (X 3003)
TO UNIT A21
MAT 786A

Fig. 6.2.84.



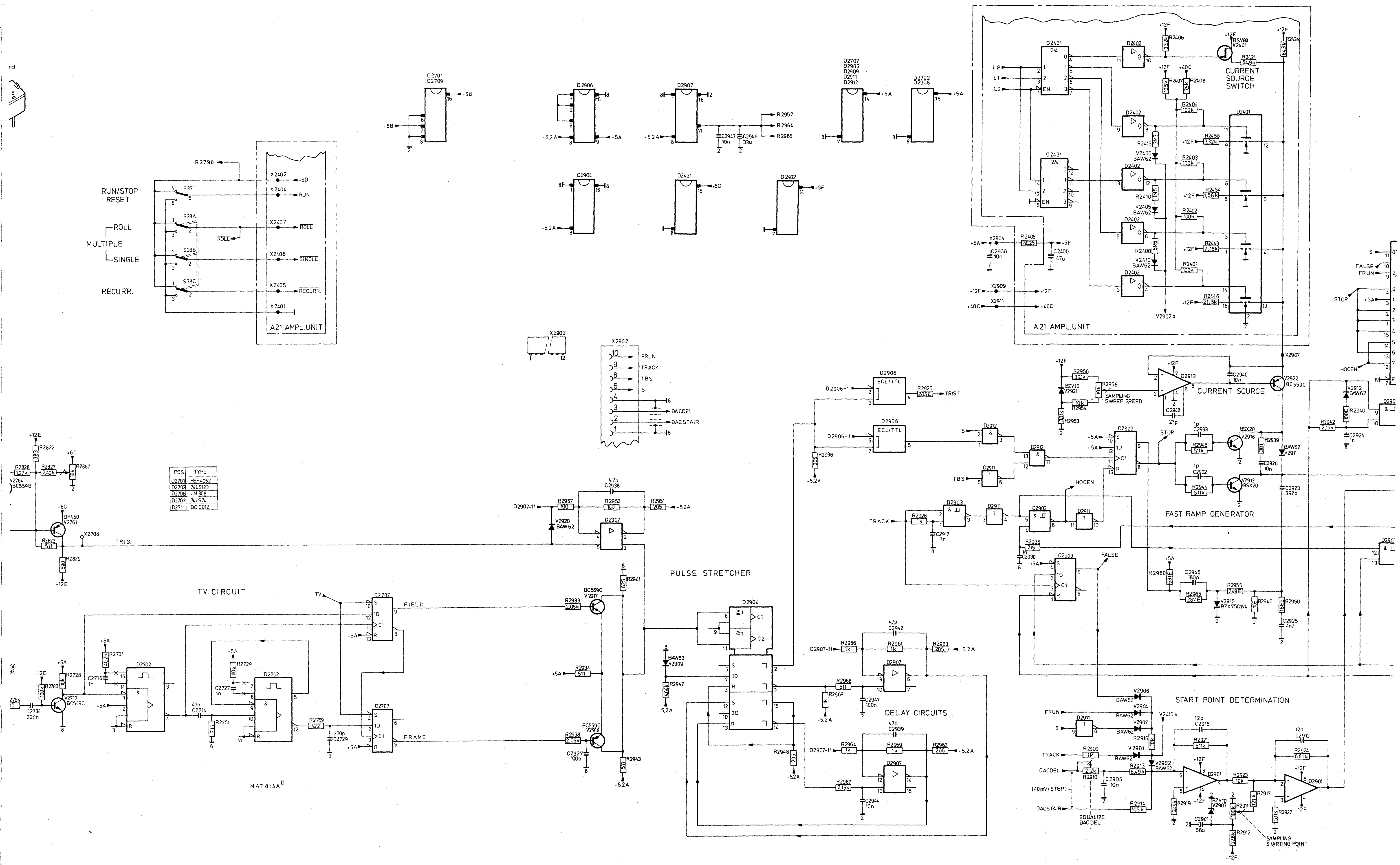
POS	TYPE
D2703	CA 3086
D2704	LM 358
D2708	LF 356
D2709	HEF 4052



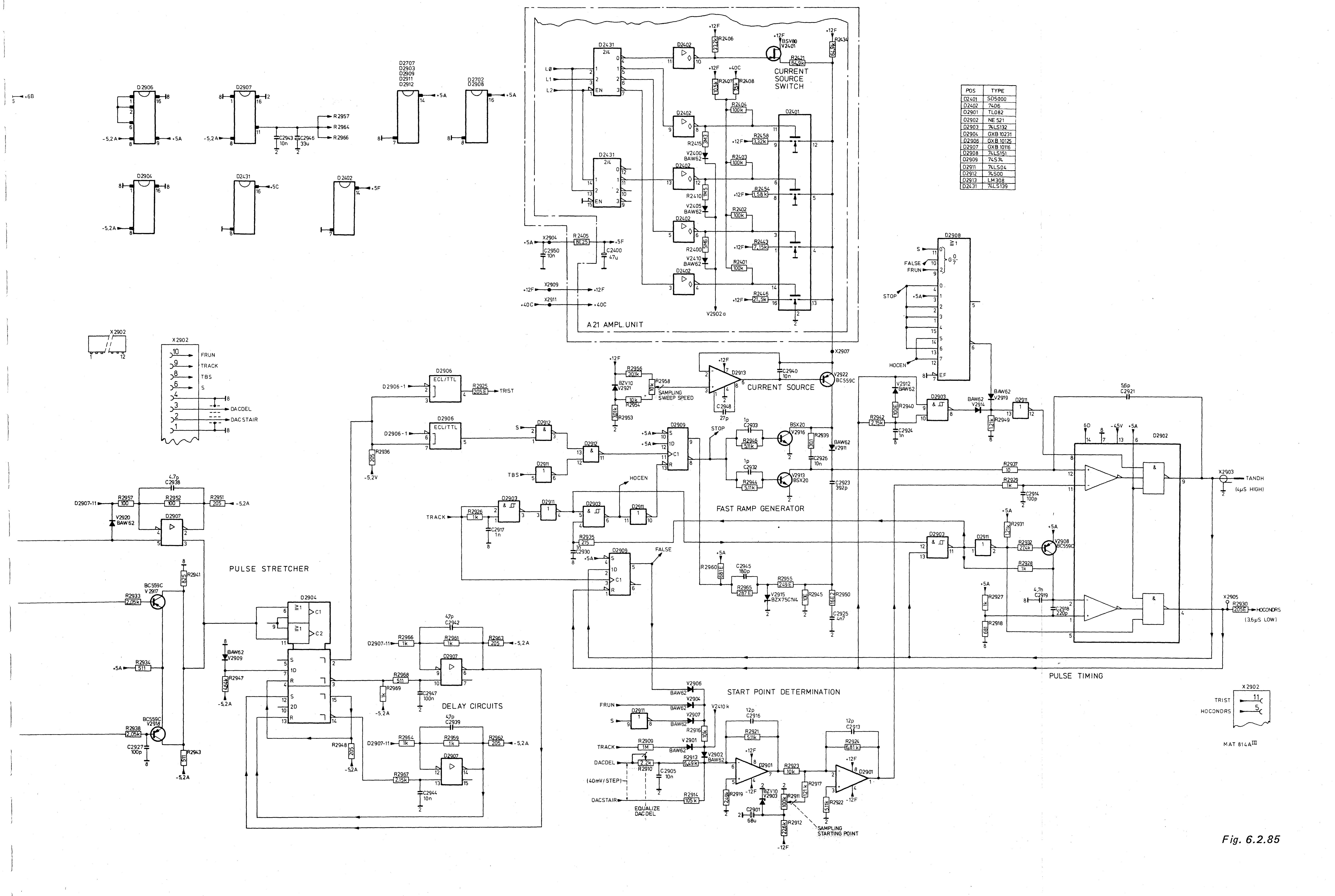
POS	TYPE
D2701	HEF4052
D2702	74LS123
D2706	LM 308
D2707	74LS74
D2711	OQ 0012

MAT 814A I

MAT 814A II

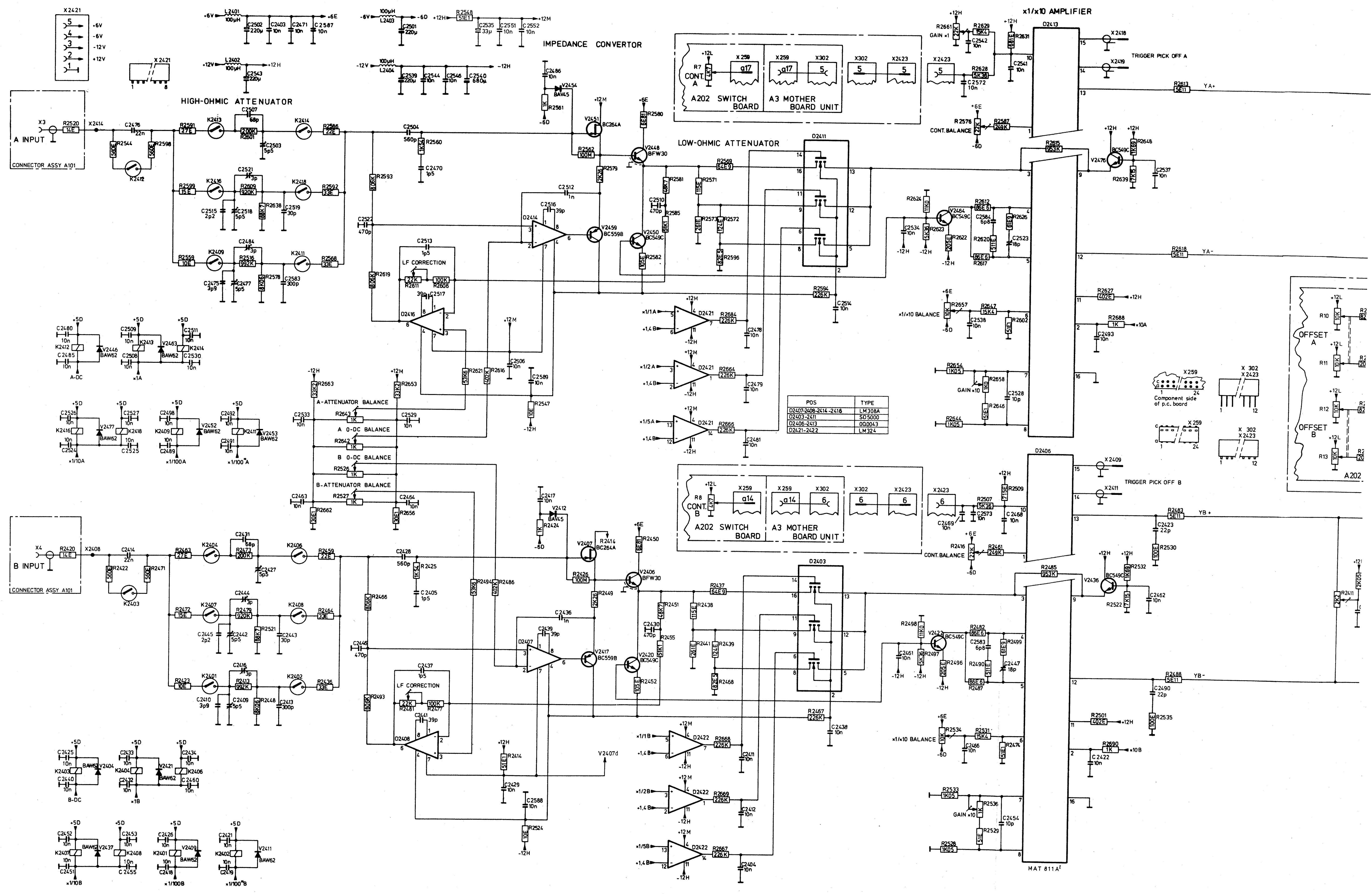


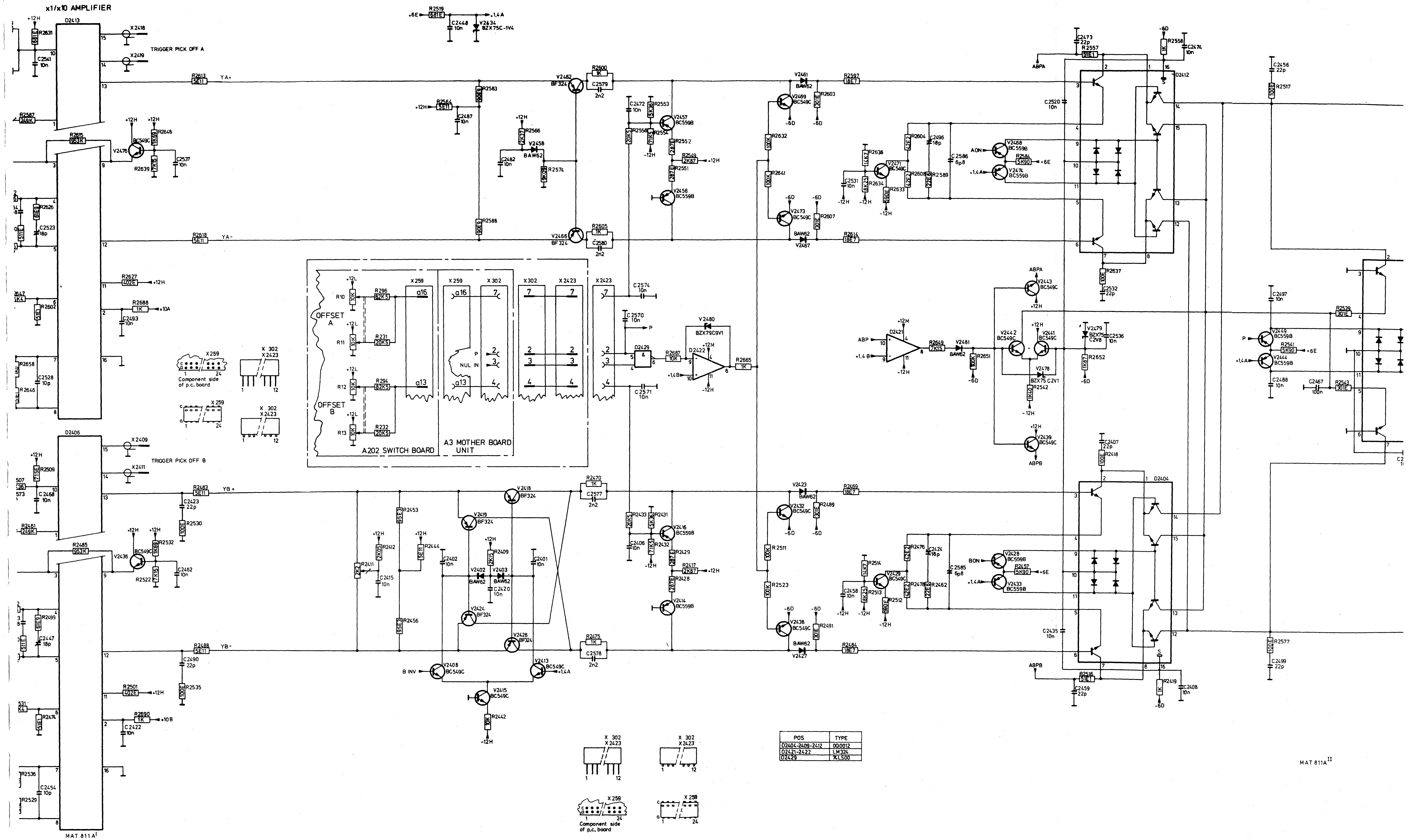
POS	TYPE
D2701	HEF4052
D2702	74LS123
D2706	LM308
D2707	74LS74
D2711	OQ 0012



POS	TYPE
D2401	SD5000
D2402	7406
D2901	TL082
D2902	NE 521
D2903	74LS132
D2904	GXB 10231
D2906	GXB 10125
D2907	GXB 10116
D2908	74LS151
D2909	74S74
D2911	74LS04
D2912	74S00
D2913	LM308
D2431	74LS139

Fig. 6.2.85


x1/x10 AMPLIFIER
IMPEDANCE CONVERTOR
HIGH-OHMIC ATTENUATOR
LOW-OHMIC ATTENUATOR
A INPUT
B INPUT
CONNECTOR ASSY A101
A202 SWITCH BOARD
A3 MOTHER BOARD UNIT
LF CORRECTION
A-ATTENUATOR BALANCE
A 0-DC BALANCE
B 0-DC BALANCE
B-ATTENUATOR BALANCE
TRIGGER PICK OFF A
TRIGGER PICK OFF B
CONT. BALANCE
x1/x10 BALANCE
GAIN x1
GAIN x10
OFFSET A
OFFSET B
YA+
YA-
YB+
YB-
POS | TYPE
D2407-2408-2414-2416 | LM308A
D2403-2411 | SD5000
D2406-2413 | OQ0043
D2421-2422 | LM324
Component side of p.c. board
MAT 811 A



POS	TYPE
D2404-2409-2412	OQ0012
D2421-2422	LM324
D2429	74LS00

6.2.6. RAM unit A6

The RAM unit basically comprises the four random-access memories, ACCU, STO1, STO2, STO3 used for signal storage, the two digital-to-analog converters X DAC and Y DAC and their associated control circuits.

6.2.6.1. RAM memories ACCU, STO1, STO2, STO3

Each of the RAM memories consists of two RAM IC-chips of ¼K-nibbles each (256x4 bits) enabling a maximum of 256 bytes to be stored.

The overall memory is selected by PON.DAT = 1, i.e. with the power on and the data field addressed. Memory allocation is as follows:

MEMORY	IC ELEMENTS
ACCU	D601, D602
STO1	D603, D604
STO2	D606, D607
STO3	D608, D609

Selection of one or more of the memories is made under microprocessor control.
A byte of data representing the information for reading or writing one or more of the memories is sent by the microprocessor on data-lines DØ ... D7 to the latch D613. If the signal combination WR.IO4 is logic 1, the data byte will be latched by D613.
Two groups of output signals are produced by latch D613:

Output Enable RAM signals (OER) – signals $\overline{\text{OERØ}}$ ... $\overline{\text{OER3}}$ select the memory of which the contents are required to be read.

Write Enable RAM signals (WRER) – signals $\overline{\text{WRERØ}}$ ... $\overline{\text{WRER3}}$ select the memory in which data is required to be written. With no WR signal available these signals are blocked.

Individual RAM locations are selected by address lines AØ ... A7.

Data inputs for the memories

Data received from other units can only be stored in the ACCU RAM.
Data stored in any of the other three memories STO1, STO2, STO3, is always derived from the ACCU memory.

Data for storage in the ACCU memory (D601, D602) can be:
– output data ACQBØ ... ACQB7 from the acquisition circuit,
– data from the microprocessor,
– data from the IEC-bus interface board via the system data-bus lines DØ ... D7.

The signals ACQBØ ... ACQB7 are applied to the latch D614 and the signals DØ ... D7 are applied to the latch D616.
Selection of either one of these latches is made under microprocessor control via the logic level of signal $\overline{\text{SOD}}$ (serial output data).

$\overline{\text{SOD}}$ = 1 selects D614
$\overline{\text{SOD}}$ = 0 selects D616 via inverter D626

Inverter D626 prohibits the output of data from both latches to the ACCU bit lines at the same time.

Overflow detection

The information in the RAMs is stored in 2's complement notation, which means that signal amplitudes are stored in positive as well as negative binary numbers.

maximum positive	+127	0111 1111
	⋮	⋮
	+1	0000 0001
	+0	0000 0000
	−1	1111 1111
	⋮	⋮
maximum negative	−128	1000 0000

From the above, we can see that if the most-significant bit of a binary number is at logic 0, we have a positive number, otherwise it represents a negative number.

An incorrect setting of the AMPL/DIV switch or the OFFSET control causes an overflow, which means that the result after digitising is greater than can be stored. Therefore, if the maximum number 0111 1111 or the minimum number 1000 0000 is reached, an overflow situation is recognised. This is signalled by a flashing trace on the c.r.t. display.

These two extreme overflow situations can be decoded as follows:

The most-significant bit D7 is inverted by D626 (1,2) resulting in the overflow codes 0000 0000 or 1111 1111. By comparing the inverted most-significant bit with the other seven bits in exclusive OR circuits D618 and D619, an output signal ZOVL (Z Overload) is indicated when one of these two overload situations occurs. The overflow signal ZOVL is applied to the Z-pulse (ZIN) circuit on Unit 4 to produce the flashing of the display when overload is reached.

6.2.6.2. *Digital-to-analog converters X DAC, Y DAC*

DAC output signals in X = t mode

Horizontal deflection on the c.r.t. display in the X = t mode is controlled by the addresses needed for reading the contents of the memories. Therefore, the address bits AØ ... A7 are applied to the X DAC (horizontal digital-to-analog converter) D622 to generate an analog deflection signal XDAC that varies between +5 V and −5 V.
The address bits are applied to the X DAC (D622) via two multiplexers D611 and D612, which are controlled by the signal $\overline{\text{AVSB}}$.

$\overline{\text{AVSB}}$ = 1 selects X = t mode
$\overline{\text{AVSB}}$ = 0 selects X = A / Y = B mode

Vertical deflection on the c.r.t. display is controlled by the eight data bits DØ' ... D7', which are applied to the Y DAC (D621) to generate an analog deflection signal Y DAC.
These data bits are routed to the Y DAC via eight exclusive OR gates D623, D624, which are controlled by the INV signal to invert the data when the front-panel INV switches are operated.

The X DAC and Y DAC latches can be enabled by the enable signals $\overline{\text{X DACE}}$ and $\overline{\text{Y DACE}}$ respectively. These are the output signals from the multiplexer D628, which is enabled by the $\overline{\text{DAT}}$ signal. Selection of input signals to the multiplexer is made by the signals AØAB and $\overline{\text{AVSB}}$ according to the following table:

$\overline{\text{AVSB}}$	AØAB	$\overline{\text{XDACE}}$	$\overline{\text{YDACE}}$	
0	0	WR		X=A/Y=B mode
0	1		WR	
1	0	WR	WR	X=t mode
1	1	WR	WR	

DAC output signals in X = A/Y = B mode

If channel A as well as channel B information is stored in the RAMs, XY deflection can be obtained by selecting the X = A/Y = B mode by depressing the relevant front-panel switch.
To give XY deflection, the channel information on A and B has to be applied to the X DAC and the Y DAC respectively.
There are two different methods of storing the channel A and channel B information in the RAMs.

Channel A ODD: (FASDI = 0) Channel A information is stored in locations with ODD addresses and channel B in locations with EVEN addresses.

Channel A EVEN: (FASDI = 1) Channel A information is stored in locations with EVEN addresses and channel B in locations with ODD addresses.

To obtain XY deflection, it is necessary to apply data from the ODD addresses to the X DAC and data from the EVEN addresses to the Y DAC or vice versa depending on the logic level of the FASDI signal.

For correct functioning, only one DAC latch may be enabled at a time, this being controlled by the enable signals $\overline{\text{XDACE}}$ and $\overline{\text{YDACE}}$ on the output of multiplexer D628.

The logic level of signal FASDI (phase of display) controls which channel is stored in odd or even addresses by determining which DAC is loaded first. If FASDI is at logic 0, we have the situation where X DAC (latch D622) is loaded first; i.e. channel A will be stored in the odd addresses.
Alternatively, if FASDI is at logic 1, then Y DAC (latch D621) will be loaded first and channel B will be stored in the odd addresses.

FASDI	AØ	AØAB
0	0	1
0	1	0
1	0	0
1	1	1

FASDI = 0 results in AØ being inverted
FASDI = 1 results in AØ not inverted

INCOMING SIGNAL	OUTGOING SIGNAL	GENERATED ON UNIT	USED ON UNIT	DESCRIPTION
AØ ... A7		A4		Address bits from system address bus
	AØAB	A6	A4	Address bit AØ in X=A/Y=B mode
ACQBØ ... ACQB7		A7		Acquisition output bits Ø ... 8
$\overline{\text{AVSB}}$		A13		Logic 0 in X=A/Y=B mode
DØ ... D7	DØ ... D7	A4-A6		Data bits from system data-bus
$\overline{\text{DAT}}$		A4		Data selection
FASDI		A13		Phase on display level
$\overline{\text{INV}}$		A4		Signal invert
$\overline{\text{IO4}}$		A4		Data RAM select
	$\overline{\text{OERØ}}$	A6	A20	Output enable RAMØ
	$\overline{\text{OER1}}$	A6	A20	Output enable RAM1
	$\overline{\text{OER2}}$	A6	A20	Output enable RAM2
	$\overline{\text{OER3}}$	A6		Output enable RAM3
PON		A4		Power on
$\overline{\text{RD}}$		A4		Signal READ from microprocessor
$\overline{\text{SOD}}$		A4		Microprocessor serial output data
$\overline{\text{WR}}$		A4		Signal WRITE from microprocessor
	X DAC	A6	A20	Horizontal DAC output signal
	Y DAC	A6	A20	Vertical DAC output signal
	ZOVL	A6	A4	Z overflow signal
+5 V		A15		
⏚		A15		
+5 BATT		A15		
+12 V		A15		
−12 V		A15		

RAM UNIT A6

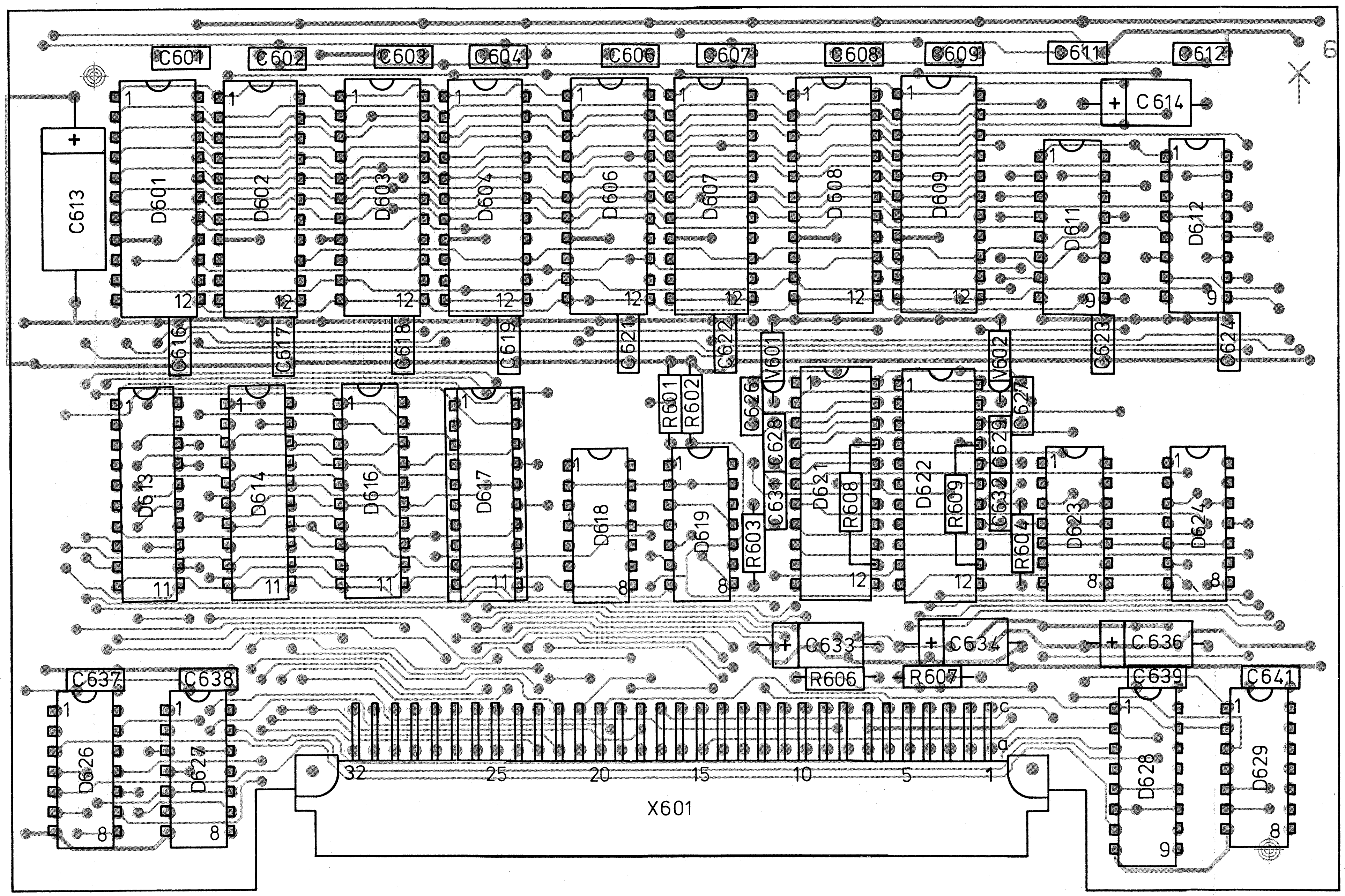


Fig. 6.2.18.

MAT 773A

BUFFER UNIT A7

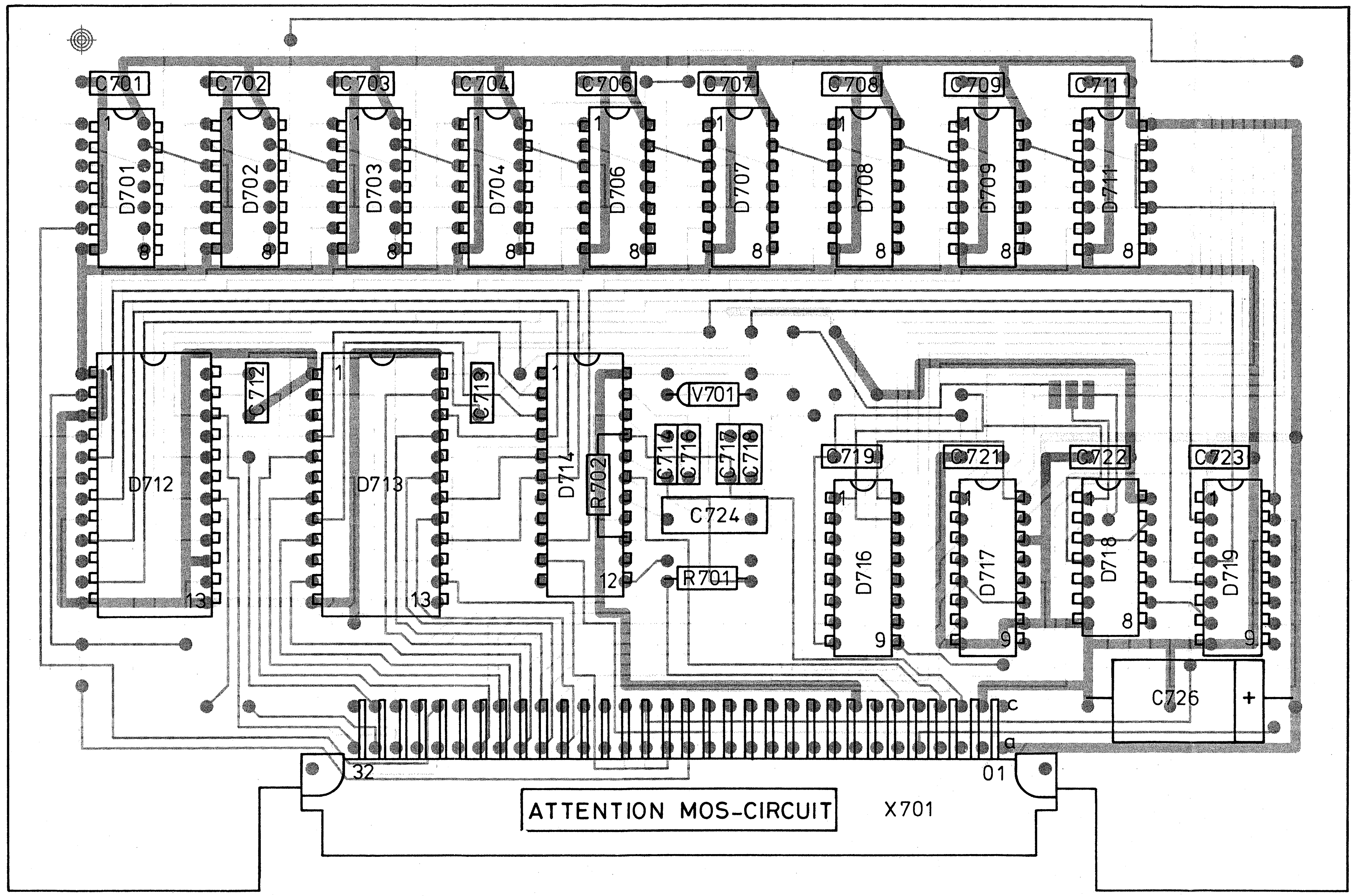


Fig. 6.2.22.

MAT774

After this procedure, the adder output value M_n will be shifted into a shift register as a new and corrected value. This system of digital adding is also used, in a different way, in the P^2CCD-mode as described in the Conversion Unit A8.

Detailed description

This digital adding technique is now described in greater detail with reference to the various circuit elements. The analog value of the preceding signal sample M_{n-1} is subtracted from the new sample M_n in the vertical amplifier stage. This results in a differential analog voltage $M_n - M_{n-1}$, which is converted to digital signals ADCBØ ... ADCB8 and applied to the adder circuit on unit A8 together with the preceding sample M_{n-1} in digital form.

After adding overflow detection and marking, the sum signal M_n is applied as ADCBØ ... ADCB8 to the shift register on the buffer unit A7. With this new signal value stored in the shift register, the circuit continues with the next.

The corrected sample value M_n on the ADCB lines from the conversion unit A8 to the shift register is also applied to the 4-bit latches D712 and stored under the control of signal CØ. The output signals from the latches are applied to the digital-to-analog converter DAC (M-1) D714.

In the P-mode, the DAC (M-1) circuit is switched off by the P signal on the $\overline{LE}$ input pin 10.
However, in the DRS-mode the DAC (M-1) circuit is switched on.
The most-significant bit of the 8-bit 2's complement information offered to the DAC (M-1) is inverted by D719 (4,5) to translate the data into 8-bit straight binary notation.
Conversion by DAC (M-1) results in the analog value of the preceding digital sample M_{n-1} and this value is fed back to the vertical amplifier stage for subtraction from the new signal sample M_n.

In the amplifier stage, analog subtraction will result in a new differential voltage as previously described. This differential voltage $M_n - M_{n-1}$ is then converted to digital in the ADC and added to the old digital value M_{n-1}. The old digital value that was stored in the two 4-bit latches D712 is in the meantime shifted to the next two 4-bit latches D713 by control signal C4 and fed to the adder circuit. Here, the 8-bit 2's complement notation is converted into a 9-bit ACQBØ ... ACQB8 digital form by copying the last bit.
Data from one signal source only may be fed to the ACQB bus by more than one buffer simultaneously. This is made possible by signals P and NDR via NOR-gate D718 (4,5,6) and inverter D719 (2,3).
Each time an NDR pulse is generated, the total shift register contents will be copied into the ACCU memory. Precise timing diagrams are given in the ACL Unit A9 description.

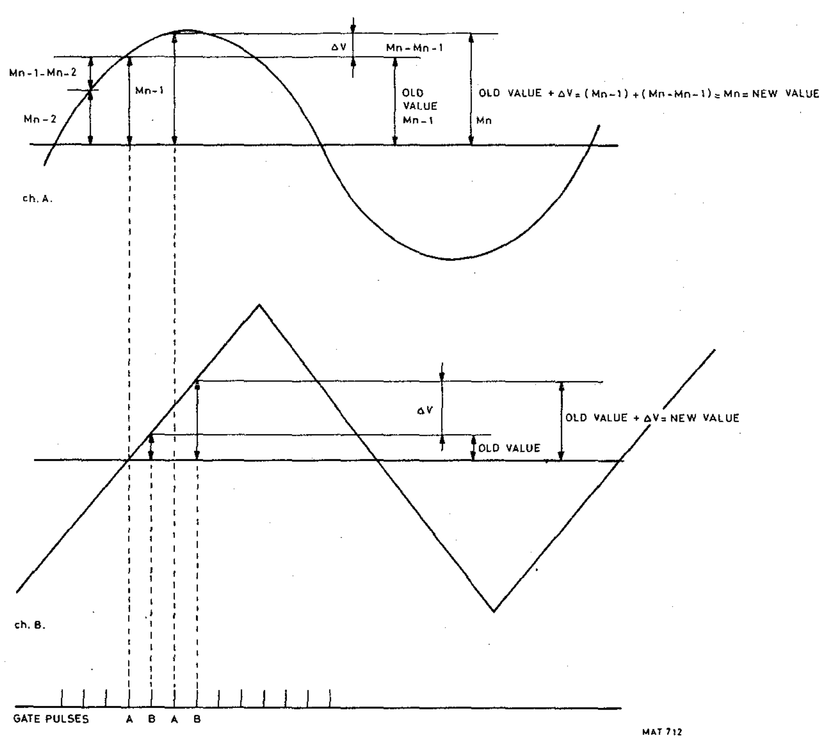


Fig. 6.2.21.

INCOMING SIGNALS	OUTGOING SIGNALS	GENERATED ON UNIT	USED ON UNIT	DESCRIPTION
	ACQBØ ... 8	A7	A6–8	Acquisition output bits Ø ... 8
ADCBØ ... 8		A8		ADC bits
CØ		A9		Control Ø signal from ACL unit
C4		A9		Control 4 signal from ACL unit
	CLKSH	A7		Clock pulse for shift register
	DAC M-1	A7	A21	DAC M-1 output signal
INS		A9		Shift command for shift register
NDR		A9	A4	New data ready
P		A12	A7–8–9–10	P-mode signal
$\overline{\text{SOD}}$		A4		*Microprocessor serial output data*
	SOD	A7	A8	Microprocessor serial output data
$\overline{\text{WR}}$		A4		Signal write from microprocessor
+5 V		A15		
+12 V		A15		
–12 V		A15		
⏚		A15		

The 2's complement equivalent value is fed to the ADCB bus-lines by the tri-state non-inverting buffers D811, D812 under the control of signal C1. With C1 at logic 1, the buffers are in 3-state mode.

Signal input C1 is a control line which, together with signal C2 prevents simultaneous input of data to the bus-lines by more than one buffer.

6.2.8.3. *Correction circuits*

As the correction circuits operate in conjunction with other circuits that are not part of the conversion unit A8, the data routeing and the principles of correction in the P²CCD-mode are first discussed.

Data routeing and correction in the P²CCD-mode

Due to internal P²CCD faults and differences between the frequencies f_{in} and f_{out}, an incorrect zero level of the P²CCD output signal is possible as shown in the following graph.

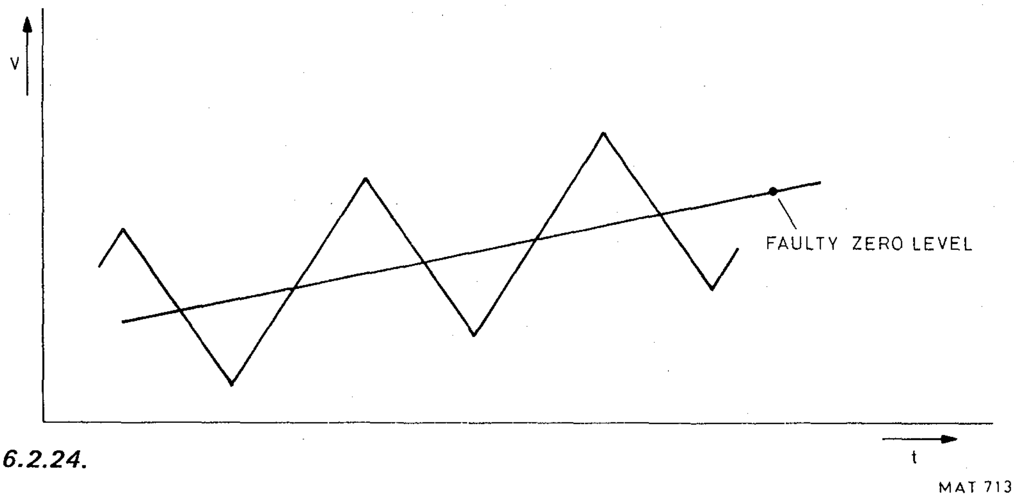


Fig. 6.2.24.

P² CCD output signal with shifting zero level

Under these conditions, the total faulty contents of the P²CCD are converted from analog form to digital in 256 steps and after each conversion the data is put on the ADCBØ ... ADCB8 bus and directly shifted into the 9-bit shift register on buffer unit A7. After 256 steps, the total P²CCD contents are stored here, and the register is then blocked.

In order to correct the zero level, the P²CCD input is switched to zero and 256 samples of this zero signal are shifted into the P²CCD at the same frequency f_{in} as for the normal input signal.

By reading the P²CCD contents again, with the same frequency f_{out} (78 kHz) as for the faulty input signal, an incorrect zero level having the same errors as described above will appear on the P²CCD output as shown below.

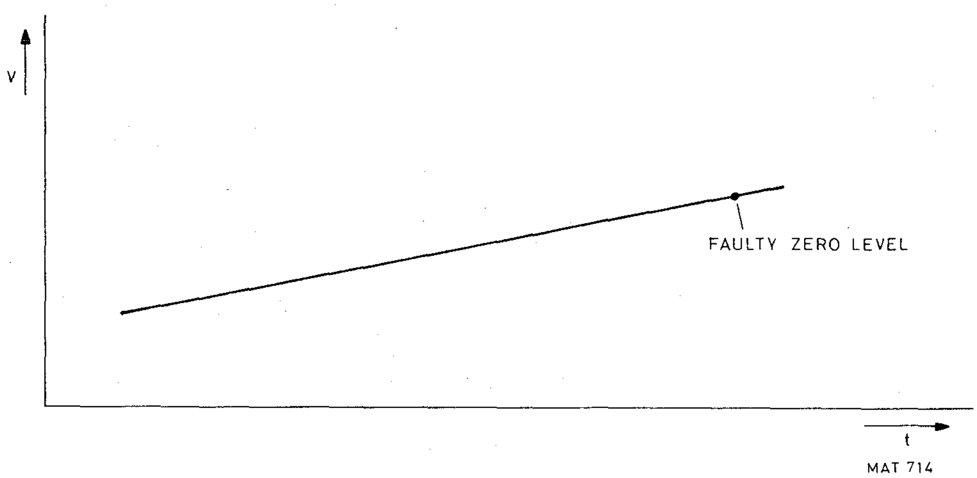


Fig. 6.2.25.

This incorrect zero level is then digitally subtracted (in 256 steps) from the faulty input signal, which was already stored in the shift register.
The corrected result is then re-stored in the shift register.

Correction circuit description

Considering the correction circuits in more detail, the correction cycle is started when the P2CCD is completely filled with zero samples. This is done in 256 steps, in which for every step, one sample of faulty input information from the shift register, and one converted zero sample from the P2CCD are applied to an adder circuit on this conversion unit (A8), consisting of the integrated circuits D803, D816 and D804.

The procedure is as follows:

- The shift register contents are placed byte after byte on the ACQBØ ... 8 bus via a buffer and directly applied to the inputs of the adder circuits.
- The samples of zero information from the P2CCD are placed on the ADCBØ ... 8 bus, sample after sample in the same way as described for the uncorrected signal information. However, in this case it is not shifted into the shift register but is transferred via AND-gates D801, D813 and exclusive-OR gates D802, D814 and D809 (4,5,6) to the adder circuit. For correct overflow detection and marking, bit 9 is copied and applied to the adder as bit 10.

  (During the copying of the shift register contents into the ACCU memory in ROLL-mode, one side of the adder input is blocked via AND-gates D801, D813 by the $\overline{\text{NDR}}$ signal to permit recirculation of the shift-register contents.)

  The exclusive-OR circuits serve to invert the zero information so that it can be subtracted from the signal information. The subtraction process is performed by inverting the zero information and adding it, together with a forced carry, to the signal information from the shift register.
  The forced carry is obtained by signal P on input 9 of adder circuit D803.

At the output of the adder, the corrected signal samples appear one by one and are transferred to the overflow detecting and marking circuits (multiplexers D806, D807, D817, D818).
The ACCU memory, and thus the c.r.t. display, is 8-bit wide; therefore the corrected adder output signals, which can be 10-bit wide, are checked for overflow. Consequently, if overflow occurs, this condition will be indicated and overflow marking is necessary.

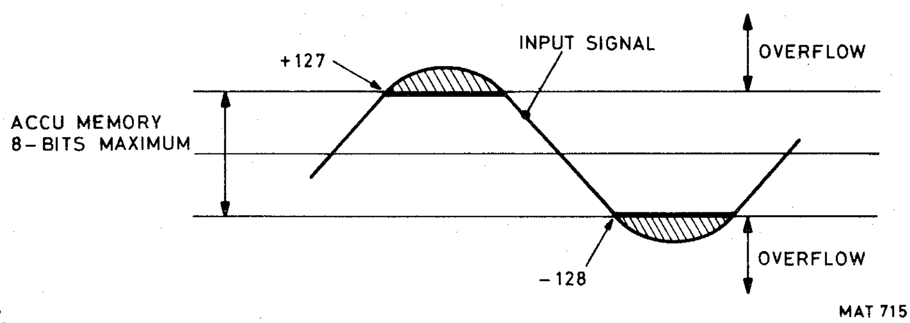


Fig. 6.2.26.

Marking is carried out by changing the signal value during overflow in one of the digital values +127 or −128, via the multiplexers D806, D807, D817, D818.

These multiplexers are controlled by the adder output bits ADOB7, ADOB8, ADOB9, which give information about overflow.

The first counting pulse results in counter-state 0. Output signals OA, OB, OC and OD are applied to a BCD/1 : 10 decoder, D923.
Control pulses C3 and C4 are derived directly from decoder outputs 3 and 4 respectively. The C3 pulses are only present whenever there is no new data ready, i.e. if $\overline{NDR}$ = logic 1.
After state 7 of the counter, a logic 0 on output pin 9 of the decoder is fed back to the direct reset input of flip-flop D927 to switch it to its zero state. Thus the count pulses for the counter are blocked and it is again preset by the value 15. From the same decoder output signal a COUNT pulse is given via flip-flop D913, which is switched as a normal inverter. One COUNT signal is generated for each ADC conversion and so provides a means of counting the number of conversions.

Control pulses C1, C2 (C1 inverted) and INSP are generated by multiplexer D921 controlled by the NDR and PN signals.

CONTROL SIGNALS		OUTPUT SIGNALS	
NDR	PN	C1	INSP
0	0	OC	INSR
0	1	0 V	$\overline{C3}$
1	0	+5 V	+5 V
1	1	+5 V	+5 V

Signals C1 and INSP are permanently at logic 1 during NDR. Therefore, during copying the contents of the shift register into the ACCU memory, the buffer following the ADC circuit will be set in its tri-state, i.e. no ADC output data can be sent either to the adder or to the shift register circuit.

Signal C1 will be at logic 1 when uncorrected signal information has to be shifted into the shift register in the P-mode (PN at logic 1). This allows the information to be shifted directly into the register. The shift command INSP is in this situation derived from signal $\overline{C3}$. In the DRS modes and during zero correction in the P-mode, C1 and also C2 signals are derived from counter output OC. These signals control the ADC output buffer and the adder output result register (D819 on unit A8) so that only one of the two can output data on to the ADCBØ ... 8 bus at any given time.
In the DRS modes, and during zero correction in the P-mode, the INSP signal is derived from decoder output signal INSR. Therefore, INSP is generated after the correction result is put in the result register and the register output data is fed to the ADCBØ ... 8 bus.

6.2.9.2. *Timing in P-mode*

Flip-flop D913 is set to logic 1 by a trigger pulse DELTRG in normal trigger mode and by $\overline{AUTRI}$ in the AUTO mode, both signals being generated by the delayed trigger unit (A13).
After receiving a trigger signal, the NULIN signal goes to logic 1. This signal is applied to the vertical amplifier unit A21 to block the amplifier channels so that a zero level is offered to the P^2CCD inputs.
A signal $\overline{FOE}$ (frequency output enable) also goes to logic 0 (assuming that pin 10 of D914 is at logic 1) to indicate to the CCD logic unit that the P^2CCD contents can be read with a clock signal of 78 kHz approx. This will result in HOCON P pulses to start ADC conversions.

The COUNT signals generated at each conversion are counted by the 10-bit acquisition control logic counter consisting of two flip-flops D924 and two 4-bit counters D918 and D917.
This counter, which was in its reset state in the preceding P-mode cycle, is now enabled for counting. Signal NUL IN switches, via multiplexer D916, the flip-flop D902 so that the counter is no longer held in its reset state and is ready to receive count pulses. Signal $\overline{FOE}$ sets the multiplexer D926 so that the COUNT pulses on input 12 appear at output 9. These COUNT pulses are applied to the counter and after 256 have been counted the entire P^2CCD contents are read, digitised and shifted into the shift register. Counter state 256 is indicated by a logic 1 on pin 12 of D917. This signal switches $\overline{FOE}$ to logic 1 via inverter D919 and NAND-gate D914 to stop the P^2CCD read cycle.

A cycle now starts in which the P2CCD is completely filled with zero information, using the same frequency for shifting as that for reading in the input signal information.
Signal $\overline{FOE}$ now switches multiplexer D926 to the state where the 50 kHz signal on pin 13 is coupled to the input of the counter. Counting continues up to 512 and in the meantime, zero information is shifted for about 5 msec into the P2CCD via the NUL IN signal in the vertical amplifier unit (256 x 0,02 msec is approximately 5 msec).
When the counter reaches 512, output 12 of D917 returns to logic 0 and also signal $\overline{FOE}$ = logic 0.
Now a cycle starts in which the zero contents of the P2CCD are read and digitised in 256 steps at a clock frequency of approximately 78 kHz. At every step, one sample of uncorrected information in the shift register is corrected by a zero sample from the P2CCD and the result shifted again into the register. After 256 corrections the total corrected signal is present in the shift register.
At the end of the correction cycle, the state 768 (512+256) of the counter is detected by NAND-gate D914 (11,12,13), which results in a logic 0 on output pin 11.

This signal is fed to output pin 9 of multiplexer D916 and causes flip-flop D902 to switch to its zero state. The output signal on pin 9 of D902 prepares the reset of two synchronous counters with synchronous clear, D918, D917. These can now be reset by a pulse on the clock input, which is derived from a 1,25 MHz clock signal via D926 and D924. The clock signal can pass through multiplexer D926 because of the low level of the output signal on pin 9 of D916, which is applied to input 2 of D926.

After the reset of counters D918 and D917, the output pin 3 of NAND-gate D914 goes to logic 0 via the multiplexer and NAND-gate D914 (11,12,13). This signal resets the two flip-flops D924 of the acquisition control logic counter. The entire counter is now in the reset state and remains in this state until the next NUL IN signal is generated.

At the end of the correction cycle, the positive-going edge of the signal on output 8 of flip-flop D902 will, via multiplexer D901, switch NDR flip-flop D902 to its logic 1 state. Signal NDR is applied to the SID input of the microprocessor on unit A4 to indicate that new data is ready and can be copied by the ACCU memory.

After a certain time, the microprocessor reacts by generating a logic 1 on its SOD output and 256 $\overline{WR}$ pulses followed by a logic 0 on its SOD input. During the SOD signal the shift register contents are copied into the ACCU memory in 256 steps controlled by the $\overline{WR}$ pulses from the microprocessor.

Trigger flip-flop D913 is then brought to its reset state by signal $\overline{CTF}$, which is derived from signal $\overline{NDR}$ via multiplexer D901.
The whole system can react again on incoming trigger pulses at the end of the 'handshake' cycle.

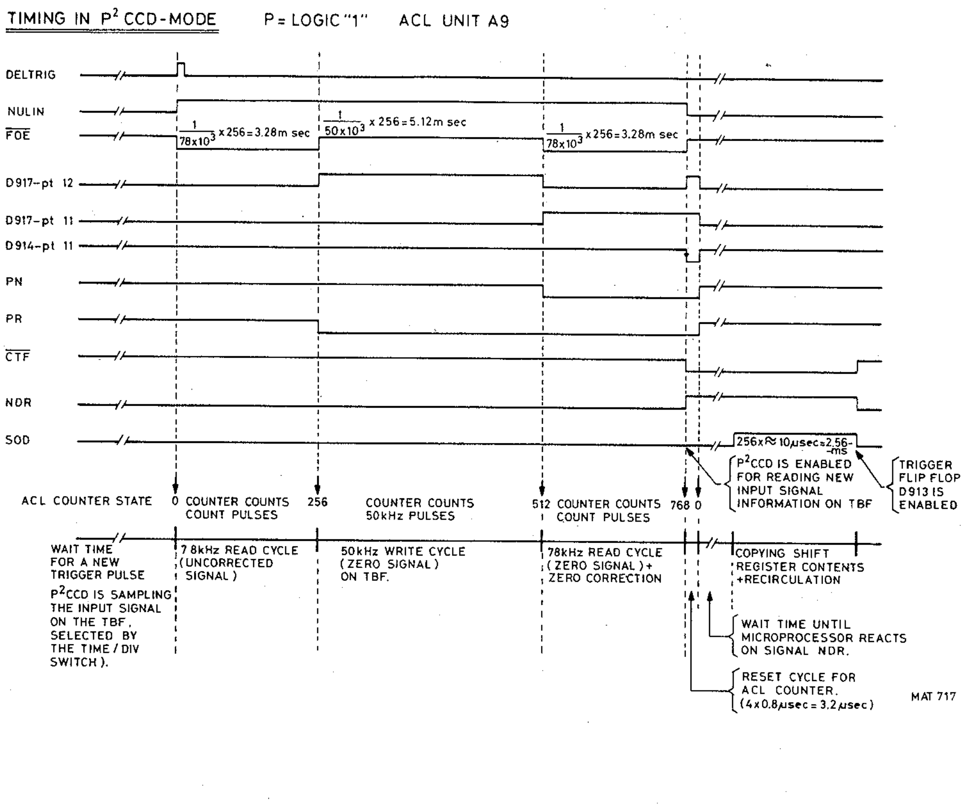


Fig. 6.2.29

Flip-flop NDR is then reset by the positive-going edge of the $\overline{SOD}$ signal via the flip-flop consisting of NAND-gates D903, and signal $\overline{CTF}$ goes to logic 1 so enabling trigger flip-flop D913 again.

The NDR signal will also be generated while the CLEAR button on the front panel is operated.
Signal $\overline{CLR}$ is then at logic 0.

6.2.9.3. Timing in Direct mode

In the Direct mode the flip-flop D913 is switched to logic 1 by a trigger pulse DELTRG in normal trigger mode and by $\overline{AUTRI}$ in the AUTO mode, both signals being generated by the delayed trigger unit (A13).

On receipt of a trigger, flip-flop D913 is switched and applies a logic 1 to the D-input of NDR flip-flop D902 via NAND-gate D903 (1,2,3).
The NDR flip-flop switches to logic 1 at the first COUNT pulse on its clock input (received via multiplexer D901).
This commences an NDR cycle to copy the shift register contents into the ACCU memory in the way already described for the P-mode.

The NDR flip-flop is reset by the positive-going edge of the $\overline{SOD}$ signal via the flip-flop comprising NAND circuits D903. Simultaneously, the acquisition control logic counter starts counting 256 COUNT pulses. This start is initiated by the $\overline{NDR}$ signal on the clock input of flip-flop D902, received via multiplexer D916.
At this same start time, a logic 0 on output 8 of flip-flop D902 causes output $\overline{CTF}$ of multiplexer D901 to go to logic 0. This results in a reset of the trigger flip-flop D913.

The acquisition control logic counter counts up to state 256. This state is decoded, resulting in a logic 1 on pin 12 of counter D917, which is applied via inverter D919 (8,9) and multiplexer D916 to flip-flop D902.

The counter is then reset in the way described for the P-mode.

At this moment, it is established that at least 256 new samples of the input signal are stored in the shift register, so the total shift register contents are refreshed (i.e. a type of trigger hold-off).

Resetting the acquisition control logic counter results in signal $\overline{CTF}$ going to logic 1, thus again enabling the trigger flip-flop D913.
This prepares the flip-flop to receive another trigger to start a new D-mode cycle.

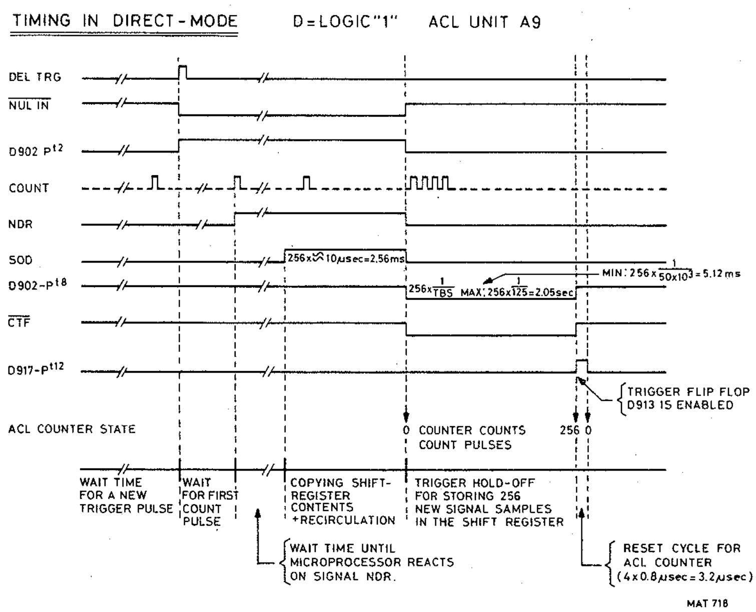


Fig. 6.2.30.

6.2.9.4. Timing in Roll mode

If ROLL-mode is selected and the RUN/STOP pushbutton is pressed once, the ROLL-mode action is started by TBS pulses generated on time-base unit A12 after a start signal from the microprocessor.
HOCON DRS pulses are derived from the TBS pulses on trigger unit A22. Each HOCON DRS pulse applied to the ACL unit A9 starts an analog-to-digital conversion of a new input signal sample.
The ACL unit is set to ROLL-mode by the R control signal.
In the ROLL-mode the D-input of the NDR flip-flop D902 is permanently at logic 1 via NAND-gate D903 (1,2,3).
Each time a new signal sample is stored in the shift register, a COUNT pulse is generated and an NDR cycle started as described for the P-mode.

During this NDR cycle, the entire shift register contents are copied by the ACCU memory and re-circulated.

The microprocessor and its software calculate the number of NDR cycles and after each 256 the ACCU memory contents are copied in one of the memories STO3, STO2, STO1 under software control.
The last 256 samples remain in the ACCU memory. The ROLL-mode is now finished, this being indicated by a flashing RUN lamp on the instrument front panel.

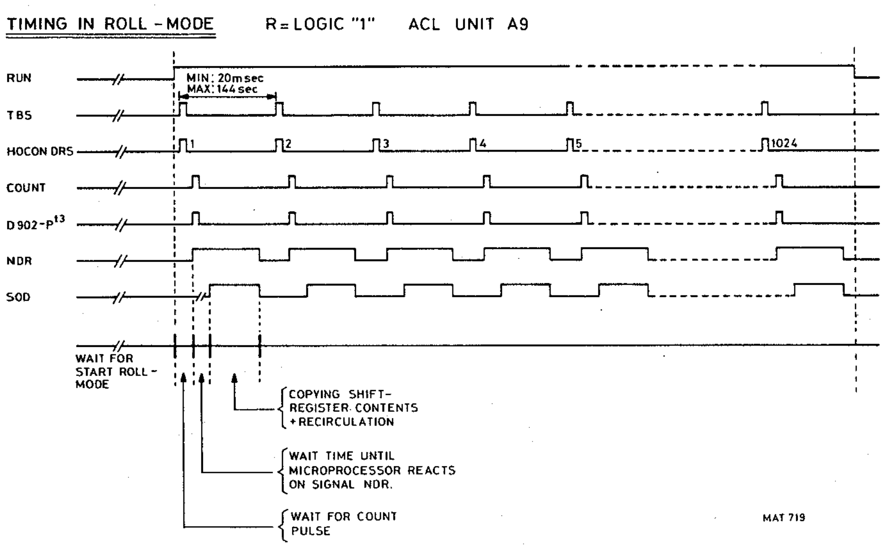


Fig. 6.2.31.

6.2.9.5. Timing in Sampling mode

The control signal S sets the ACL unit in the Sampling mode.

Correct functioning in this mode requires that signals of a repetitive nature are applied to the input channels of the instrument.

Each sampling cycle is started with the staircase counter in the zero position and a pre-determined LEVEL setting.
During one sampling cycle 256 samples of the input signal are stored in the shift register to build a complete signal picture. Each input trigger signal takes one sample of the input signal as now described.

On each trigger signal a fast ramp signal is generated (on unit A22) which is compared with the output of a DAC circuit DACSTAIR, D904. This circuit is coupled to the staircase counter to convert the counter state into the analog signal DACSTAIR.
At the crossover point determined by each comparison of the fast ramp signal and the DACSTAIR signal, an HOCON DRS pulse is generated to start the ADC conversion of the new signal sample.
The time between samples depends on the fast ramp speed which, in turn, is determined by the time-base frequency setting.

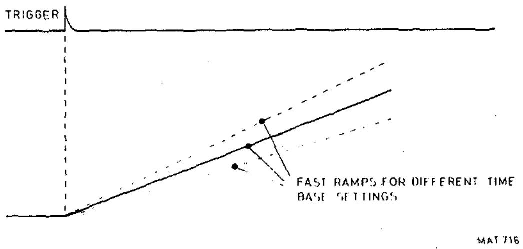


Fig. 6.2.32.

After each conversion, a COUNT pulse is counted by the staircase counter, which causes the DACSTAIR output signal to increase by one step (40 mV).
In this way, the time between the trigger pulses and the generation of the HOCON DRS signal increases so that each new sample is taken one step later.

The shift register is completely filled after 256 samples and its contents can be copied by the ACCU memory. This is initiated by state 256 of the staircase counter. A logic 1 on pin 12 of the counter D917 causes it to reset to zero as already described in the P-mode. The logic 1 level on output 8 of reset flip-flop D902 is fed to the clock input of the NDR flip-flop via multiplexer D901. This starts an NDR cycle and the shift register contents can be copied in the ACCU memory. After this, the staircase counter is again enabled for counting by the positive-going edge of the $\overline{\text{NDR}}$ signal via multiplexer D916 and a new sampling cycle is started.

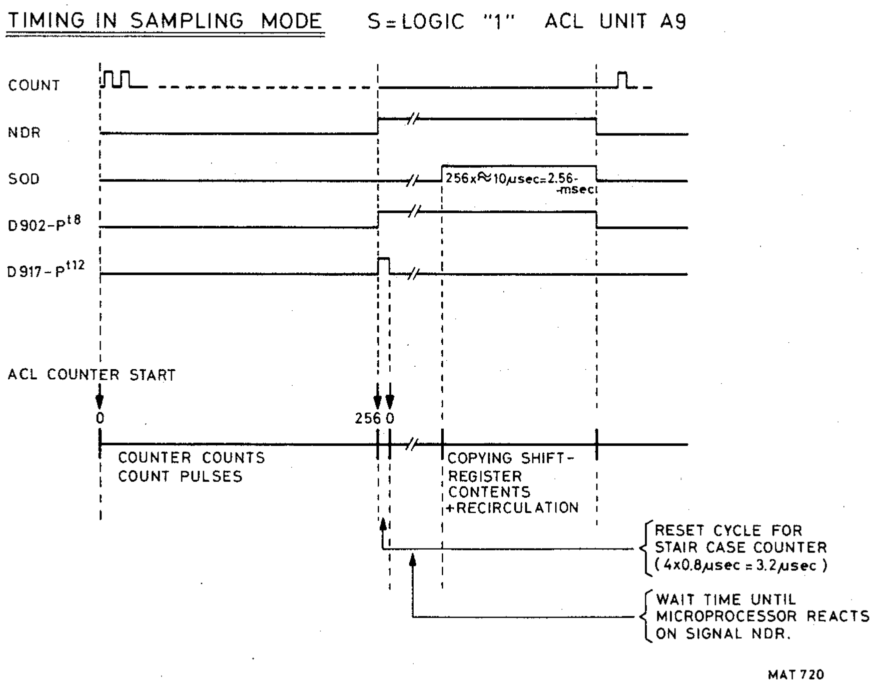


Fig. 6.2.33.

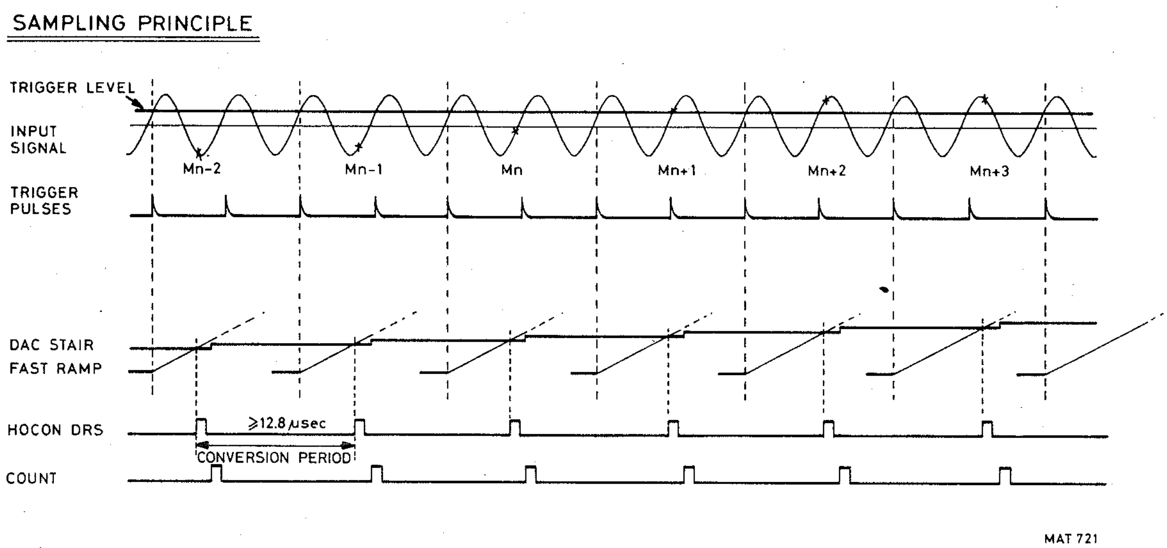


Fig. 6.2.34.

As a result, clean output signals are produced, which are applied via multiplexer D1008 and amplifier stage D1017 to the conversion unit A8 as the V OUT signal.

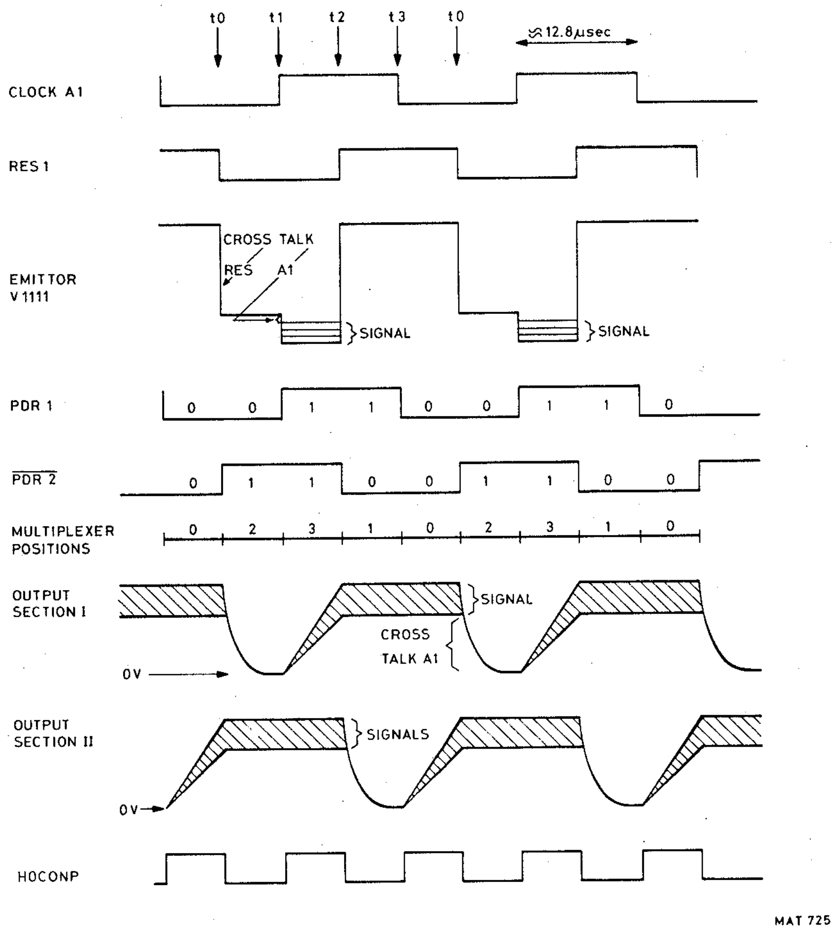


Fig. 6.2.40.

Before time t_0, signal RES1 is at logic 1, which causes the P²CCD reset FET to conduct. The parasitic capacitor C_p of the source-follower gate is then charged to the level of the DRAIN RS1 voltage.

At the moment t_0, signal RES1 switches to logic 0 and the reset FET goes non-conducting.
Due to the crosstalk of signal RES1 present on the source-follower gate, a voltage jump appears on the emitter of transistor V1111.

During the time between t_0, and t_1, the analog multiplexer D1018 is set to position 2 by its control signals PDR1 and $\overline{\text{PDR2}}$, Capacitor C1012 is then charged to the level on the emitter of V1111. At the same time, integrator capacitor C1034 will be discharged to 0 V via position 2 of the multiplexer.

At t_1 (the positive-going edge of the clock-signal A1), a signal sample is fed to the source-follower gate, which results in a change of the voltage across C_p. This voltage across C_p is also influenced by crosstalk from the clock-signal A1. The emitter of transistor V1111 follows the voltage changes across C_p.

During the time between t_1 and t_2, the multiplexer D1018 is set to position 3. The difference between the emitter voltage of V1111 and the voltage across C1012 is now applied across R1079 and is integrated by the circuit D1009 and C1034. As can be seen from the timing diagram, the crosstalk of RES1 is now completely suppressed.

During the time between t_2 and t_3, the analog multiplexer switches to either position 1 or 0, but the multiplexer is not then enabled (signal PDR2 on the enable input G4). The output voltage therefore remains available on pin 6 of D1009.

A similar external output circuit is available for signal OUT PB, resulting in integrated voltages on pin 6 of D1011. Because of the differences in control signals PDR1 and PDR2, the signals are 180° phase-shifted.

The signals that are read into the P^2CCD for temporary storage need to be converted into digital information for permanent storage in a digital memory.
For this purpose, the output signals on pins 6 of D1009 and D1011 are applied to a multiplexer, D1008.

This multiplexer switches both P^2CCD output signals to one single serial output signal V OUT, when P-mode is selected (signal P at logic 1).
Signal PDR2 is responsible for switching over from output section I to output section II. For the DRS modes the multiplexer D1008 switches the signal DRS to its output V OUT.

Amplifier stage D1017 can also be switched as an inverter by multiplexer D1008.
This is necessary to correct for the different phases of the two signals in the two sections of the P^2CCD.
Presets R1006 and R1024 provide a means of gain adjustment for the two P^2CCD sections.
Signal V OUT is applied to conversion unit A8.

6.2.10.4. Control signals generator

In the P-mode, the signals P, PRES, $\overline{\text{FOE}}$ and 78 kHz are converted from TTL to ECL by D1013.
As long as signal PRES = logic 1, these signals control the two D-type flip-flops D1003, which generate the signals WREP and RDEP.

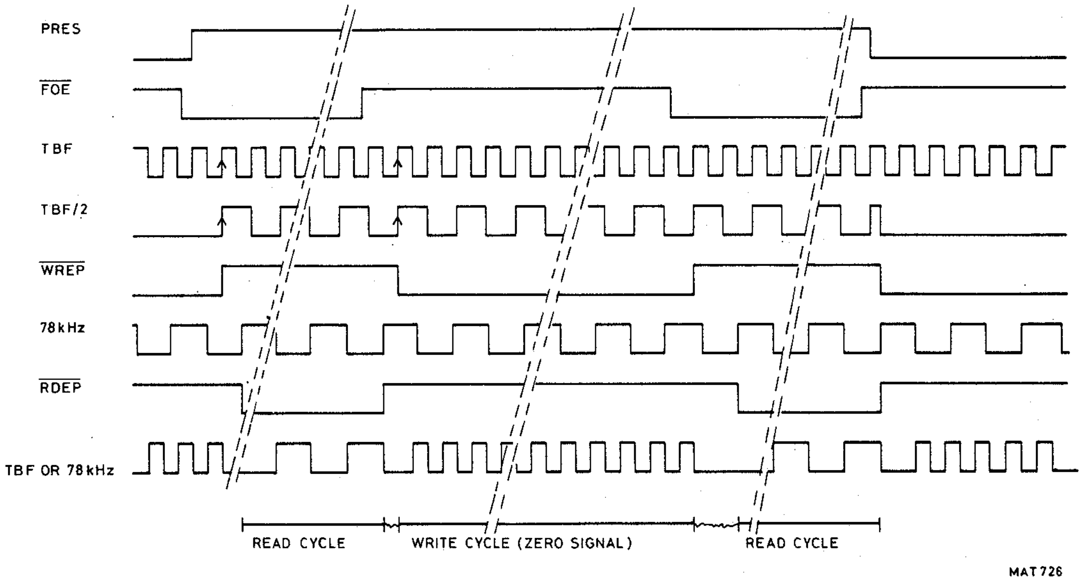


Fig. 6.2.41.

As shown in the timing diagram, during the time that signal $\overline{\text{WREP}}$ = logic 0, new signal samples will be shifted into the P^2CCD with a clock-frequency signal derived from signal TBF. (WREP: WRITE ENABLE P-MODE).

Signals WREP and $\overline{\text{WREP}}$ are only switched synchronously with even TBF pulses (TBF/2) in order to achieve precise zero-correction (see ACL unit A9). This is realised by dividing the TBF pulses using the lower flip-flop of D1014, resulting in signal TBF/2, which is used as a clock-signal for flip-flop WREP.

During the time that signal $\overline{\text{RDEP}}$ = logic 0, the P^2CCD contents are shifted out with a clock-frequency derived from signal 78 kHz.

Signals RDEP and $\overline{\text{RDEP}}$ are only switched synchronously with the 78 kHz signal.
(RDEP: READ ENABLE P-MODE).

The signal on pin 10 of NOR-gate D1004 is built up by TBF or 78 kHz.
This signal, which is applied to pin 6 of D1006, is also inverted by D1004 and applied to pin 11 of D1006. These flip-flops and the associated circuits that follow (D1007, D1012) generate the signals listed below in accordance with the timing diagram.

RES1:	Reset signal for P^2CCD output section I
RES2:	Reset signal for P^2CCD output section II
P DRIVE:	P^2CCD phase signal
PDR1 & PDR2:	Control signals for multiplexers D1018, D1019 and D1008
CLKDR:	Drive signal for clock-pulse generator.

Integrated circuits D1012 are ECL/TTL converters of which one output is connected to an internal reference voltage of −1,2 V.

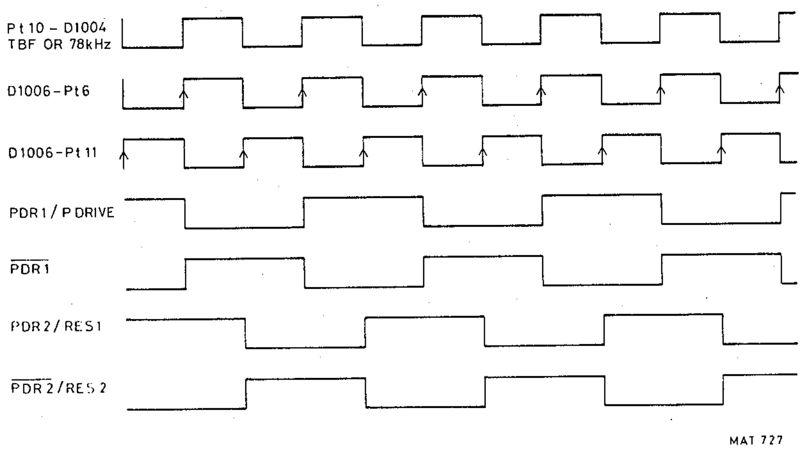


Fig. 6.2.42.

The whole system is inactive while signal $\overline{\text{PECL}}$ from the time-base unit is at logic 1. Signal P DRIVE will then be permanently at logic 1.
Furthermore, the generation of signals PDR1, PDR2, $\overline{\text{PDR2}}$, PDRIVE, RES1 and RES2 is inhibited while signal WREP is at logic 1. This signal is at logic 1 during the reading of new signal samples into the P^2CCD. Signals RES1 and RES2 are then positive to open the reset FET during reading in.

Signal HOCONP (Hold and Convert in P-mode)

HOCONP pulses are only generated during the reading of the P2CCD contents. These pulses are derived from the 78 kHz pulses via NOR-gate D1004 while signal $\overline{\text{RDEP}}$ = logic 0 (RDEP: READ ENABLE in P-MODE). Immediately the first P2CCD signal sample is available for conversion to digital, the leading edge of the first HOCONP pulse has already passed. Therefore, this analog-to-digital conversion has to be started on the second HOCONP pulse.
For this reason, the first HOCONP pulse is suppressed by the upper flip-flop of D1014 as shown in the following diagram.

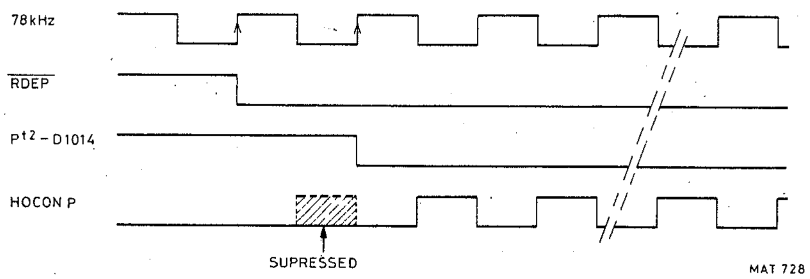


Fig. 6.2.43.

6.2.10.5. Clock-pulse generator

The four clock-pulse signals P2, A2, P1 and A1 needed to shift the signal samples through the P2CCD, are produced by clock-pulse generator D1001 in combination with the LC filters on unit A11, which are terminated by 50 Ω resistors to minimise reflections. One of these double-T filters is connected between the output pins 7 and 6, and the other between the output pins 9 and 10 of clock-pulse generator D1001.
The resulting four square-wave clock-pulse signals have a high level of +11,4 V and a low level of +2 V as shown below.

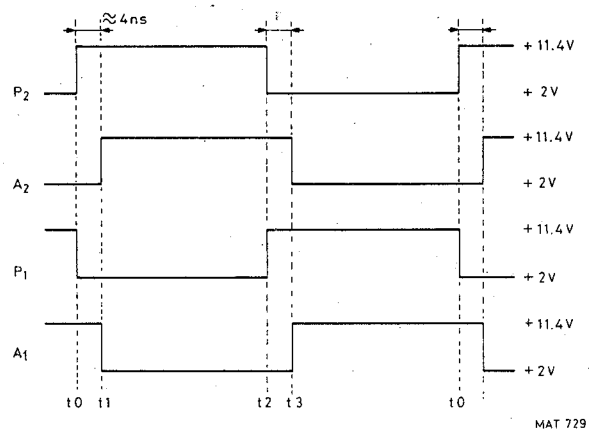


Fig. 6.2.44.

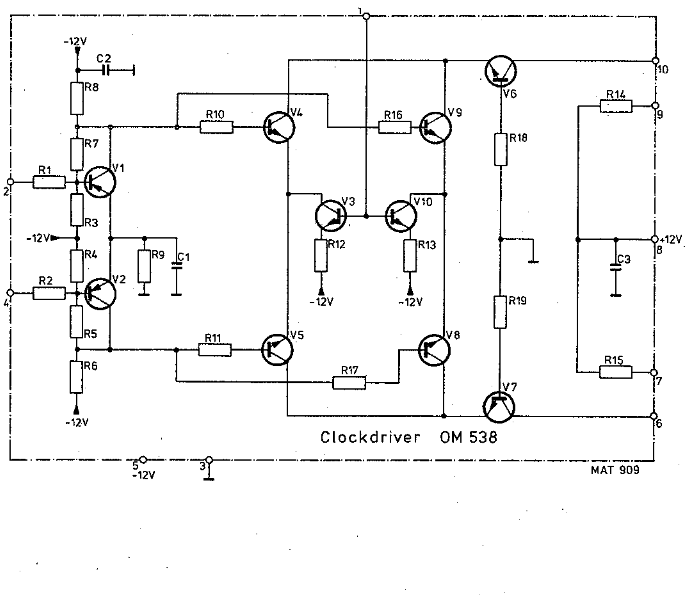


Fig. 6.2.44a

6.2.11.2. Input section

Each of the two sections of the P^2CCD circuit has its own input section. One of these input sections is now described. This particular section has the following inputs:

IN1 (pin 22)	this input is connected to the clock signal P2 in such a way that the d.c. voltage level on IN1 is always about 13 V more positive than the P2 signal level.
P11IN (pin 21)	this is a threshold voltage set to +6 V approx.
A11IN (pin 17)	this is connected to the analog input signal P AMP OUT 1 with a maximum amplitude of 1 V peak-peak on a d.c. bias level of about +7,5 V.

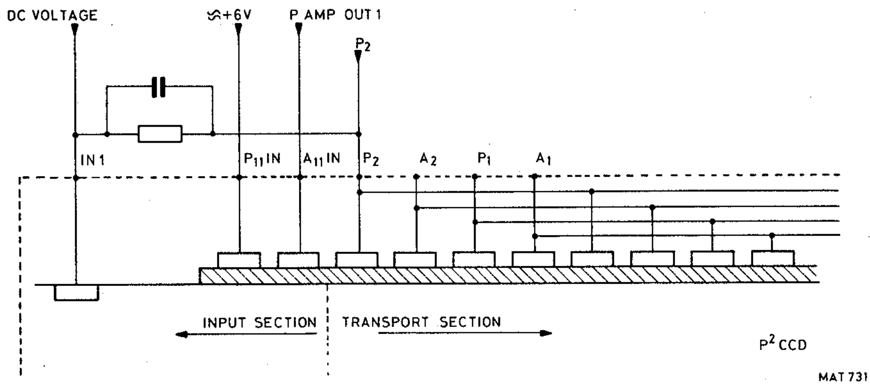


Fig. 6.2.48.

For correct sampling of the input signal, it is most important that the low level (+2 V) of the clock signal P2 remains constant. For higher frequencies, the amplitude of the clock signal P2 decreases due to the capacitive loading caused by the P^2CCD circuit.
A control loop is used to ensure that the low level of P2 remains constant.
The clock signals P2 and P1 are measured by the circuit V1101, V1117, which results in a feedback signal CLAFB for the four-phase clock-pulse generator on unit A10.
(CLAFB = CLOCK AMPLITUDE FEEDBACK).

6.2.11.3. Transport section

The four clock signals P2, A2, P1 and A1 are used to shift information in and out of the P2CCD. These signals, generated on CCD logic unit A10, are derived from the 125 kHz ... 50 MHz input frequency (TBF) from the time-base circuit (A12) when reading in, and from a 78 kHz input frequency when reading out.

Each stage inside the P2CCD consists of four gates that are isolated from each other, and are controlled by the four clock signals as shown in the following diagram.

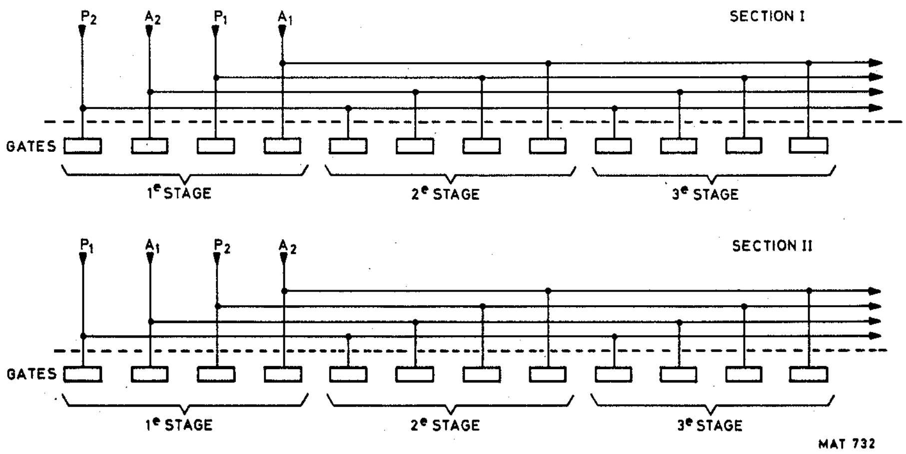


Fig. 6.2.49.

The charges are transported in the following way:

Assume for instance that a negative charge is brought under a positive gate. If the next gate is made positive and the previous gate is made negative, the charge will be repelled in the direction of the position gate.

Displacement of charges is achieved in practice by changing the levels on the gates by the four periodically changing clock-pulses. For a description of the clock-pulse generator, refer to unit A10.

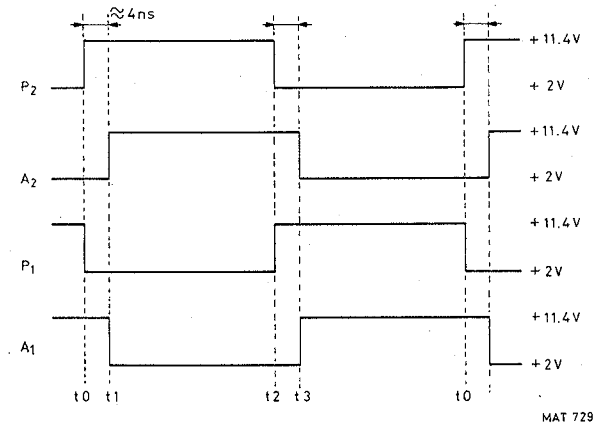


Fig. 6.2.50. Timing clock signals

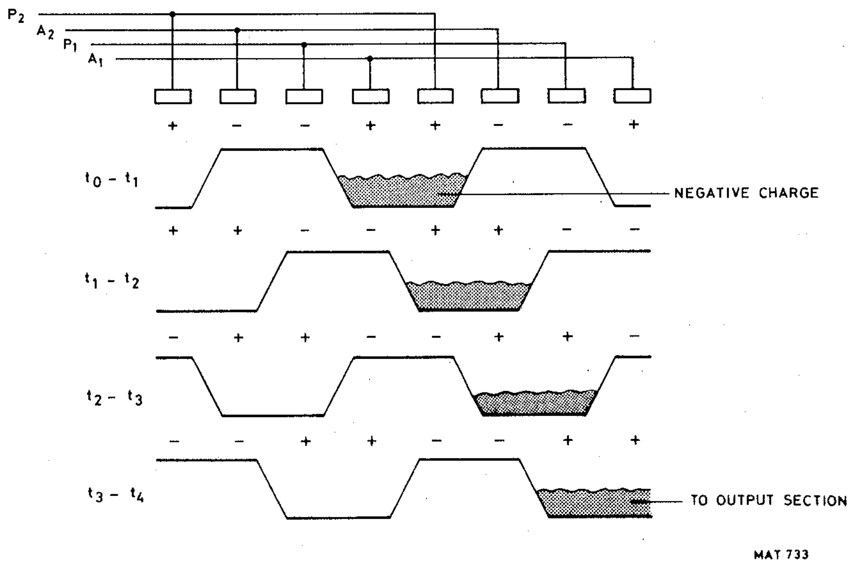


Fig. 6.2.51. Displacement of a negative charge as a function of the clock voltages.

6.2.11.4. Output section

Each of the two P2CCD sections has its own output stage, as now described.

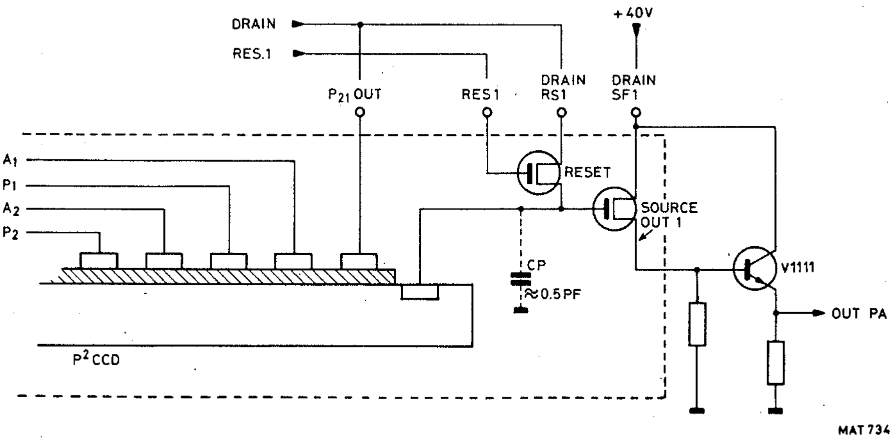


Fig. 6.2.52.

On every positive-going edge of the clock signal A1 a charge will load the parasitic capacitor C_p of the source-follower gate (previously discharged to the DRAIN RS1 voltage level by the reset FET).

The level across C_p will leave the output section via the appropriate source-follower. Both FET transistors are also part of the P2CCD circuit.
The output signal is approx. 100 mV for an input signal (Vin) of 1 Vp-p.
This source-follower output signal is applied to an emitter-follower V1111 which in turn feeds it as signal OUTPA to an output amplifier on unit A10.

6.2.11.5. P2CCD circuit in dual-channel mode

In the dual-channel mode, channel A signal is shifted to section I and channel B to section II. The clock signals for the two sections are in anti-phase, which results in a situation where the P2CCD itself acts as a chopper.
The chopper frequency depends on the TIME/DIV switch setting.
This dual-mode of working results in 128 samples per channel being stored, instead of 256.

6.2.12. Time-base unit A12

The time-base unit generates a number of control signals of different frequencies derived from the microprocessor clock-pulse output signal of 2,5 MHz.

6.2.12.1. Encoding TIME/DIV settings

Depending on the setting of the TIME/DIV switch, one of these frequencies is selected and applied to other units as signals TBF (time-base fast, used in P^2CCD mode) or TBS (time-base slow, used for other modes).

The relation between the TIME/DIV switch settings and the signals TBF and TBS is such that there are always 25 pulses (TBF or TBS) generated per horizontal division.

The settings of the TIME/DIV switch are read by the microprocessor system (unit A2).
The microprocessor loads the 8-bit latch D1221 with a byte of data according to the TIME/DIV settings listed in the following table.
Latch D1221 is selected when the microprocessor generates address 8Ø6ØH.
When the microprocessor places this address on the address bus, signal $\overline{IO6}$ goes to logic 0.
This $\overline{IO6}$ signal combined with the $\overline{WR}$ signal enables data latch D1221 to latch the data present on the data bus.

The output signals of latch D1221 have the following functions:

DØ ... D4*	used to control the various multiplexers on time-base units A12.
D5*	enables or disables the output signal TBS.
D6* and D7*	these signals together, control decoder D1216, which results in the four mode signals: P – P^2CCD mode D – Direct mode R – Roll mode S – Sampling mode

TIME/DIV	FREQUENCY	MODE	D7	D6	D5	D4	D3	D2	D1	DØ
5 ns/div		S	1	1	0	0	0	1	1	0
10 ns/div		S	1	1	0	0	0	0	0	1
20 ns/div		S	1	1	0	0	0	1	0	0
50 ns/div		S	1	1	0	0	0	1	0	1
0.1 µs/div		S	1	1	0	0	0	0	0	0
0.2 µs/div		S	1	1	0	0	0	1	1	1
	TBF									
0.5 µs/div	50 MHz	P	0	0	0	0	1	1	0	1
1 µs/div	25 MHz	P	0	0	0	0	1	1	1	0
2 µs/div	12,5 MHz	P	0	0	0	0	1	0	1	0
5 µs/div	5 MHz	P	0	0	0	0	1	0	1	1
10 µs/div	2.5 MHz	P	0	0	0	1	0	0	0	1
20 µs/div	1.25 MHz	P	0	0	0	1	0	0	1	0
50 µs/div	0.5 MHz	P	0	0	0	1	0	0	1	1
0.1 ms/div	0.25 MHz	P	0	0	0	1	1	0	0	1
0.2 ms/div	125 kHz	P	0	0	0	1	1	0	1	0
	TBS									
0.5 ms/div	50 kHz	D	1	0	1	0	0	0	0	0
1 ms/div	25 kHz	D	1	0	1	0	0	0	0	1
2 ms/div	12.5 kHz	D	1	0	1	0	0	0	1	0
5 ms/div	5 kHz	D	1	0	1	0	0	1	0	0
10 ms/div	2.5 kHz	D	1	0	1	0	0	1	0	1
20 ms/div	1.25 kHz	D	1	0	1	0	0	1	1	0
50 ms/div	500 Hz	D	1	0	1	0	1	0	0	0
0.1 s/div	250 Hz	D	1	0	1	0	1	0	0	1
0.2 s/div	125 Hz	D	1	0	1	0	1	0	1	0
	TBS									
0.5 s/div	50 Hz	R	0	1	0/1	0	1	1	0	0
1 s/div	25 Hz	R	0	1	0/1	0	1	1	0	1
2 s/div	12.5 Hz	R	0	1	0/1	0	1	1	1	0
5 s/div	5 Hz	R	0	1	0/1	1	0	0	0	0
10 s/div	2.5 Hz	R	0	1	0/1	1	0	0	0	1
20 s/div	1.25 Hz	R	0	1	0/1	1	0	0	1	0
30 s/div	5/6 Hz	R	0	1	0/1	1	0	1	0	0
60 s/div	5/12 Hz	R	0	1	0/1	1	0	1	0	1
120 s/div	5/24 Hz	R	0	1	0/1	1	0	1	1	0
360 s/div	5/72 Hz	R	0	1	0/1	1	1	0	0	0
900 s/div	5/180 Hz	R	0	1	0/1	1	1	1	0	1
1800 s/div	5/360 Hz	R	0	1	0/1	1	1	1	1	0
3600 s/div	5/720 Hz	R	0	1	0/1	1	1	1	1	1

D5 = 1 → RUN
D5 = 0 → STOP

6.2.12.2. Generation of signals 1.25 MHz, 0.5 MHz, 250 kHz, 156 kHz, 78 kHz

The 2.5 MHz clock-pulse signal from the microprocessor is divided by factors of 2, 5 and 10 in divider D1206, resulting in signals 1,25 MHz (pin 3), 0.5 MHz (pin 4) and 250 kHz (pin 6) respectively.

Two other signals are derived from the 1.25 MHz signal by D1207, which divides by factors of 8 and 16. These divisions produce a signal of 156 kHz for use in the Z-amplifier and a signal of 78 kHz for reading out the contents of the P^2CCD unit.

6.2.12.3. Generation of TBS signals for the D and R modes

The 0.5 MHz signal on pin 4 of D1206 is applied to pin 10 of D1206, the first of a chain of dividers consisting of D1206, D1204, D1203, D1202 and D1201.
The first three of these divide by a factor of ten, thus producing the frequencies 50 kHz, 5 kHz, 500 Hz, 50 Hz and 5 Hz.
The 2.5 kHz output from D1204 pin 11 is applied via inverter D1218 (8, 9, 10) to the final amplifier unit A20 for generating the CAL voltage.

Pin 2 of D1203, normally at 500 Hz, can be switched to 2.5 MHz by switch S1201 for test purposes in the ROLL-Mode.

Circuit D1202 divides the 5 Hz input signal by a factor of 6 to give an output signal with a frequency of 5/6 Hz. In turn, D1201 divides this 5/6 Hz input signal by a factor of 12 if D2* is logic 0, and by a factor of 15 if D2* is logic 1, thus producing frequencies of 5/72 Hz or 5/90 Hz.

All these frequencies are routed to multiplexer D1214, the outputs of which are controlled by signals D2*, D3* and D4*.
Only one of the input frequencies appears on output 3 of D1214 and is applied in one of two ways to multiplexer D1219:

- directly to input 6 of D1219, or
- first divided in D1207 by factors of 2, 4 and 8 and then applied to inputs 5, 4 and 3 of D1219.

Multiplexer D1219 is controlled by signals DØ* and D1*.
The final selected frequency, obtained via NOR-gate D1217 as signal TBS, is applied to the trigger unit.
The output TBS can be disabled by flip-flop D1222, under the control of the D5* signal.
Signal TBS is blocked at the end of the ROLL-mode and in the P-mode. D* is then logic 0.

6.2.12.4. Generation of TBF signals for the P-mode

Signals of a higher frequency than the microprocessor clock-pulse output signal of 2.5 MHz are generated by means of a voltage-controlled oscillator (VCO) D1213 that has an output frequency of 100 MHz.
The output frequency of this oscillator is controlled by a d.c. voltage, VC_x on the VCO input, pin 2.
To obtain this stable VCO output, the 100 MHz output is divided by a factor of 80 in circuits D1227, D1209 and D1208. The resulting 1.25 MHz signal, VCO/80, is then compared with a reference signal of the same frequency in a phase detector, which is then used to control the VCO frequency.

The phase detector comprises the flip-flops D1211 and the associated integrator circuit. These flip-flops are set and reset in accordance with the timing diagram shown below.
The output signals on pins 1 and 12 are added and applied to pin 2 of D1212 of the integrator. The resulting signal VC_x controls the VCO to ensure a constant frequency. The VCO is only switched into circuit by signal VCOEN (VCO Enable) in the 4 TIME/DIV switch positions 0.5 µs/div to 5µs/div.

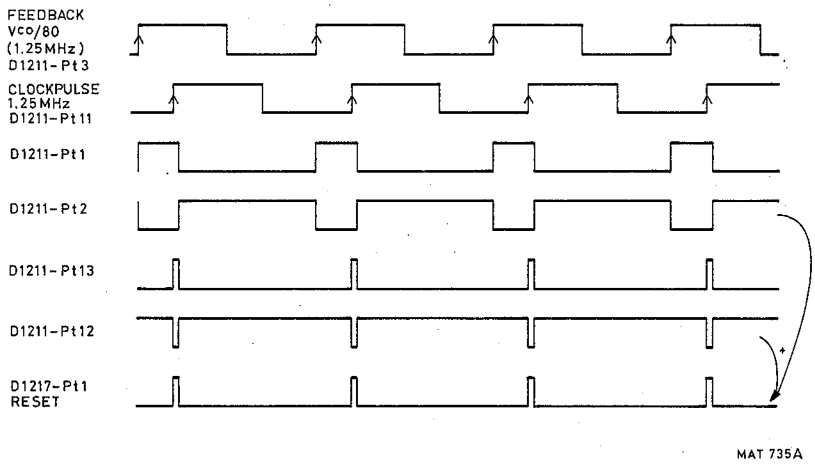


Fig. 6.2.55.

Divider D1227 derives the 50 MHz and 25 MHz signals from the 100 MHz VCO output signal, these being routed to multiplexer D1224 for selection.
The 25 MHz signal is also applied to a multiplexer D1223 via ECL/TTL converter D1231. This multiplexer selects one of the input signals 25 MHz, 2.5 MHz and 250 kHz under the control of signals D3* and D4*.

The 25 MHz output signal from D1223 is divided in D1209 by a factor of 5 and a factor of 2. From there it is divided further in D1208 by a factor of 2, giving a signal VCO/80 of 1.25 MHz on output pin 12 of D1208. This is the 1.25 MHz signal that is fed back to the phase detector for controlling the VCO frequency.

The following frequencies are also available:

output pin 9 of D1223: 25 MHz, 2.5 MHz or 250 kHz
output pin 8 of D1222: 12,5 MHz, 1.25 MHz or 125 kHz
output pin 12 of D1209: 5 MHz, 500 kHz (or 50 kHz - not used)

After selection by multiplexer D1219 (only enabled in P-mode), one of these frequencies appear on output pin 9 of D1219.

The selected signal is applied to multiplexer D1224 via a TTL/ECL converter, D1226.

Multiplexer D1224, which is controlled by DØ*, D1* and D2*, is employed for the final selection of the frequency of the output signal TBF. This signal is applied to the CCD logic unit A10 via a 50 Ω cable.
In parallel, a TBF signal is generated, which is connected via a 50 Ω cable to the trigger unit A22.

6.2.13. Delay trigger unit A13

The delay trigger unit comprises the following sub-circuits:

- The time-base AUTO circuit
- Plot output circuit and control signals for the dot-join circuit
- Down counters for trigger delay in Direct or P^2CCD mode
- Digital-to-analog converter for trigger delay in Sampling mode

6.2.13.1. The time-base AUTO circuit

The time-base auto circuit consists of D1321 and its associated components. In the absence of the TRIST signal, i.e. no trigger pulse, and with the trigger switch in the AUTO mode, the trigger flip-flop of the ACL unit A9 requires a pulse to restart. This pulse is generated by D1321 output 4 and is referred to as the $\overline{\text{AUTR1}}$ signal.

A FRUN signal can enable the output pulse of the trigger unit A22. If no TRIST pulses are available, the re-triggerable monostable multivibrator D1321 (output 12) is at the rest position with output 12 at logic high. Together with signal AUTOTB, which is also high from the AUTO switch, output 6 of D1313 goes high. This output is the FRUN signal. As this time, D1321 output 4 is enabled and, on receipt of a $\overline{\text{CTF}}$ pulse, the $\overline{\text{AUTR1}}$ signal goes active low for 3 μs approx. to preset the trigger flip-flop on the ACL unit
A frequency of 1,25 MHz is applied at input 1 of D1321 to ensure that an $\overline{\text{AUTR1}}$ pulse occurs.

6.2.13.2. Plot output circuit and control signals for the dot-join circuit

The X OUT and Y OUT signals derived from the final amplifier unit A20 are applied to the sample-and-hold gates D1328 and D1329. At a particular moment, determined by the software, the data line D3 goes high for 30 μs approx. and D1328 and D1329 respectively will now hold the instantaneous values of X OUT and Y OUT for 17 ms approx. The outputs of the sample-and-hold gates are buffered by operational amplifiers D1319 and D1331 to obtain output voltages of 1 V full-scale for X and Y plotting.

The pen-lift circuit is controlled by a high level on data line D4 at the moment that D1318 is enabled. Changeover of the soldered dot-connection between D1323 and R1334 gives the possibility of active high or active low pen-lift operation. The output is an open-collector output with a maximum load capability of 1 A.

The following pulses are all derived from the $\overline{\text{WR}}$ pulse by a network of dividers and logic gates, and serve to control the dot-join circuit (final amplifier A20):
QØ and Q1; ZDJ and RESDJ, and TRSH.
The signals QØ and Q1 control the channel separation. Signal TRSH controls the sample-and-hold gates of the dot-join, the signal RESDJ serving to control the reset dot-join for the X channel. The ZDJ signal generates the blanking pulse on the microprocessor board and discharges the capacitor of the sawtooth generator on the final amplifier unit.

6.2.13.3. Down counters for trigger delay in Direct or P^2CCD modes

The input of the counters may be the signal TBF or TBS. Signal TBF is at ECL-level at a frequency of 125 kHz ... 50 MHz. Conversely, the TBS signal is at TTL-level and at a frequency below 125 kHz.
Both signals are always 25 pulses per division. The signal TBS is converted into ECL-level and applied via a wired-OR circuit to D1306, which functions as a divide-by-five circuit (output on pin 15). Via ECL/TTL converter D1307, the signal is applied to the 4-stage down counter consisting of D1308, D1309, D1311 and D1312. This system operates as follows:

The preset trigger delay in the DIV display is converted to a particular number by the microprocessor system and this number is set on the data-bus and loaded in the counters in two cycles.
First, D1308 and D1309 are loaded by enabling them (on D1308-1 and D1309-11) with pulse $\overline{\text{IO8}}$ together with address 8086 and the $\overline{\text{WR}}$ pulse. After this, D1311 and D1312 are loaded by enabling them (pins 11) with pulse $\overline{\text{IO8}}$ in combination with address 8085 and $\overline{\text{WR}}$ pulse.
The number now loaded must be counted down. The count pulses are derived from signals TBS or TBF, which may be enabled by $\overline{\text{EDCT}}$ applied via TTL/ECL converter D1303 and flip-flop D1304 to input 7 of D1306.
The pulse $\overline{\text{EDCT}}$ is generated under the following conditions:

- Reset input 1 of D1317 is high.
- TRIST pulse goes high.

In this event, $\overline{\text{EDCT}}$ goes active, so set input 5 of D1304 goes low, and on receipt of a TBS or TBF pulse at clock input 6 of D1304, output 3 goes high and enables D1306 as a five-counter.
After counting down to zero, output 13 of D1312 goes low and via AND-gate D1316 (8, 9, 10) the reset input 1 of D1317 goes low and output 6, the $\overline{\text{EDCT}}$ pulse, goes high to disable D1306.

Divider D1306 must be blocked during the new loading of the down counter. This is achieved by the pulse NTSC which remains low during loading, and D1317 reset 1 remains low.
After loading, D1317 reset 1 goes high and on receipt of a TRIST pulse, signal $\overline{\text{EDCT}}$ reverts to the active state.
If the counter is blocked, the signal DELTRG goes high via D1323 and D1316 (4, 5, 6).

6.2.13.4. Digital-to-analog converter for trigger delay in Sampling mode

In the sampling mode, an analog signal is required to delay the trigger. This signal is derived from the digital-to-analog converter D1327, which is loaded with the information of the data-bus when enabled by pulse $\overline{\text{WR}}$ in combination with $\overline{\text{IO8}}$ and address 8086.
The digital information is coded by the software and is converted into an analog voltage. This is a d.c. voltage for the time during which no change is made in the delay setting. The total delay possible in the sampling mode is 100 divisions. These 100 divisions are digitally divided into 200 steps; that is, each division delay is digitally two steps. On conversion, it is then 80 mV/division.
The function of the trigger delay is explained in the description of the trigger unit A22.

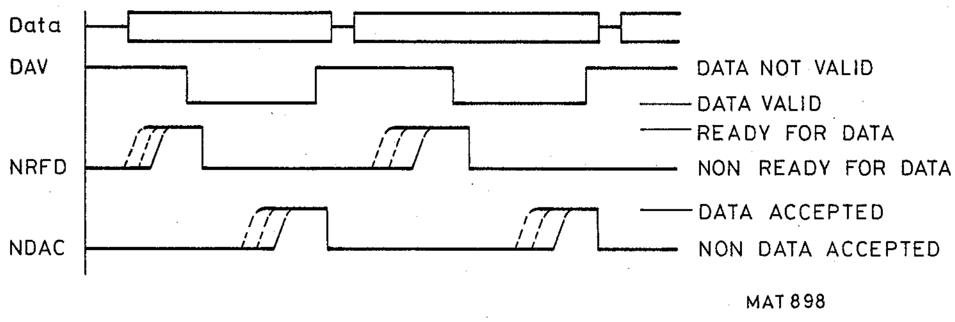
Note: Bear in mind that the principle of the oscilloscope with a trigger delay of zero means that the DELTRIG pulse always appears 10 divisions after the TRIST pulse.

6.2.14.1 General description (refer to block diagram).

An IEC bus line interface is used in multidevice systems to connect the instruments in parallel to the same interface lines. Each instrument has its own specific address (selected with switches in the instrument) so that an instrument is only listening after it has received its specific address, in IEC terms is called **My listen Address (MLA).** The Listen addresses are generated by the controller of the system (e.g. a computer) and are transmitted via the data lines of the bus during an address or interface message the attention line (ATN) is active to indicate that the information on the data lines have a special interface function.
The IEC bus can be split up into three functional parts: the data bus, the handshake bus and the management bus.

- **The Data Bus** is used to transport messages for the device functions as well as for the interface functions and consists of 8 lines **(D101...8).**
- **The Handshake Bus** controls the correct transfer of data bytes with the next three signals.

Data Valid (DAV) indicated the condition of information on the 8 DIO lines.
Not ready for data (NRFD) indicates the condition of readiness of device (s) to accept data.
Not data accepted (NDAC) indicates the condition of acceptance of data by devices.
A timing diagram for the handshake cycle is shown in the figure,take notice that the cycle is as fast as the slowest instrument.



- **The management bus** is used to manage an orderly flow of information **accross** the interface.

Herefore the next five signals are available:
Attention (ATN) specifies how data on the DIO lines are to be interpreted. Active indicates a message is transferred via the data bus (for example a listen address), not active status is present during normal data transfer (for example a command for the oscilloscope).
Interface clear (IFC) places the interface of all interconnected devices in a known quiescent state.
Service Request (SRQ) indicates that one of the instruments wants the attention of the controler for example to give an error message.
Remote enable (REN) sets an instrument to its remote-control mode, if it is in the addressed state.
End of identify (EOI) indicates the end of a multiple byte transfer.

NOTE: *Because of the negative logic used for the IEC-bus the signals are "true" (active) when they have a low level, HOWEVER all signals at the lefthand of the buffers D1406-07-16-17 are given for positive logic, so "true" is a high level.*

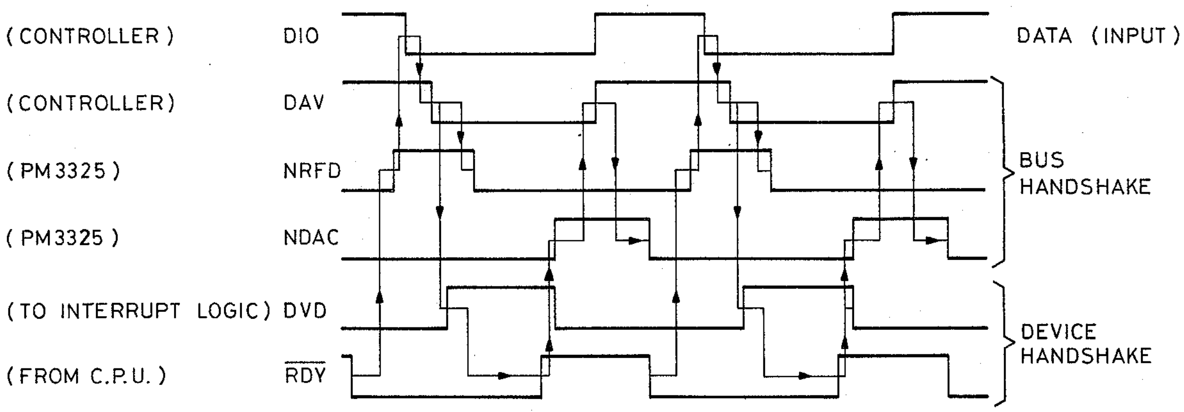
How does the interface function?

Initiation:

When the oscilloscope is switched-on, the C.P.U. reads the card code to identify which of the optional interfaces has been fitted. In this case it is the PM3325 so the C.P.U. starts with the initiation of the interface by sending control-signals to the latch D1426. The integrated circuit D1408 (HEF 4738) reads the status of the switches for MLA/MTA, TALK ONLY and LISTEN ONLY and some control signals via the two shift registers D1428 and D1429. The listen address is put into a register of D1408.
Now the interface is ready to operate.

Receiving:

First the system-controller sends a listener address via the DIO lines (so ATN is "true"). If the address is equal to the MLA in the HEF 4738, the interface becomes the listener status, this action is performed without intervention of the C.P.U. of the oscilloscope. Once in the listener state all succeeding data (without ATN="true") is read by the C.P.U. of the oscilloscope in the following way: The C.P.U. sets **(via the data bus (hit o) and the** control-signals latch) the signal READY FOR NEXT MESSAGE to the active (low) state.
After the falling edge of the RDY signal the HEF 4738 starts with the bus handshake. First Not Ready For Data (NRFD) on connector X1402-pt8 is made high by the PM3325, so the interface is ready to receive data (for remember the IEC-bus uses negative logic). Then the controller puts data on the DIO lines and makes Data Valid (DAV) on connector X1402-pt7 "true" (= low). DAV is received by the HEF 4738 and as a result Data Valid Device (DVD) on pin 17 becomes "true" (= high). When DVD becomes high the data is latched into D1424. DVD is also supplied to the interrupt logic, so the C.P.U. of the oscilloscope interrupts its current program and checks the interrupt status D1423. DVD on pin 2 of D1423 is high, consequently the oscilloscope sets listen enable high, to inhibit interrupts caused by DVD and reads the contents of the input latch D1424. Subsequently the C.P.U. sets the signal ready for next message high and reads DVD, when DVD becomes low the C.P.U. resets the signals ready for next message and listen enable. The latter enables the DVD signal again to interrupt the oscilloscope.



MAT 900

6.2.18. Delay line unit A18

Unit A18 is the delay line unit, which is mounted in the instrument under the C.R.T.

The unit is electrically connected between the channel switch and the delay line compensation amplifier on unit A21.

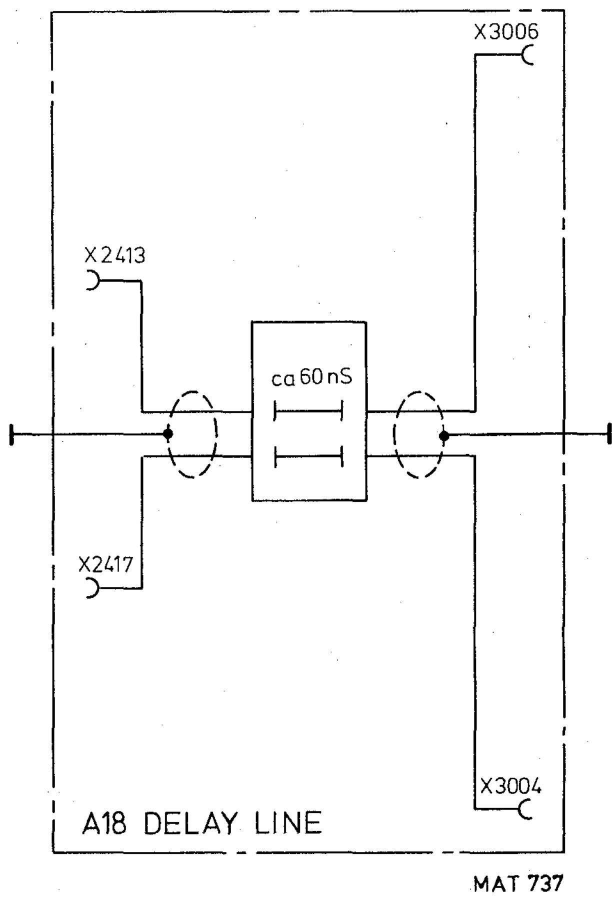


Fig. 6.2.65.

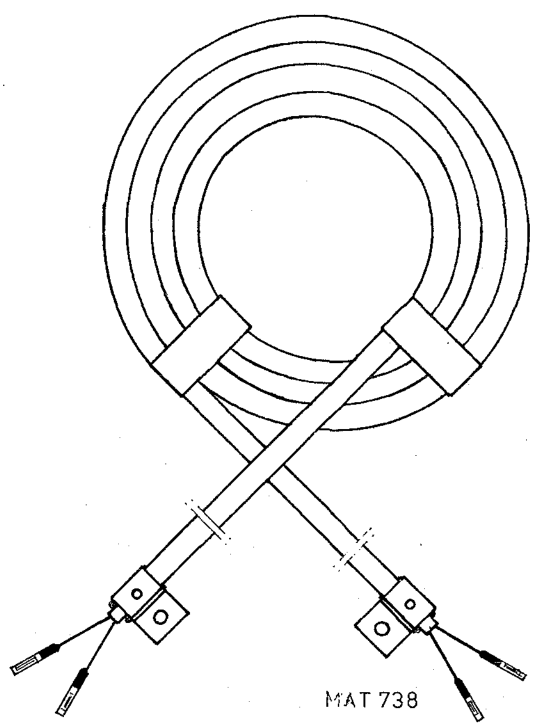


Fig. 6.2.66.

6.2.19. C.R.T. socket A19

The C.R.T. socket unit A19 consists of the socket itself (X1901) and two cables with the connectors X1506 and X2002.

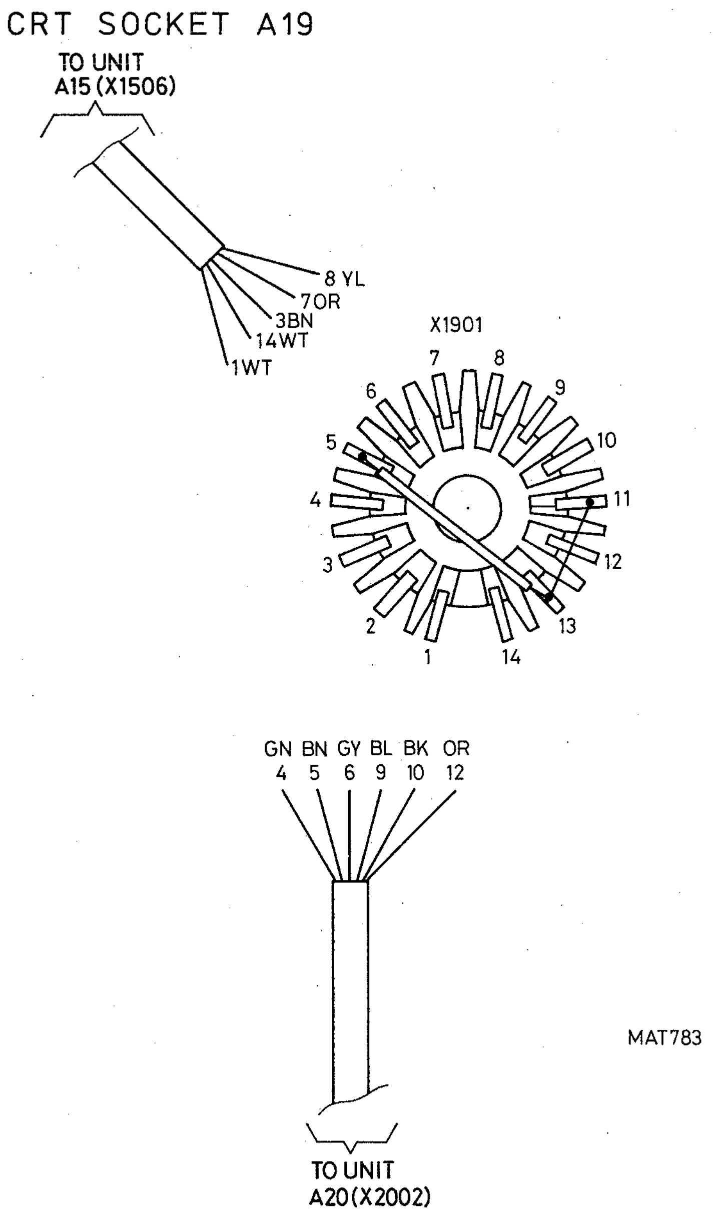


Fig. 6.2.67.

6.2.15. DC power unit A15

The DC power unit A15 contains the following circuits:

- DC output circuits
- High voltage converter and EHT unit
- Memory back-up circuit
- Protection circuit for the +5 V
- Cathode-ray tube circuit
- Z-amplifier circuit
- Illumination circuit
- Line signal circuit

Each of these circuits is now separately described.

DC output circuits

The voltages on the secondary windings of transformer T1602 on the AC power unit A16 are applied to several rectifiers and voltage doublers.

The bridge rectifiers provide for the +5 V, –5 V, +6 V, –6 V, +12 V, –12 V and +40 V supply voltages. The voltage doublers provide for the +125 V and –125 V supplies.

A –5 A supply voltage is derived from the –12 A via D1501.
A +6,5 V supply is derived from the +12 A by R1561, C1547 and V1544.
A +94 V supply is derived from the +125 V via R1572, C1548 and zener diodes V1554, V1556.

The secondary windings providing the voltages for the various circuits in the oscilloscope are completely isolated from the mains power supply.
Each supply voltage is individually rectified and smoothed.

The filament of the c.r.t. is supplied by the 6.3 V heater voltage between f_1 and f_2.

High-voltage converter and EHT unit

A sine-wave converter formed by transformer T1501 and V1501 converts the +40 V d.c. into 1500 V a.c. with a frequency of approximately 30 kHz.
This voltage is applied to a voltage multiplier on EHT unit A23. The output voltage of this multiplier, 6.5 kV, is applied to g8 of the c.r.t.

Furthermore, the converter output of 1500 V is also rectified and smoothed by V1502, C1502, R1514 and C1503 and applied to the c.r.t. cathode. It is also fed back to the positive input of operational amplifier D1503 to stabilise the cathode voltage of the c.r.t. and thus prevent any variations in c.r.t. sensitivity.

A reference voltage, obtained from divider R1578, R1591 and R1577 is applied to the negative input pin 2 of operational amplifier D1503.
The resulting voltage on pin 6 of D1503 now controls the high-voltage converter via R1526.

Memory back-up circuit

Two 1.5 V batteries can be fitted in the instrument for memory back-up.

When this battery back-up facility is used, the information that was stored in the random-access memories (RAMs) before switch-off (i.e. signal information and switch settings) is saved when the POWER switch is OFF.

The RAM memories are normally supplied by the voltage +5 BATT, which is derived from the +5 V via transistor V1549 when the instrument is switched on. In this case, the batteries are protected by diode V1546. When the POWER switch is OFF, the supply for the RAM memories is obtained from the batteries via V1546.

Protection circuit for the +5 V

This circuit protects the TTL circuits in the instrument from damage caused by an excessively high +5 V supply. When, for some reason, the +5 V supply increases to a value above 6 V approx., this +5 V supply is switched off by thyristor V1551 under the control of SCS V1527.

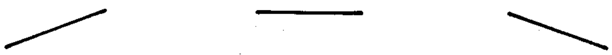
Cathode-ray tube circuit

In addition to the c.r.t., this circuit includes the intensity, focus, astigmatism, trace rotation and geometry controls.

C.r.t. controls

By means of the front-panel INTENS potentiometer R15, the intensity of the display can be continuously controlled.
Focussing of the trace is only possible by means of the internal FOCUS potentiometer R1506 (coarse control) and R1588 (fine control).

Trace rotation is achieved by the trace rotation coil circuit. The coil is mounted inside a mu-metal screen and provides a magnetic field for rotational control of the entire scan. The degree and direction of rotation is determined by the setting of the TRACE ROTATION front-panel preset R16 (screwdriver-operated).
The slider of R16 is connected to the bases of complementary emitter-followers V1558, V1559. The trace rotation coil current is supplied by these transistors, only one conducting at a time depending on the setting of R16.



OPTIMUM ADJUSTMENT

The ASTIGMATISM control R1587 enables the form of the spot to be adjusted by influencing the voltage on c.r.t. grids G2/G4.

Barrel and pin-cushion distortion are automatically minimised by the signal X-Y GEM connected to G5, G6 and G7. In this way, these screening grids are connected to a potential equivalent to the mean voltage of the deflection plates. The signal X-Y GEM is generated in the final amplifier unit A20.

Z-amplifier circuit

a. Intensity control

The output voltage of amplifier D1502 can be varied by INTENS potentiometer R15, to give variable illumination of the c.r.t. trace.

The Z-amplifier receives an input signal ZIN which originates in the microprocessor unit A4.
When necessary, the trace is blanked by this signal ZIN, which is the final outcome of a number of different blanking situations occurring in this instrument. Signal ZIN is amplified by the stage incorporating transistors V1547 and V1553. Transistor V1553 acts as a constant-current source. At the output of this amplifier the a.c. and d.c. components of the blanking signal are routed along different paths.
The a.c. path is via blocking capacitor C1518 directly to the Wehnelt cylinder of the c.r.t. The d.c. component of the signal is fed to the emitters of V1541 and V1537 via a low-pass T-filter, R1571, C1555 and R1569.

The signal is modulated by a frequency of 156 kHz applied to V1541 via diode V1552. The resulting a.c. voltage on the collector of V1537 has a peak-to-peak value that depends on the output voltage of the low-pass filter.

The a.c. collector voltage of V1537 is applied via a symmetrical emitter-follower V1526, V1533 to a peak detector. This peak detector (C1522, V1517, V1516, R1518 and C1516) rectifies the a.c. voltage. Finally, this rectified voltage is added to the cathode voltage and applied to the Wehnelt cylinder G1.

The signal is split into its a.c. and d.c. components in order to isolate the cathode and Wehnelt cylinder, which stand at –1500 V, from the other circuits.

Adjustment of the black level is achieved by potentiometer R1589 in the emitter circuit of V1537 in the d.c. amplifier.

At pin 3 of D2023 the X OUT signal is available.
This signal may be:
– with no DOT-JOIN facility, a staircase voltage.
– with DOT-JOIN facility, a staircase voltage with a sawtooth voltage on every stair.

6.2.20.2. Y-Position Control System

In the two modes Yx1 and Yx5, a different method of position control is employed for each.

Yx1 mode

In this mode, two different voltages are added to the signal at the summing point (D2001-2):
– A preset voltage for position determination of the displayed memories on the c.r.t. screen.
– An adjustable voltage to position the displayed memories on the screen.

The preset voltage is selected by multiplexer D2012 output 13 and applied to the summing point via D2008 and buffer amplifier D2002 (5.6.7).

The selection of the corresponding memory is controlled by the $\overline{\text{OER}\emptyset}$ ... $\overline{\text{OER2}}$ signals generated on RAM unit A6.
The adjustable voltage is selected by multiplexer D2012 output 3 and applied to the summing point via buffer amplifier D2002 (1,2,3).

The Y*OUT signal is applied via D2008 output 12 and R2036 to the summing point if YEX is 0, as is the case in the Yx1 mode.

Yx5 mode

The preset voltage must not be added in the Yx5 mode, since the base-line of all displayed memories is now situated on the centre-line of the c.r.t. screen (Y POS controls at mid-range position). Multiplexer D2008 is switched by signal YEX = 1 so that the output on pin 15 is connected to earth. This means that no additional voltage is applied to the summing point.

Moreover, the Y*OUT signal is applied to the summing point via resistors R2027 and R2023 in series. The value of these resistors is only one-fifth of R2036, so a 5 times magnified signal is applied to the summing point.

6.2.20.3. Final Y Amplifier

The output of the summing amplifier D2001 (2,3,6) is applied to the differential amplifier V2001 and V2021. The constant emitter current is derived from the current source V2028 and its associated components. Variation in the collector current results in a control voltage for V2006 and V2013, which produces output signals Y2 and Y1 to drive the c.r.t. deflection plates.

6.2.20.4. Final X Amplifier

To obtain the possibility of magnification in the X direction, integrated circuit D2023 is used. This circuit comprises a Darlington pair input stage to obtain a symmetrical signal; a buffer stage and a continuous gain adjustment facility for X magnnification and for X gain.

The final stage functions in a similar way to that of the final Y stage.

6.2.20.5. CAL circuit

The lower part of multiplexer D2008 is controlled by a frequency of 2.5 kHz, derived from the microprocessor crystal frequency of 5 MHz by dividers on the time-base unit.

Input 3 of D2003 is switched between pins 3 and 5 of D2008, i.e. between 1 V and 0 V. Amplifier D2003 serves as a follower circuit with an output of 3 V, adjustable by means of R2017.

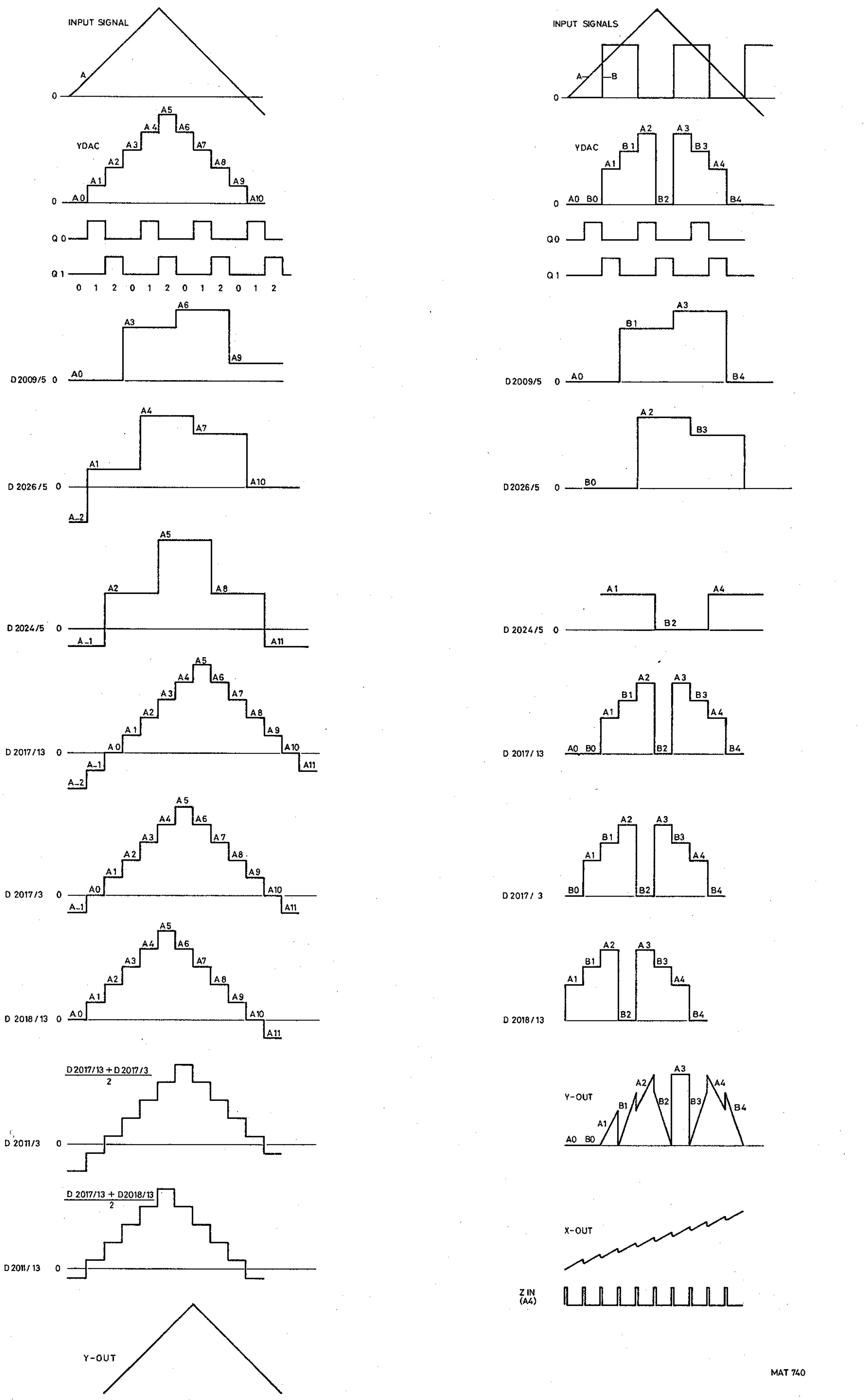

INPUT SIGNAL
YDAC
Q 0
Q 1
D 2009/5
D 2026/5
D 2024/5
D 2017/13
D 2017/3
D 2018/13
D 2017/13 + D 2017/3
2
D 2011/3
D 2017/13 + D2018/13
2
D 2011/13
Y-OUT
INPUT SIGNALS
X-OUT
Z IN
(A4)
MAT 740

Fig. 6.2.69.

INCOMING SIGNAL	OUTGOING SIGNAL	GENERATED ON UNIT	USED ON UNIT	DESCRIPTION
AØ-1-2		A4		Address bits from system address bus
ACON		A202		Slider of channel A continuous control
BCON		A202		Slider of channel B continuous control
CHOP		A9		Chopper signal
DØ ... D7		A4		Data bits from system data bus
	DØ ... D7	A21	A4	Data bits to system data bus
DAC M-1		A7		DAC M-1 output signal
	DRS	A21	A10	Signal information in D-R and S mode
ERUN		A22		Enable run signal
$\overline{\text{IOØ}}$		A4		I/O address decoding signal
NULIN		A9		Signal to switch vert. ampl. input to zero
OFFA		A202		Slider of channel A OFFSET control
OFFB		A202		Slider of channel B OFFSET control
P		A12		P-mode signal
	PAMPOUT1	A21	A11	Output signal for P^2CCD
	PAMPOUT2	A21	A11	Output signal for P^2CCD
$\overline{\text{RD}}$		A4		Signal READ from microprocessor
$\overline{\text{RECURR}}$		A22		Signal from RECURR switch
$\overline{\text{ROLL}}$		A22		Signal from ROLL switch
$\overline{\text{RUN}}$		A22		Signal from R/S-RESET switch
$\overline{\text{SINGLE}}$		A22		Signal from SINGLE switch
$\overline{\text{TANDH}}$		A22		Track and hold signal
$\overline{\text{WR}}$		A4		Signal WRITE from microprocessor
+6 V		A15		
–6 V		A15		
+12 V		A15		
–12 V		A15		
⏚		A15		

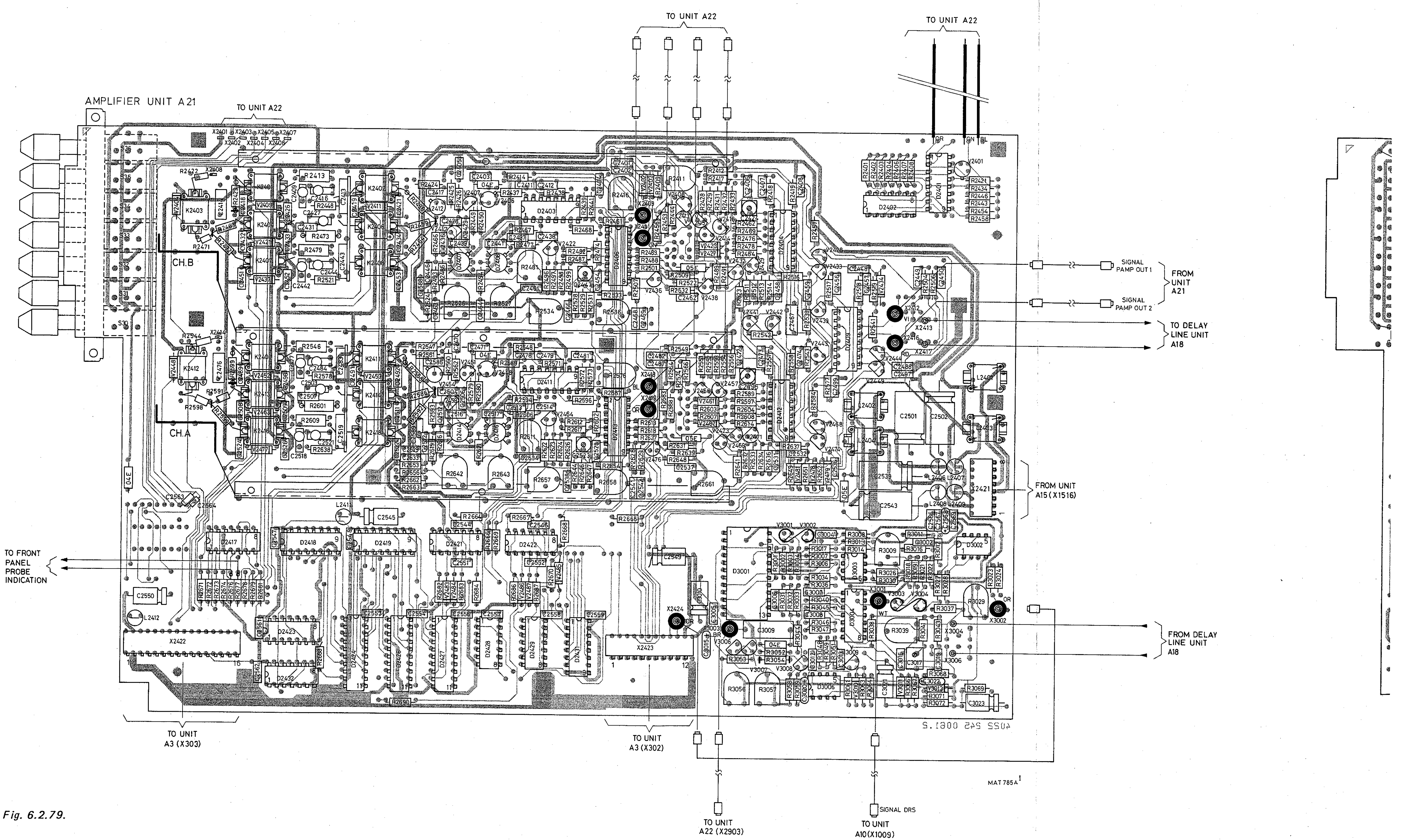
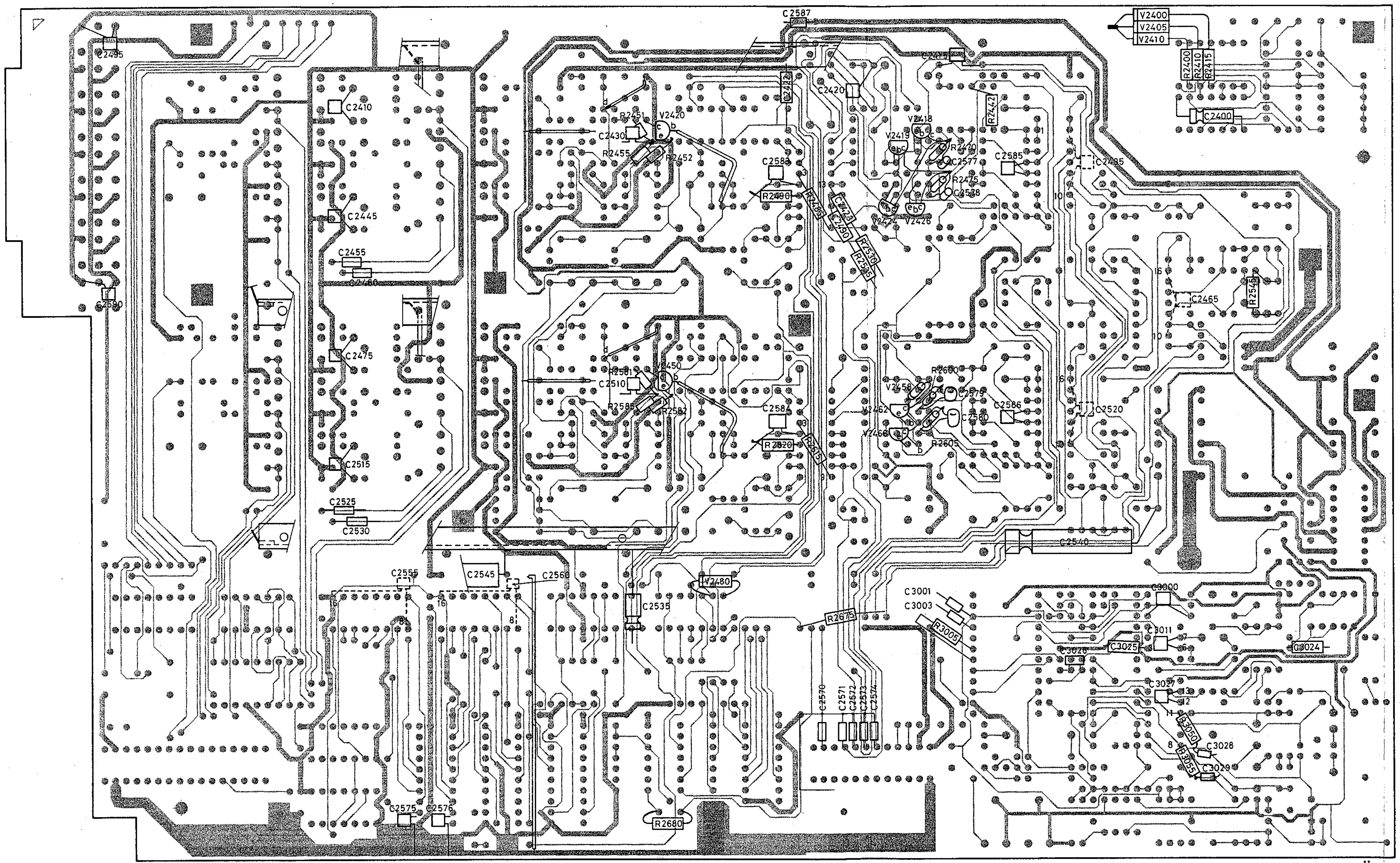
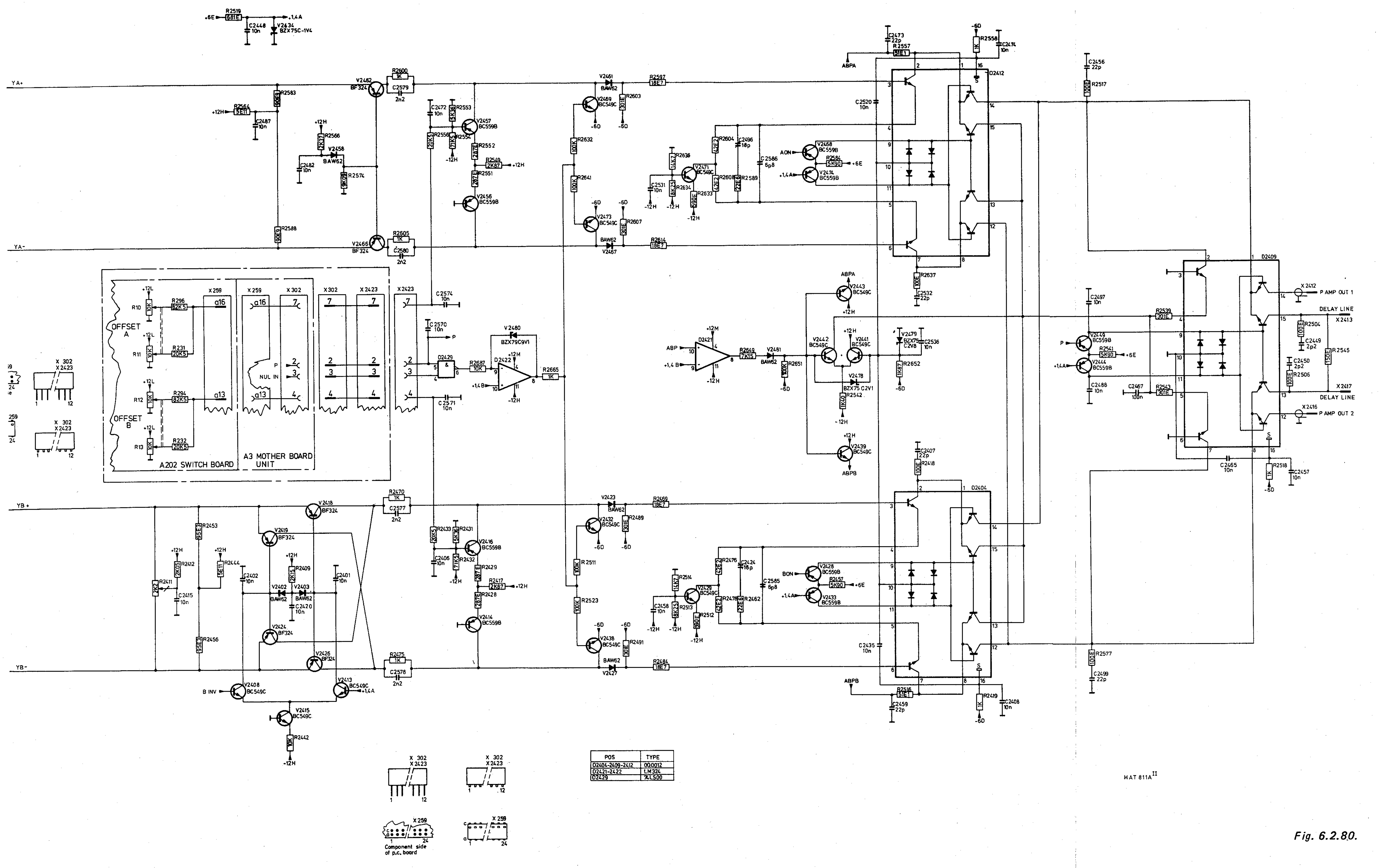

AMPLIFIER UNIT A21
TO UNIT A22
TO UNIT A22
TO UNIT A22
CH.B
CH.A
SIGNAL PAMP OUT 1
SIGNAL PAMP OUT 2
FROM UNIT A21
TO DELAY LINE UNIT A18
FROM UNIT A15 (X1516)
TO FRONT PANEL PROBE INDICATION
FROM DELAY LINE UNIT A18
TO UNIT A3 (X303)
TO UNIT A3 (X302)
TO UNIT A22 (X2903)
SIGNAL DRS
TO UNIT A10 (X1009)
MAT 785A

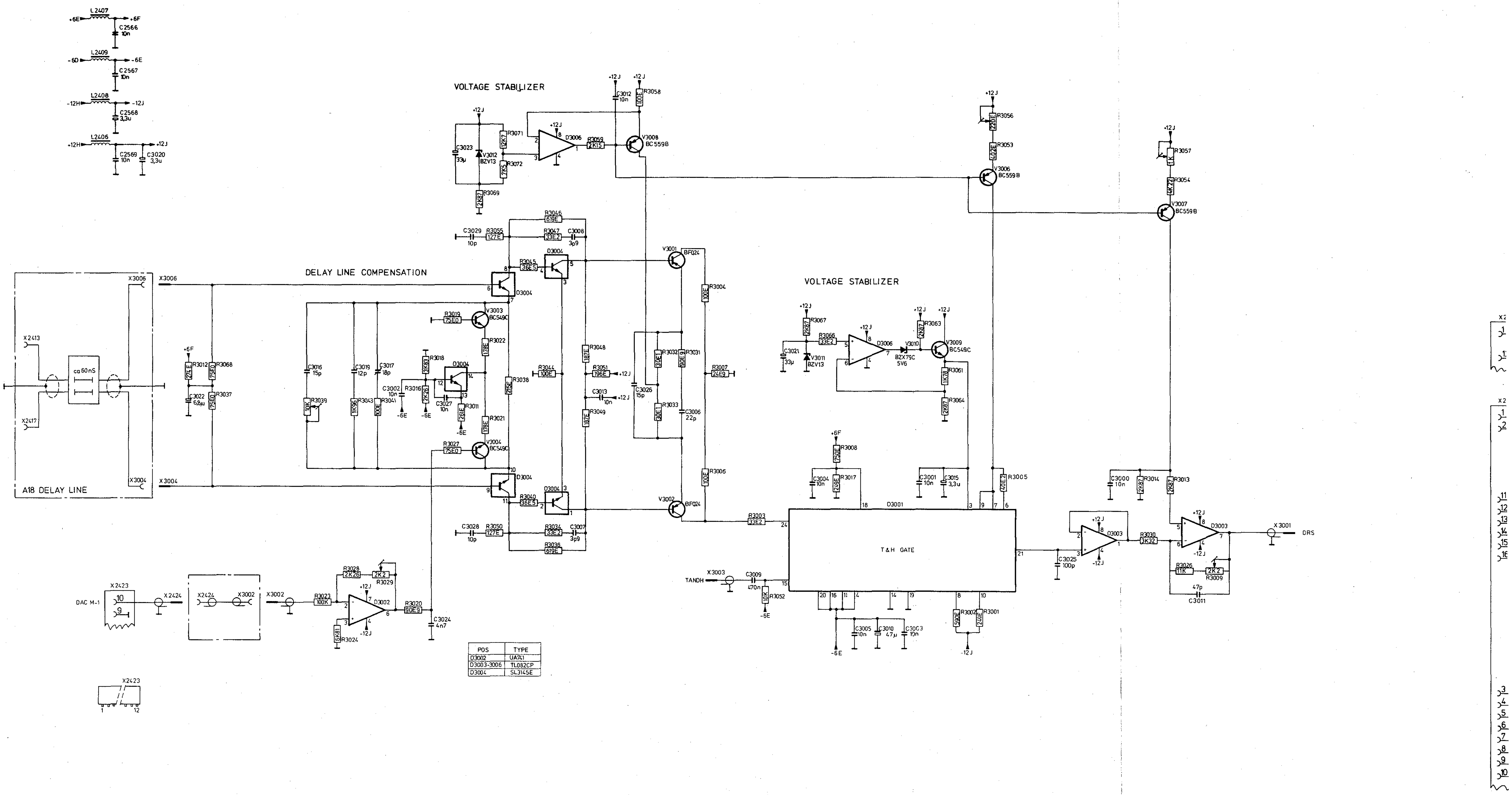
Fig. 6.2.79.


C2587
V2400
V2405
V2410
R2400
R2410
R2415
C2400
C2495
C2410
C2445
C2455
C2460
C2590
C2475
C2515
C2525
C2530
C2420
R2451
V2420
C2430
R2455
R2452
C2583
R2480
V2418
V2419
R2470
C2577
C2585
C2485
R2475
C2578
V2426
R2442
C2465
R2546
R2581
C2510
R2585
R2582
C2584
R2620
R2600
V2456
C2579
C2580
V2462
V2466
R2605
C2586
C2520
C2540
C2555
C2545
C2560
C2535
V2480
C3001
C3003
R3005
R2675
C3000
C3011
C3025
C3026
C3024
C3027
C3028
C3029
C2570
C2571
C2572
C2573
C2574
C2575
C2576
R2680
MAT785A



POS	TYPE
D2404-2409-2412	OQ0012
D2421-2422	LM324
D2429	74LS00

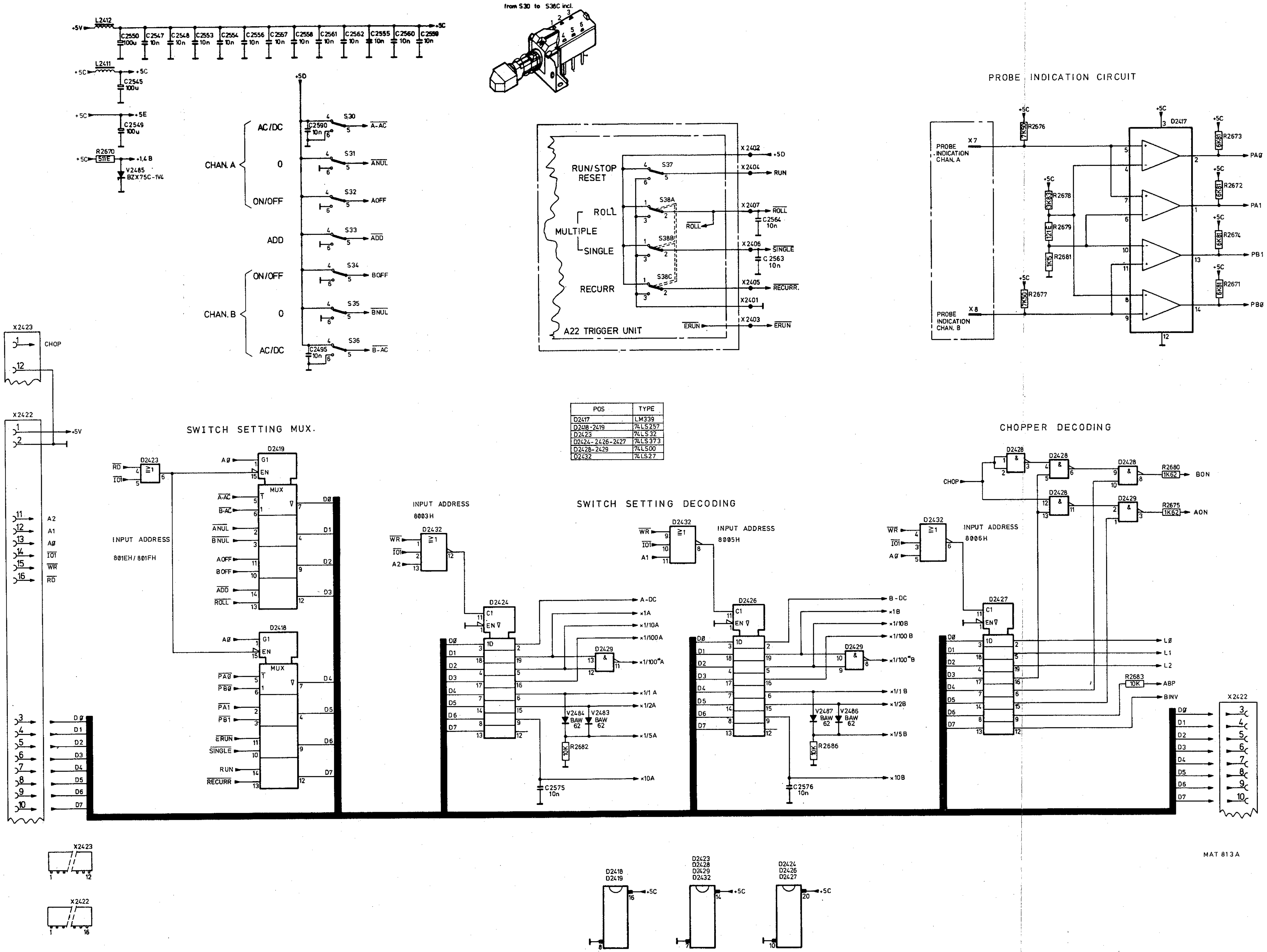
Fig. 6.2.80.



POS	TYPE
D3002	UA741
D3003-3006	TL082CP
D3004	SL3145E

MAT 812A

Fig. 6.2.81.



POS	TYPE
D2417	LM339
D2418-2419	74LS257
D2423	74LS32
D2424-2426-2427	74LS373
D2428-2429	74LS00
D2432	74LS27

Fig. 6.2.82.

6.2.22. Trigger unit A22

The trigger unit comprises the following circuits:

- Trigger source switching circuit
- AC-DC coupling
- Peak-peak detector
- Level circuit
- Slope circuit
- TV circuit
- Pulse stretcher
- Time-base slow circuit
- Sampling circuit

6.2.22.1. Trigger source switching circuit

The trigger source switching circuit serves to detect the selected trigger source, the various possibilities being:

- channel A
- channel B
- LINE
- EXTERN
- EXTERN ÷ 10

With no pushbutton depressed, channel A is automatically chosen. Transistor V2723 provides this facility.
If all pushbuttons are released, the base of V2723 is connected to zero, which causes the transistor to block.
In turn, transistors V2746 and V2747 are blocked and therefore the signal of channel A is enabled.
In all other positions of the switches, except for CHAN A switch, V2723 is conductive and the channel A signal flows via V2746 and V2747 to the –6 V supply line, i.e. it is blocked.

In single or recurrent operation, two modes of external triggering are possible: EXT and EXT ÷ 10.
In the EXT ÷ 10 mode, the input signal is attenuated by a factor of 10 and applied to the amplifier. The h.f. path of the amplifier is via C2708 and V2701 to V2702; the l.f. path is a.c.-coupled via C2719 and D2708 to V2702, and d.c.-coupled via D2709 (13, 14) and D2708 to V2702.

In the roll-mode the function of the external input is a RUN/STOP action at TTL-level. This is a software OR-function together with the position of the R/S switch. A high level at the input is applied to V2727 via D2709 and D2708, V2702, V2707. This causes the ERUN signal to go high, which then starts the ROLL-mode via the software program if the R/S switch is at STOP.

6.2.22.2. AC-DC coupling

The trigger signal is routed to V2724 and V2729 via the AC-DC coupling circuit.
If the d.c. signal is high, the reed relay K2701 switches off and the signal is applied to the bases of V2724 and V2729 via R2789, R2788 and R2792, R2791 respectively. If the d.c. signal is low, the reed relay is energised and the d.c. component in the trigger signal is filtered out, the a.c. component flowing through C2737 and C2743. The signal is applied via an amplifier stage to the input of the slope circuit and the input of the peak-peak detector.

6.2.22.3. Peak-peak detector

A peak-to-peak detector is introduced to enable the possibility of levelling between the positive and negative peaks of the signal in the AUTO mode.
The positive peak flows via the base-emitter diode of D2703 (6, 7, 8), to charge electrolytic capacitor C2709.
The current required to drive D2703 (9, 10, 11) is obtained from D2704 (5, 6, 7). The output of this amplifier is the d.c. level proportional to the positive peak.
The negative peak flows via the emitter-collector diode of D2703 (1, 2, 3) to charge C2711. This peak voltage is amplified by D2704 (1, 2, 3) to give an output d.c. level proportional to the negative peak.

6.2.22.4. Level circuit

The level potentiometer is connected to the outputs of a multiplexer D2701.
Depending on the signals TV and OH, the level potentiometer is connected to:

MODE	D2701 OUTPUTS 13	3	TV	OH
AUTO	postop	negtop	0	0
DCor AC	d.c.	d.c.	0	1
TV +	postop	postop	1	0
TV –	negtop	negtop	1	1

6.2.22.5. Slope circuit

The trigger signal is applied to the differential amplifier in D2711.
The output of the level circuit is applied to the other input.
Depending on the position of the slope switch, either V2732 or V2751 conducts, which causes the positive or negative signal to be connected to the outputs of D2711. The trigger signal is applied via an electronic switch V2761 and its associated components to ECL-Schmitt trigger D2907 (2, 3, 4, 5).

6.2.22.6. TV circuit

The outputs 12 and 13 of D2711 are applied to the video clipper consisting of V2717 and its components. The TV trigger signal is now applied to two re-triggerable monostable one-shots (D2702) in series, with different pulse times. The output of the first one-shot is applied to the clock input of D-flip-flop D2707. This flip-flop is enabled by the TV signal. At output 9 of D2707 a 50 Hz field pulse is available. To obtain frame pulses, the inverting output 8 of D2707 is applied to clock input 3. At the D input 2, the output of the second one-shot is applied. The frame pulse now appears at the inverting output 5 of D2707.
Normal triggering is now inhibited because of the TV signal applied to the electronic switch V2761, which causes the voltage at X2708 to go low.

6.2.22.7. Pulse stretcher

The trigger pulse is applied via the ECL-Schmitt trigger to the clock input of the dual ECL D-flip-flop D2904.

This flip-flop in combination with two Schmitt trigger circuits D2907 (9, 10, 6, 7), D2907 (12, 13, 14, 15) form the pulse stretcher.
The principle is shown in the following diagram.

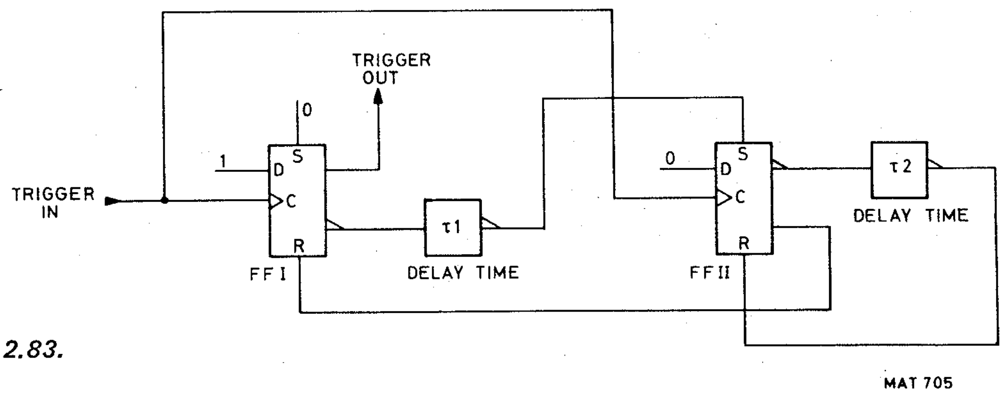


Fig. 6.2.83.

On receipt of a trigger pulse at the clock input of FFI, its inverted output goes low. After time t_1, this output is applied as a logic high signal, which sets FFII. Consequently, its inverted output goes low and the non-inverting output goes high. This results in a reset of FFI. After t_2, FFII is reset and, as a result, FFI is enabled.

Times t_1 and t_2 are chosen so that the pulse stretcher acts as a pulse-shaper at frequencies up to 2 kHz, as a divide-by-two circuit from 2 kHz to 10 kHz, and as a divider by n for frequencies above 10 kHz.

6.2.22.8. Time-base slow circuit

The output of the pulse stretcher is converted to TTL-level by the two converters D2906. The upper converter produces the TRIST signal which is applied to the delayed trigger unit A13. In the sampling mode, the lower converter can feed the trigger signal to the sampling system.

In the Direct and Roll-modes, the system is operated by the TBS signal. This signal is fed via inverter D2911 (5, 6) and NAND-gate D2912 (11, 12, 13) to the clock input 11 of D-flip-flop D2909. At the inverted output 8, a low level is clocked, which is the STOP signal. This STOP signal is applied to multiplexer D2908 and via the inverted output and diode V2919 to the wired-OR gate (D2911-13). Pin 12 of D2911 goes low and via the upper NAND-gate of D2902 a Track and Hold (TANDH) pulse is generated.

The lower NAND-gate of D2902 is controlled by the TANDH pulse via D2903 (13, 11) and inverter D2911 (1, 2) and generates a HONCONDRS pulse. At the same moment, a TANDH pulse is taken over by a high level at output 8 of D2903.

The HOCONDRS pulse goes high after 3.6 µs caused by the RC combination R2928 and C2918, C2919. After approximately 0.4 µs, output 8 of D2903 goes low and therefore the HOCONDRS pulse again becomes low.

6.2.22.9. The sampling circuit

If the oscilloscope is in the sampling mode, the output of the pulse stretcher is applied to the clock input 11 of D2909. This flip-flop is enabled by a high level on reset input 13, and its inverted output blocks transistors V2916 and V2913.
Sawtooth capacitor C2923 starts charging with a current derived from the current source V2922. The current that feeds the fast ramp sawtooth generator is determined by the settings of the time-base switch. These settings are decoded by the microprocessor system and applied to a FET-switch array D2401 and FET V2401, via D2402. The following table shows the relationship between the time-base settings and the current-source control FETs.

	D2431					D2431		
	4	5	11	6	7	2 LØ	3 L1	1 L2
5 ns/cm	1	1	0	1	1	0	1	1
10 ns/cm	1	0	1	1	1	1	0	0
20 ns/cm	1	1	1	0	1	0	1	0
50 ns/cm	1	1	1	1	0	1	1	0
.1 µs/cm	0	1	1	1	1	0	0	0
.2 µs/cm	1	1	1	1	1	1	1	1

Except for the .2µ/div, one control line is always low. This means that one of the resistors R2421, R2443, R2446, R2454 and R2458 is switched in parallel with the current-determining resistor R2434. The value of the resistors is determined so that in the 5 ns/cm position the highest current is obtained.
The fast ramp sawtooth voltage is applied to the positive input of comparator D2902 (11, 12). To the negative input, a preset voltage built-up from DACSTAIR and DACDEL is applied. If the last ramp reaches the potential of the preset voltage, the comparator output goes low and the triple-NAND gate goes high for 4 µs (described under time-base slow).
The sawtooth voltage is blocked and the capacitor is discharged by a reset pulse derived from the TANDH pulse at D2909-13, so output 8 goes high.
The flip-flop is enabled to start a new sawtooth ramp if the TANDH signal is low and TRACK is high.
The DACSTAIR signal is generated at the ACL unit and is divided into 256 steps, each of 40 mV. The DACDEL signal is generated on the delayed time-base unit and is divided into 200 steps, each of 40 mV. This means that each division delay corresponds to two steps (i.e. 80 mV). The resistor network R2910, R2913, R2914 is chosen so that 256 steps of DACSTAIR generate the same potential as 20 steps of DACDEL at input 6 of D2901.
If no sampling mode is chosen, the TANDH signal is not generated by means of the sawtooth generator and the comparator, but via the system described under time-base slow. This is effected by presetting the negative input 11 of the comparator to a high voltage via D2901.

INCOMING SIGNAL	OUTGOING SIGNAL	GENERATED ON UNIT	USED ON UNIT	DESCRIPTION
	AUTO TB	A22	A13	Auto signal from AUTO switch
DAC DEL		A13		Output signal of DAC delay
DAC STAIR		A9		Output signal of DAC STAIR
	ERUN	A22	A21	Enable run signal
FRUN		A13		Freerun signal
	HOCONDRS	A22	A9	Hold and convert signal in D-R and S-mode
LINE		A15		Signal for mains triggering
S		A12		S-mode signal
	TANDH	A22	A21	Track and hold signal
TBS		A12		Time-base slow
TRACK		A9		Track command for S/H circuit
	TRIST	A22	A13	Trigger signal for strecher
+5V		A15		
−5.2V		A15		
+6V		A15		
−6V		A15		
+12V		A15		
−12V		A15		
+40V		A15		
⏚		A15		

TEST POINTS	
X2700	External trigger
X2707	TRIGGER SIGNAL
X2708	TRIG.
X2905	HOCONDRS

6.2.23. EHT unit A23

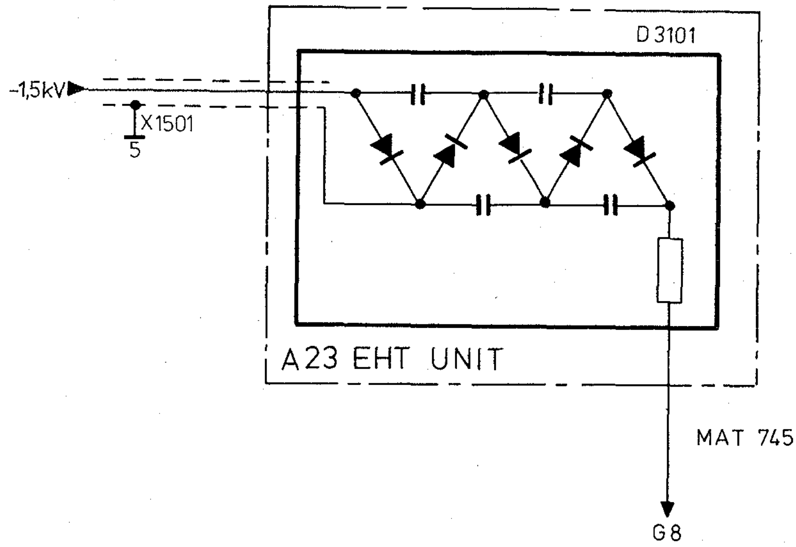


Fig. 6.2.86

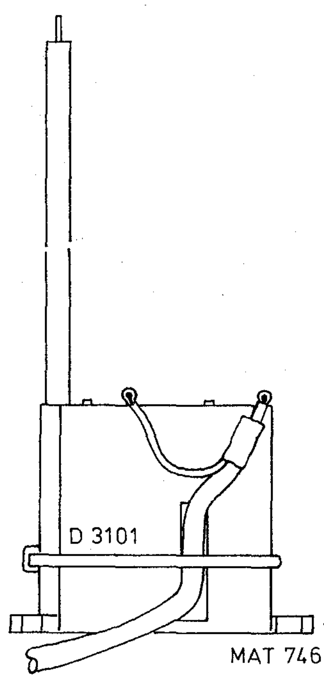


Fig. 6.2.87

7. DISMANTLING THE INSTRUMENT

7.1. WARNINGS

WARNING: The opening of covers or removal of parts, except those to which access can be gained by hand, is likely to expose live parts, and also accessible terminals may be live.
The instrument shall be disconnected from all voltage sources before any adjustment, replacement or maintenance and repair during which the instrument will be opened.
If afterwards any adjustment, maintenance or repair of the opened instrument under voltage is inevitable, it shall be carried out only by a skilled person who is aware of the hazard involved.
Bear in mind that capacitors inside the instrument may still be charged even if the instrument has been separated from all voltage sources.

ATTENTION: This section provides the dismantling procedures required for the removal of components during repair operations. All circuit boards removed from the oscilloscope should be adequately protected against damage, and all normal precautions regarding the use of tools must be observed. During dismantling procedures, a careful note must be made of all disconnected leads that they may be reconnected to their correct terminals during assembly. Damage may result if the instrument is switched on when a circuit board has removed, or if a circuit board is removed within one minute after switching off the instrument.

WARNING: The E.H.T. cable is unbreakably connected to the E.H.T. unit (disconnection at C.R.T.). When the E.H.T. cable to the post-acceleration anode of the C.R.T. is disconnected at the C.R.T. unit end, the E.H.T. cable must be discharged immediately by shortening them to earth.

7.2. REMOVING THE COVERS

To remove the instrument covers, proceed as follows:

- Both upper and lower cabinet plates can be removed after slackening the four quick-release fasteners at the corners of each plate. To prevent the fasteners coming apart, do not slacken more than two turns.

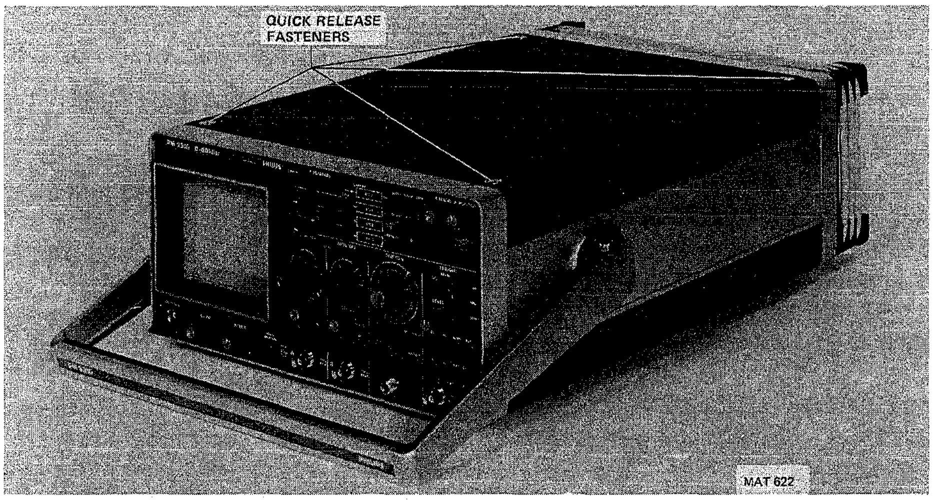


Fig. 7.2.1. Removing the instrument covers.

7.3. ACCESS TO PARTS FOR CHECKING AND ADJUSTING PROCEDURE

Adjusting elements are accessible after removing the instrument covers.
Only for measurements and adjustments on the AC POWER unit A16 and DC POWER unit A15 the rear panel has to be removed.

Remove the six screws that secure the rear panel to the instrument

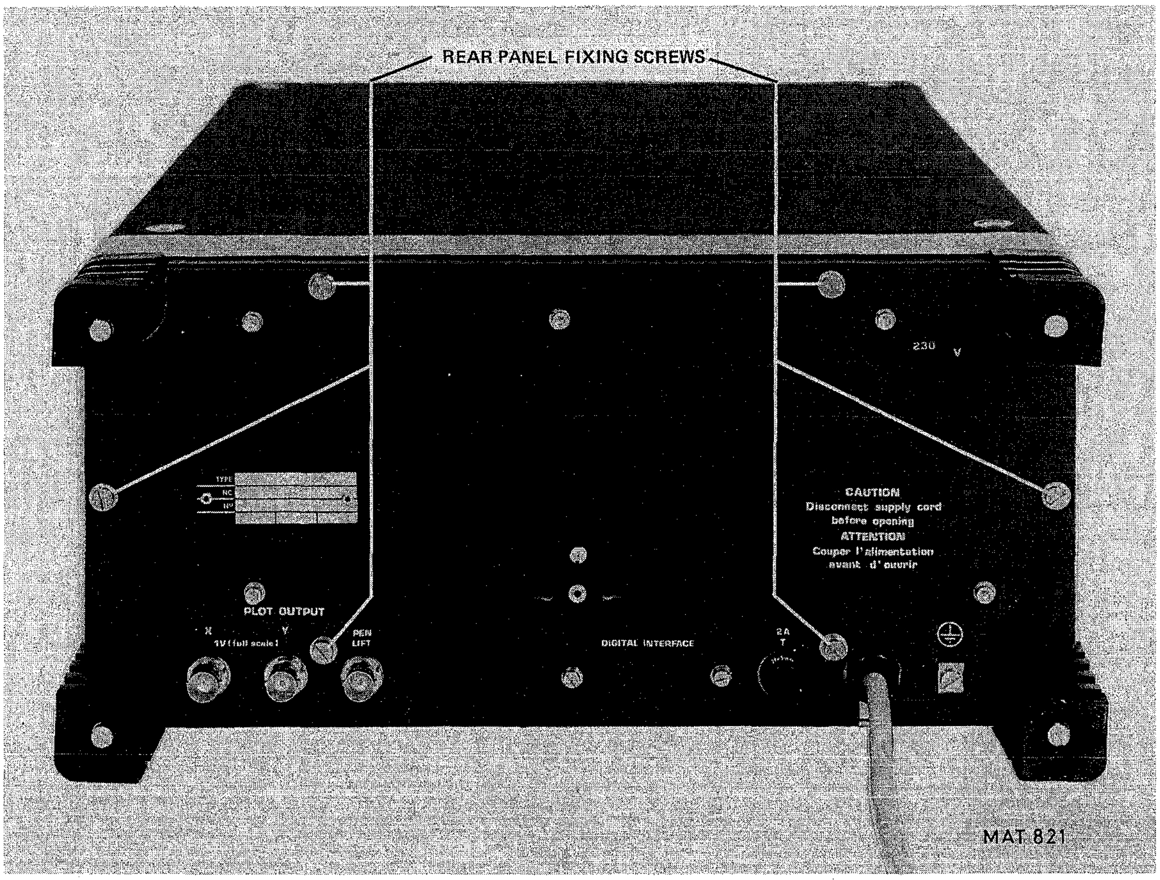


Fig. 7.2.2.

Unit A16 which is mounted on the rear panel can be placed outside the instrument by pulling the rear panel.

For better access to unit A15 both the upper and lower screening plates can be removed.

8. CHECKING AND ADJUSTING

WARNING: The opening of covers or removal of parts, except those to which access can be gained by hand, is likely to expose live parts, and also accessible terminals may be live.
The instrument shall be disconnected from all voltage sources before any adjustment, replacement or maintenance and repair during which the instrument will be opened.
If afterwards any adjustment, maintenance or repair of the opened instrument under voltage is inevitable, it shall be carried out only by a skilled person who is aware of the hazard involved.
Bear in mind that capacitors inside the instrument may still be charged even if the instrument has been separated from all voltage sources.

8.1. GENERAL INFORMATION

The following information provides the complete checking and adjusting procedure for the oscilloscope. As various control functions are interdependent, a certain order of adjustment is often necessary.
The procedure is, therefore, presented in a sequence which is best suited to this order, cross-reference being made to any circuit which may affect a particular adjustment.
Before any check or adjustment, the instrument must attain its normal operating temperature.

- Where possible, instrument performance is checked before an adjustment is made.
- Warming-up time under average conditions is 30 minutes.
- All limits and tolerances given in this section are calibration guides and should not be interpreted as instrument specifications unless they are also published in chapter 1.2. characteristics.
- Tolerances given are for the instrument under test and do not include test equipment error.
- The most accurate display adjustments are made with a stable, well-focused, low-intensity display. Unless otherwise noted, adjust the Intensity, Astigmatism, Focus and Trigger Level controls as needed.

8.1.1. Recommended test equipment

Type of instrument	*Specifications*	*Used for*	*Example of recommended instrument*
1. Constant amplitude sine-wave generator	Freq. 200 kHz ... 60 MHz Constant amplitude of 12 mVp-p ... 1.2 Vp-p	Bandwidth check of vertical channels and triggering	Tektronix SG 503 + SG 504
2. Time marker generator	Repetition rate 0.5 s ... 20 ns	Checking and adjusting of sweep rates	Tektronix TG 501
3. Square-wave calibration generator	Rise time ⩽ 200 ns Voltage 10 mV up to (for preference) 30 V Duty cycle 50 % Rise time ⩽ 1 nsec.	Checking and adjusting of square-wave response of vertical channels and triggering	Generator with additional attenuator unit. Partly PG506
4. L.F. sine-wave/square-wave generator	Sine-wave: 1 Hz ... 1 MHz/0 ... 30 V Square-wave: 1 Hz ... 1 MHz/0 ... 30 V Rise time ⩽ 100 ns	Checking the trigger sensitivity Checking and adjusting square-wave response of for instance attenuator unit	PM 5129
5. Cables, T-piece, terminations for the generators	General Radio types for fast rise-time square-wave and high frequency sine-wave. BNC-types for other applications.	See points 1 and 3 See points 2 and 4.	
6. Dummy probe 2 : 1	1 MΩ ± 0.1 % // 25 pF	Adjustment of input capacitance.	
7. Trimming tool kit		Adjustments	PHILIPS 800 NTX - 4822 310 50015
8. Variable mains transformer	Well-insulated output voltage 90 ... 264 Va.c.	Checking influence of mains voltage variations and adjustment of power supply.	PHILIPS ord. number 2422 529 00005
9. Moving-iron meter		Checking the power consumption of the instrument.	
10. Oscilloscope	The bandwidth must be the same or higher than the bandwidth of the instrument under test.	Various measurements.	PM 3262 PHILIPS
11. Digital multimeter	Wide voltage, current and resistance ranges. Required accuracy 0.1 %.	Checking the instrument under test.	PHILIPS PM 2527

8.1.2. Preliminary settings

- **No** input signals connected.
- All pushbuttons released and all switches in the CAL position.

A trace will now appear within the upper two divisions of the screen.

Clear all the four memories ACCU - STO1 - STO2 and STO3.

8.2. SURVEY OF ADJUSTING ELEMENTS AND AUXILIARY EQUIPMENT

ADJUSTMENT	ADJUSTING ELEMENT + UNIT	ADJUSTING RESULT OR CHECK RESULT	RECOMMENDED INPUT SIGNALS	EXAMPLE OF MEASURING INSTRUMENT	CHAPTER
POWER SUPPLY					8.3.1.
Power consumption	–	Current consumption ≤ 300 mA at 220 V local mains	–	–	8.3.1.
+12 V supply voltage	R1646 – (A16)	+12.6 V ± 1 %	–	PM 2517 or PM 2527	8.3.1.
+5 V supply voltage	–	+5 V ± 0.25 V	–	PM 2517 or PM 2527	8.3.1.
+12 V supply voltage	–	Vary mains voltage between 200 V and 265 V. Check +12 V output (+ or – 60 mV).	–	PM 2517 or PM 2527	8.3.1.
Oscillator frequency	R1647 – (A16)	Set mains voltage to 180 V. Check +12 V output for ripple ≤ 10 mV.	–	PM 3262	8.3.1.
C.R.T. CIRCUIT					8.3.2.
Cathode voltage	R1591 – (A15)	–1.5 V on test point X1502	–	PM 2517 or PM 2527	8.3.2.
Intensity	R1589 – (A15)	Trace just not visible	–	–	8.3.2.
Focus and Astigmatism	R1588 – (A15)	in its mid position	Sine-wave signal of 240 mVp-p – 2 kHz to X4	PM 5129	8.3.2.
	R1506 – (A15)	Sharp and well-defined trace	–	–	8.3.2.
	R1587 – (A15)	Sharp and well-defined trace	–	–	8.3.2.
Trace rotation	R16 – (front)	Horizontal trace	–	–	8.3.2.
PRE ADJUSTMENT P²CCD CIRCUIT					8.3.3.
Pre-settings	R1002 – (A10)	Set these potentiometers as indicated on unit A10		PM 2517 or PM 2527	8.3.3.
	R1006 – (A10)			PM 2517 or PM 2527	8.3.3.
	R1007 – (A10)			PM 2517 or PM 2527	8.3.3.
	R1008 – (A10)			PM 2517 or PM 2527	8.3.3.
	R1024 – (A10)			PM 2517 or PM 2527	8.3.3.
	R1026 – (A10)			PM 2517 or PM 2527	8.3.3.
	R1027 – (A10)			PM 2517 or PM 2527	8.3.3.
	R1080 – (A10)			PM 2517 or PM 2527	8.3.3.
	R1101 – (A11)			PM 2517 or PM 2527	8.3.3.
	R1102 – (A11)			PM 2517 or PM 2527	8.3.3.
	L1102 – (A11)			PM 2517 or PM 2527	8.3.3.
	L1103 – (A11)			PM 2517 or PM 2527	8.3.3.
	L1104 – (A11)			PM 2517 or PM 2527	8.3.3.
	L1106 – (A11)			PM 2517 or PM 2527	8.3.3.
	R3057 – (A21)	Minimum trace jump when switching 0.2 ms/div to 0.5 ms/div	–	–	8.3.3.
BALANCE ADJUSTMENTS					8.3.4.
Vertical amplifier balances					8.3.4.1.
0-DC balance	CH.A – R2642 – (A21) CH.B – R2526 – (A21)	Minimum trace jump when switching 0-DC	–	–	8.3.4.1.
Attenuator balance	CH.A – R2643 – (A21) CH.B – R2527 – (A21)	Minimum trace jump when switching between 10 mV/ div – 20 mV/div – 50 mV/div	–	–	8.3.4.1.
X1/X10 balance	CH.A – R2657 – (A21) CH.B – R2534 – (A21)	Minimum trace jump when switching between 50 mV/div and 0.1 V/div	–	–	8.3.4.1.
Continue balance	CH.A – R2576 – (A21) Ch.B – R2416 – (A21)	Minimum trace shift when turning the continuous control	–	–	8.3.4.1.
Normal/Invert balance	CH.B – R2411 – (A21)	Minimum trace jump when switching Normal-Invert	–	–	8.3.4.1.
Trigger symmetry	R2819 – (A22)	Voltage on test point X2707= –1V	–	PM 2517 or PM 2527	8.3.4.2.
Trigger balances AC-DC					8.3.4.3.
External	R2753 – (A22)	No movement of trigger point when switching AC-DC	Sine-wave signal of 1,2 V p.p 2 kHz.	PM 5129	8.3.4.3.
A balance	R2861 – (A22)	No movement of trigger point when switching AC-DC	Sine-wave signal of 1,2 V p.p 2 kHz	PM 5129	8.3.4.3.
B balance	R2859 – (A22)	No movement of trigger point when switching AC-DC	Sine-wave signal of 1,2 V p.p 2 kHz	PM 5129	8.3.4.3.
LINE balance	R2857 – (A22)	No movement of trigger point when switching AC-DC	Sine-wave signal of 1,2 V p.p 2 kHz	PM 5129	8.3.4.3.
Trigger amplifier balance	R2867 – (A22)	Trigger point in middle of signal amplitude	Sine-wave signal of 1,2 V p.p 2kHz	PM 5129	8.3.4.4.

ADJUSTMENT	ADJUSTING ELEMENT + UNIT	ADJUSTING RESULT OR CHECK RESULT	RECOMMENDED INPUT SIGNALS	EXAMPLE OF MEASURING INSTRUMENT	CHAPTER
FINAL AMPLIFIER ADJUSTMENTS					8.3.5.
Vertical trace height	R2008 – (A20)	Display is blinking at + 4 divisions	Sine-wave signal to X3	PM 5129	8.3.5.
Display positions ACCU-STO1-STO2-STO3	R2009 – (A20)	Distance of two divisions between the traces	–	–	8.3.5.
Invert registers	–	STO1 – STO2 – STO3 are inverted	Sine-wave signal to X3	PM 5129	8.3.5.
Horizontal trace length	R2011 – (A20)	Horizontal trace length of 10 divisions	–	–	8.3.5.
Dot join adjustments	R2019 – (A20)	Equal vertical dot join faults on positive and negative going edge of the signal	Sine-wave signal of 10 divisions 2 kHz	PM 5129	8.3.5.
	R2018 – (A20)	Eliminated dot join faults	Sine-wave signal of 10 divisions 2 kHz	PM 5129	8.3.5.
	R2072 – (A20)	Dots on the screen connected with each other	Sine-wave signal of 10 divisions 2 kHz	PM 5129	8.3.5.
	R2039 – (A20)	Minimum cross-talk between the channels	Sine-wave signal of 10 divisions 2 kHz	PM 5129	8.3.5.
CALibration voltage	R2017 – (A20)	3 V ± 0.7 % – 2.5 kHz	Oscilloscope and digital multimeter	PM 3262 – PM 2527	8.3.5.
VERTICAL CHANNELS					8.3.6.
Vertical amplifier sensitivity adjustments					8.3.6.1.
Channel B gain x1	R3029 – (A21)	Trace height of 6 DIV	Square-wave signal of 240 mVp-p – 2 kHz to X4	PM 5129	8.3.6.1.
Channel A gain x1	R2661 – (A21)	Trace height of 6 DIV	Square-wave signal of 240 mVp-p – 2 kHz to X3	PM 5129	8.3.6.1.
Channel A gain x10	R2658 – (A21)	Trace height of 6 DIV	Square-wave signal of 24 mVp-p – 2 kHz to X3	PM 5129	8.3.6.1.
Channel B gain x10	R2536 – (A21)	Trace height of 6 DIV	Square-wave signal of 24 mVp-p – 2 kHz to X4	PM 5129	8.3.6.1.
Channel A L.F. corr.	R2611 – (A21)	Straight pulse top	Square-wave signal of 240 mVp-p – 100 Hz to X3	PM 5129	8.3.6.1.
Channel B L.F. corr.	R2481 – (A21)	Straight pulse top	Square-wave signal of 240 mVp-p – 100 Hz to X4	PM 5129	8.3.6.1.
AC – DC channel A AC – DC channel B	– –	Pulse top difference > 0,5 div. Pulse top difference > 0,5 div.	Square-wave signal of 240 mVp-p – 100 Hz	PM 5129 PM 5129	8.3.6.1. 8.3.6.1.
Sampling loop gain	R3009 – (A21)	Straight pulse top	Square-wave signal of 240 mV p.p – 2 kHz to X3	PM 5129	8.3.6.1.
	R 3056 – (A21)	Pulse variations are symmetrical	Square-wave signal of 240 mVp-p – 2 kHz to X3	PM 5129	8.3.6.1.
	R3057 – (A21)	Line is in middle of the screen	–	–	8.3.6.1.
IF NECESSARY PRE-ADJUST P²CCD					
Input attenuators		Straight pulse top. Pulse top errors + or –4 % maximum	Square-wave signal with a rise time ⩽ 100 ns	PM 5129 2 : 1 Dummy probe 1 MHz // 25 pF	8.3.6.2.
	CH.A – CH.B	AMPL/DIV Switch — Trace-height	Amplitude and frequency		
	C2503 (C2427) C dummy	20 mV/div — 6 div ± 4 % 20 mV/div — 6 div ± 4 %	24 mV – 2 kHz 48 mV – 10 kHz (via dummy)		
	– –	0.2 V/div — 6 div ± 4 % 0.2 V/div — 6 div ± 4 %	240 mV – 2 kHz 480 mV – 10 kHz (via dummy)		
	C2521 (C2444) C2518 (C2442)	2 V/div — 6 div ± 4 % 2 V/div — 6 div ± 4 %	2.4 V – 2 kHz 4.8 V – 10 kHz (via dummy)		
	C2484 (C2416) C2477 (C2409)	20 V/div — 6 div ± 4 % 20 V/div — 6 div ± 4 %	24 V – 2 kHz 48 V – 10 kHz (via dummy)		

ADJUSTMENT	ADJUSTING ELEMENT + UNIT	ADJUSTING RESULT OR CHECK RESULT	RECOMMENDED INPUT SIGNALS	EXAMPLE OF MEASURING INSTRUMENT	CHAPTER
Square-wave response CH.A (CH.B). x1	R3039 - (A21) C3017 - (A21)	Pulse top errors may not exceed 1 subdivision	Square-wave signal of 1MHz - rise time ⩽ 1 ns to X3.	–	8.3.6.3.
	C2424	"	"	–	"
	C2447	"	"	–	"
	C2429	"	"	–	"
	C2523	"	"	–	"
Ch.A. square-wave response in ADD-mode	–	No change in square-wave response when operating the ADD push-button	"	–	8.3.6.3.
CH.B. square-wave response in ADD-mode	–	No change in square-wave response when operating the ADD push-button	"	–	8.3.6.3.
Square-wave response channel B - INVERT	–	No change in square-wave response when operating the PULL-FOR -B switch	"	–	8.3.6.3.
Bandwidth	–	Vertical deflection must be 6 divisions at 1 MHz input and 4,8 divisions minimum at 60 MHz.	Sine-wave signal of 12 mVp-p – 60 MHz	Tektronix SG 503 + SG 504	8.3.6.4.
OFFSET control range	–	Display can be shifted more than 15 divisions on both sides	Sine-wave signal of 1.2 Vp-p – 20 MHz	Tektronix SG 503 + SG 504	8.3.6.5.
Common mode rejection	–	Rejection factor better than 100	Sine-wave signal of 960 mVp-p – 2 MHz	Tektronix SG 503 + SG 504	8.3.6.6.
TIME COEFFICIENTS					8.3.7.
Recurrent-mode	R2958 (A22)	Correct 20 ns range	Time marker signal of 160 mV-pulse repetition rate of 20 nsec to X3	Tektronix TG 501	8.3.7.1.
	R2911 (A22)	Correct start point of the trace on the screen	Time marker signal of 160 mV-pulse repetition rate of 20 ns to X3	Tektronix TG 501	8.3.7.1.
ROLL-mode	–	Correct ROLL-mode in 0.5 s/div and 1 s/div	Time marker signal with a repetition rate of 0.5 s or 1 s	Tektronix TG 501	8.3.7.2.
Effective delay	–	Correct effective delay (⩾ 10 ns)	Square-wave voltage of 2.4 Vp-p – 100 kHz – rise time ⩽ 3 ns	–	8.3.7.3.
Single shot	–	Accu is refreshed	Square-wave signal of 1,2 V p.p – 1 kHz	PM 5129	8.3.7.4.
Multiple	–	All four memories are refreshed	Square-wave signal of 1,2 V p.p – 1 kHz.	PM 5129	8.3.7.5.
TRIGGERING					8.3.8.
Trigger sensitivity	R2867 – (A22)	Triggered display	Sine-wave signal of 20 mVp-p – 2 kHz to X3	PM 5129	8.3.8.
Trigger slope and level	–	Starting point trace on positive or negative signal edge when the SLOPE switch is operated	Sine-wave signal of 240 mVp-p – 2 kHz to X3	PM 5129	8.3.8.
	–	Correct LEVEL function	Sine-wave signal of 960 mVp-p – 2 kHz to X3	PM 5129	8.3.8.
Trigger level AUTO	–	Trigger point can be shifted over at least 4 divisions when operating the LEVEL control	Sine-wave signal of 240 mVp-p – 100 Hz to X3	PM 5129	8.3.8.
Trigger level EXT	–	Trigger point can be shifted over total signal amplitude when operating the LEVEL control	Sine-wave signal of 240 mVp-p – 100 Hz to X3 Sine-wave signal of 3.2 Vp-p – 2 kHz to X6	PM 5129 PM 5129	8.3.8.
Trigger level EXT÷10	–	Trigger point can be shifted over total signal amplitude when operating the LEVEL control	Sine-wave signal of 240 mVp-p – 100 Hz to X3 Sine-wave signal of 32 Vp-p – 2 kHz to X6	PM 5129 PM 5129	8.3.8.
Trigger sensitivities	–		Sine-wave signal to X3	Tektronix SG 503 + SG 504	8.3.8.
		Triggered display in AUTO	100 Hz – 0,75 div.		
		Triggered display in AUTO	60 MHz – 1,5 div.		
		Triggered display in AC	20 Hz – 0,75 div.		
		Triggered display in AC	60 MHz – 1,5 div.		
		Triggered display in DC	10 Hz – 0,75 div.		
		Triggered display in DC	60 MHz – 1,5 div.		
		Triggered display in EXT	40 MHz – 0,15 V		
		Triggered display in EXT	60 MHz – 0,3 V		
		Triggered display in EXT ÷ 10	40 MHz – 1,5 V		
		Triggered display in EXT ÷ 10	60 MHz – 3 V		
	–	Triggered display in DC	Sine-wave signal of 300 mV p.p – 60 MHz to X4	Tektronix SG 503 + SG 504	8.3.8.
Triggering at mains frequency	–	Triggered display	Mains voltage derived signal of 200 mVp-p to X3	–	8.3.8.
TV triggering	–	Triggered display	T.V. signal CCIR norm – 625 lines – positive video – amplitude 0.5 division sync pulse.	–	8.3.8.
Trigger delay	R2910 – (A22)	Correct trigger delay functioning	Square-wave signal of 2 MHz – rise time ⩽ 1 ns to X3	–	8.3.8.

ADJUSTMENT	ADJUSTING ELEMENT + UNIT	ADJUSTING RESULT OR CHECK RESULT	RECOMMENDED INPUT SIGNALS	EXAMPLE OF MEASURING INSTRUMENT	CHAPTER
X-Y MODE	–	Straight line with an angle of 45^o with the positive horizontal axis	Sine-wave signal of 240 mVp-p – 2 MHz to X3 and X4	–	8.3.9.
RANGE INDICATION	–	Correct V/div display change when connecting probes with range indication	–	–	8.3.10.
PLOTTER OUTPUTS	–	Correct plotting	Square-wave signal	PM 5129	8.3.11.
PERIODIC AND RANDOM DEVIATIONS	–	Ripple-noise – instability of the trace and microfony ≤ 2 mm		–	8.3.12.
EFFECT OF MAINS VOLTAGE VARIATIONS	–	No change in trace height and trace width when mains voltage is varied by + or –10 %	CAL signal to X3 and X4	–	8.3.13.

8.3. CHECKING AND ADJUSTING PROCEDURE

8.3.1. Power supply

Power consumption

- Check that the mains adapter switch S45 has been set to the local mains voltage and connect the instrument to such a voltage.
- Switch the oscilloscope on and check that the pilot lamp on POWER ON the front panel lights up.
- Check that the current consumption does not exceed 300 mA at 220 V local mains and 600 mA at 117 V local mains. (Measured with a moving-iron meter.)

+12 V supply voltage

- Check at nominal mains voltage that the voltage on the positive pole of C1513 on unit A15 is +12,6 V ± 1 %; if necessary readjust potentiometer FEEDBACK **R1646** on unit A16.
- Check that this voltage does not vary more than ± 60 mV when the mains voltage is varied between 200 V and 265 V or between 100 V and 130 V.
- Check that the +5 V on the positive pole of C1527 on unit A15 is +5 V ± 0.25 V.
- Check that the oscilloscope starts at 180 V or 90 V.

Frequency

- Set the mains input voltage to 180 V or 90 V.
- Check that the voltage on the positive pole of C1513 on unit A15 has a ripple that does not exceed 10 mV. If necessary; readjust potentiometer FREQ. **R1647** on unit A16.

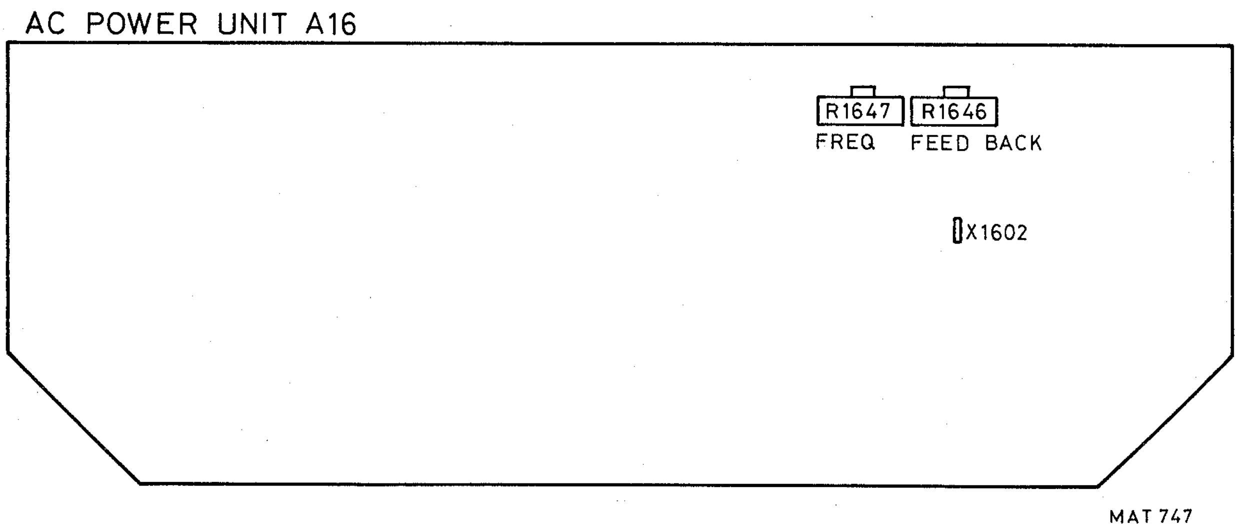


Fig. 8.3.1.

8.3.2. Cathode-ray-tube circuit

Cathode voltage

- Check that the voltage on testpoint X1502 on unit A15 is −1.5 V.
  If necessary; readjust potentiometer **R1591** on unit A15.

Intensity

- Set the front panel INTENS control R15 to 90° from its left hand stop.
- Adjust potentiometer **R1589** on unit A15 in such a way that the trace is just not visible.

Focus and astigmatism

- Depress pushbutton DISPLAY STO1 S2.
- Depress pushbutton WRITE S12-A.
- Set channel A AMPL/DIV switch S20 to position 50 mV/div.
- Set TIME/DIV switch S23 to position 50 ms/div.
- Depress pushbutton AUTO S29-A of the trigger mode selector switch.
- Depress pushbutton Yx5 S16-B.
- Apply a sine-wave voltage of 240 mV-2 kHz to the A-input socket X3.
- Depress pushbutton SAVE STO1 S8.
- Depress pushbutton LOCK S12-B.
- Depress pushbutton DOTS S17.
- Set FOCUS LINE potentiometer **R1588** on unit A15 in its mid-position.
- Set the front panel INTENS control R15 to maximum brightness.
- Adjust FOCUS potentiometer **R1506** on unit A15 and ASTIGMATISM potentiometer **R1587** on unit A15 for a sharp and well-defined trace over the whole screen area.
- Check that the trace remains focused when the intensity is varied.

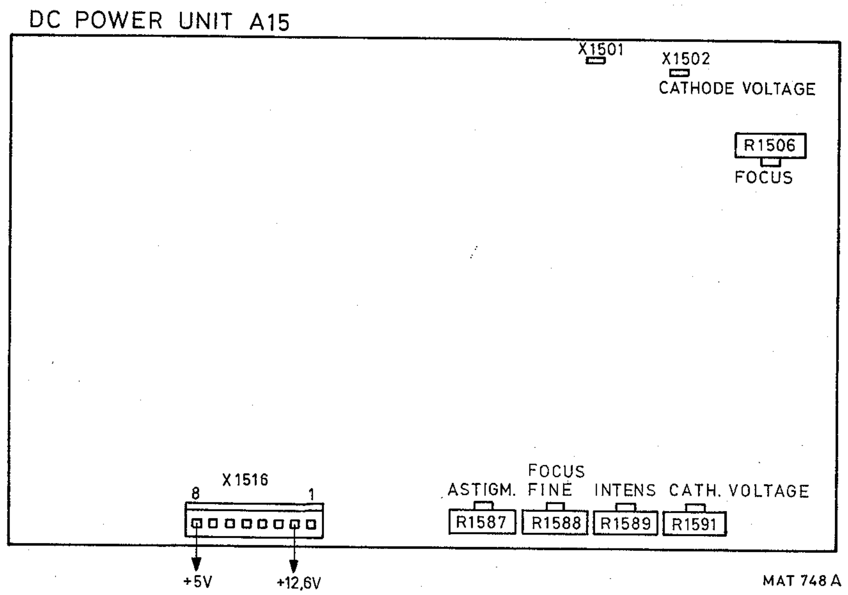


Fig. 8.3.2.

Trace rotation

- Release push-button DOTS S17.
- Depress push-button WRITE S12-A.
- Depress both push-buttons CLEAR S11 and SAVE STO1 S8 simultaneously.
- Set the STO1 Y POSITION control R4 in such a way that the trace is placed in the centre of the screen.
- Check that the trace runs exactly in parallel with the horizontal graticule lines; if necessary, readjust the TRACE ROTATION screw driver control **R16** on the front panel.
- Release push-button DISPLAY STO1 S2.

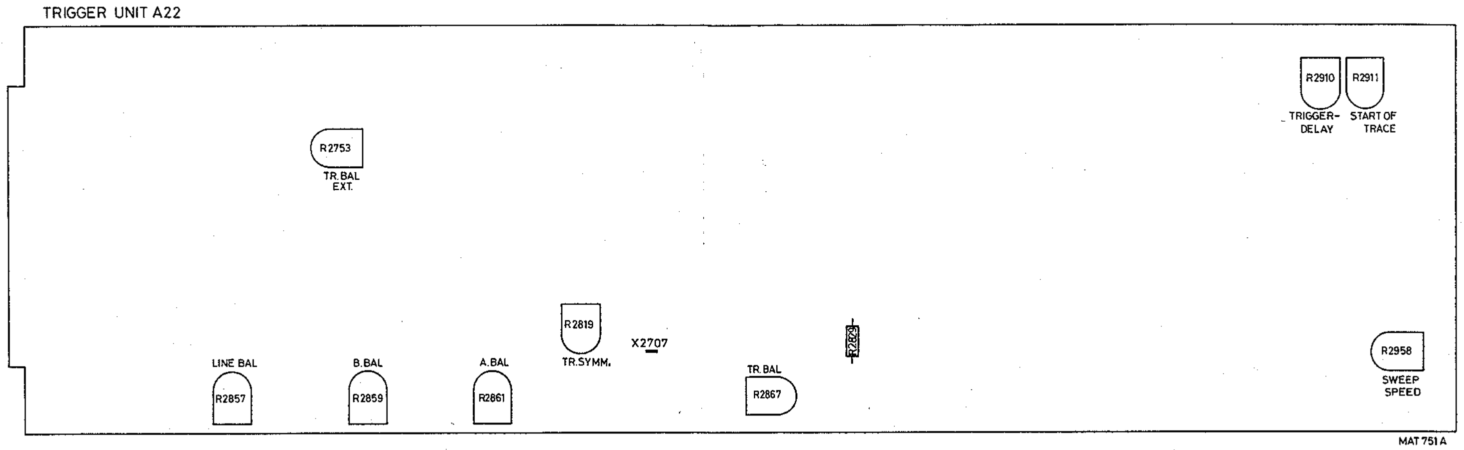


Fig. 8.3.3.

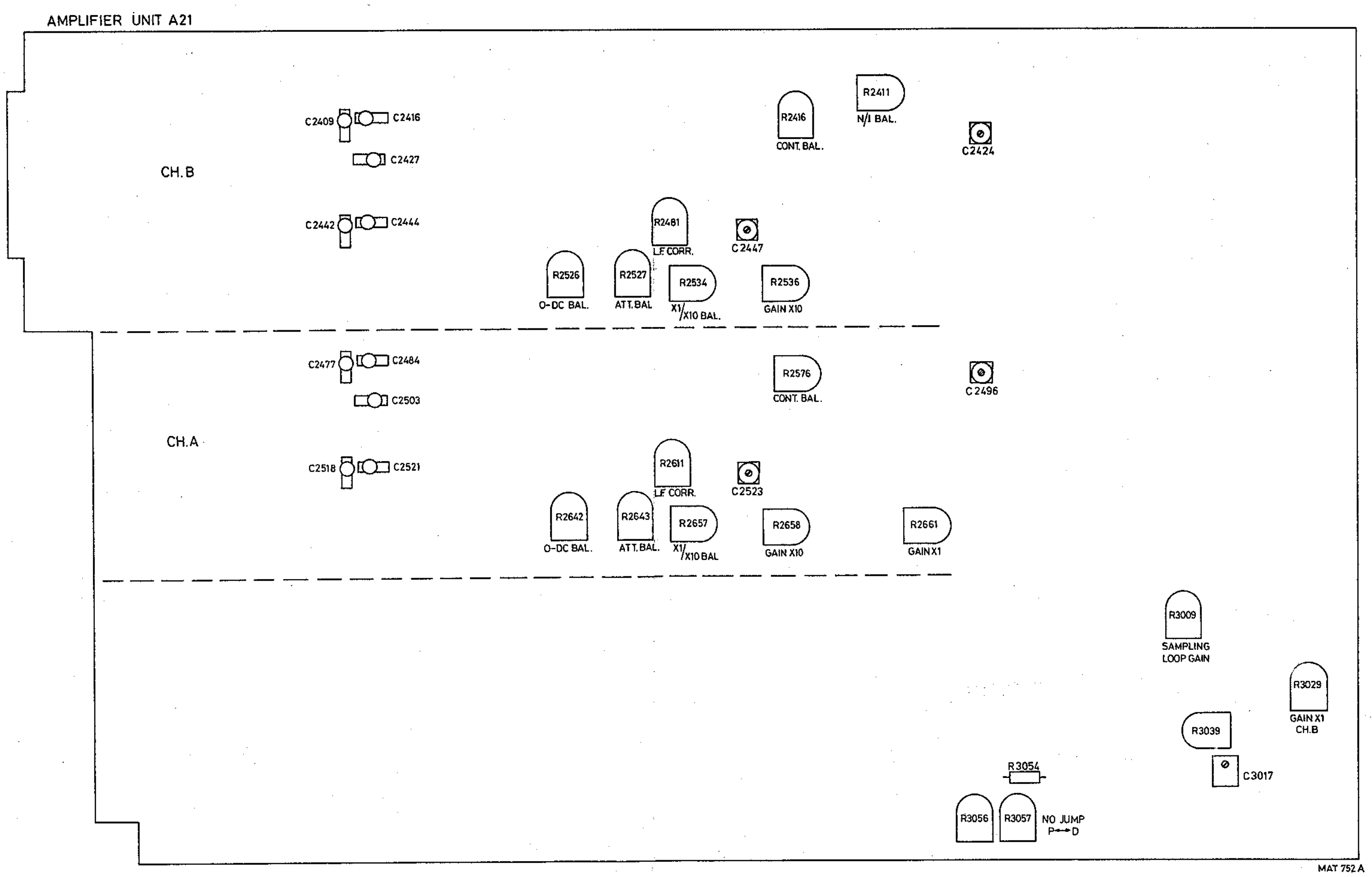


Fig. 8.3.4.

8.3.3. Pre-adjustment P²CCD circuit

- Check that the trace does not jump when the TIME/DIV switch S23 is switched between positions 0.2 ms/div and 0.5 ms/div.
  If necessary, readjust potentiometer **R3057** on unit A21.

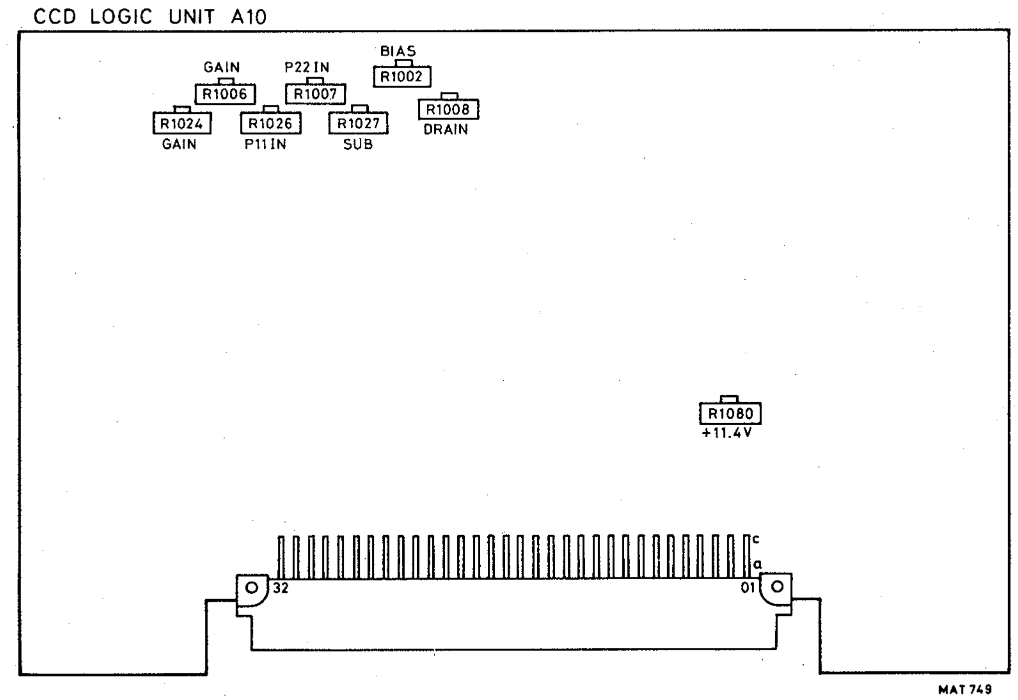


Fig. 8.3.5.

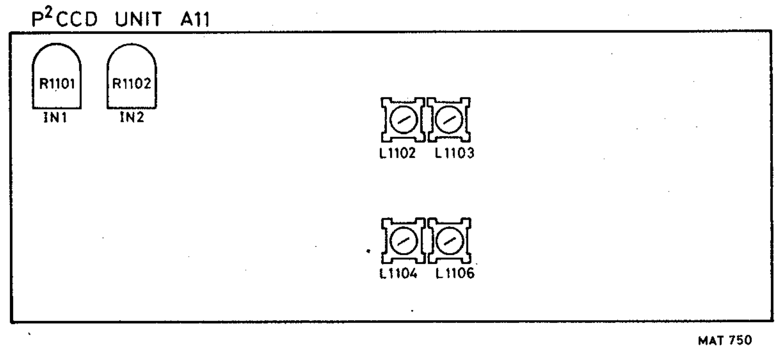


Fig. 8.3.6.

8.3.3.1. P^2CCD adjusting procedure

IMPORTANT: Before adjusting the P^2CCD be sure that the channels are adjusted correctly in direct mode.

PRELIMINARY SETTINGS

- Depress the channel A ON-OFF pushbutton S32.
- Release the channel B ON-OFF pushbutton S34.
- Set the channel A variable AMPL/DIV control R7 in the CAL position.
- Depress RECURR S38-C
- Depress pushbutton AUTO S29
- Depress pushbutton A S39
- Depress pushbutton ACCU DISPLAY S1
- Release pushbutton ST01, STO 2 and STO 3, S2, S3, S4
- Depress pushbutton WRITE S12-A
- Depress pushbutton X = T S15-A
- Depress pushbutton Y x5 S16-B
- Depress pushbutton DOTS S17
- Set the X MAGN control R2 into its CAL position.
- Depress the channel A 0 pushbutton and adjust the trace to the centre of the screen with the OFFSET control and release the 0 pushbutton.
- Set the channel A AMPL/DIV switch to .1V/DIV.
- Set the TIME/DIV switch S23 to position 0,5ms/div.

Due to the fact that the P^2CCD is divided in two parts, the following procedure is necessary to equalize the differences between these two parts.
The signal ENKEL is connected to ground to obtain the possibility to use the PM 3310 oscilloscope itself for adjustings.

- Apply a sine wave of 1kHz with an amplitude to obtain 8 divisions display height to the channel A input socket X3.
- Connect point C22 of PCB connector X2003 (Unit A20) to ground.
- Set the TIME/DIV switch S23 to position 0.2ms/div.

- Connect the measuring oscilloscope to signal V OUT (testpoint X 1001 unit 10) and trigger it on the negative edge of the signal NULIN (testpoint X902 unit 9).
  Settings of the measuring oscilloscope :1V/div; 1ms/div; zero line on the centre of the screen.

ADJUSTING PROCEDURE

1. Adjust supply voltage at X1007-8 to 11,40 Volt with R1080.
2. Set sliders of

	R 1027 to +5V	(SUB X1007-6)
	R 1026 to +6V	(P11 IN X1007-4)
	R 1007 to +6V	(P22 IN X1007-5)
	R 1024 to midposition	
	R 1006 to midposition	
	R 1002 to 9V	(BIAS X1007-11)
	R 1008 to 22V	(DRAIN X 1007-7)

3. Adjust **R 1101** and **R 1102** so that the signal is symmetrical aroun the zero line of the measuring oscilloscope.
4. Increase the frequency of the applied signal up to 300kHz through all time settings from 0,2ms/div. . . . . . 0,5μs/div. and check that the signal remains symmetrical around the zeroline of the measuring oscilloscope. If necessary adjust **R 1007** and **R 1026** in position 0,5μs/div. Start with point 3 again and adjust for optimum and continue with point 5.
5. Apply a triangle-wave of 1kHz and set the TIME/DIV switch of the PM 3310 to 0,2ms/div. Adjust **R 1002** so that the signal on the screen of the PM 3310 is as linear as possible. Apply a sine-wave again.
6. Set the TIME/DIV switch to 0,5ms/div and adjust the input signal to 8 divisions and switch to 0,2ms/div. again. Adjust **R 1008** so that the signals on the measuring oscilloscope cover each other within two subdivisions around the zero line (see fig. A).

7. Adjust **R 1006** and **R 1024** for 8 divisions deflection on the screen of the PM 3310 and so that both signals cover each other. If necessary start with point 5 again.
8. Apply a square wave of 1kHz and check that the signal corresponds to fig. B. If necessary increase the SUB voltage to 6 or 7V with **R 1027**. Apply a sine wave of 1kHz again.
9. If the last adjustment was necessary start with point 3 again, and if no adjustment was made continue.
10. Increase the frequency of the applied signal to 300kHz, set the TIME/DIV switch to 0,5μs/div. and adjust **L 1102, L 1103, L 1104** and **L 1106** so that the signals cover each other on the measuring oscilloscope.

11. Decrease the input frequency to 1kHz and set the TIME/DIV switch to 0,2ms/div. and adjust **R 1006** and **R 1024** for 8 divisions deflection on the PM 3310 screen.
    Adjust **R 1008** so that the signals cover each other on the measuring oscilloscope within two subdivisions around the zero line (see fig. A).

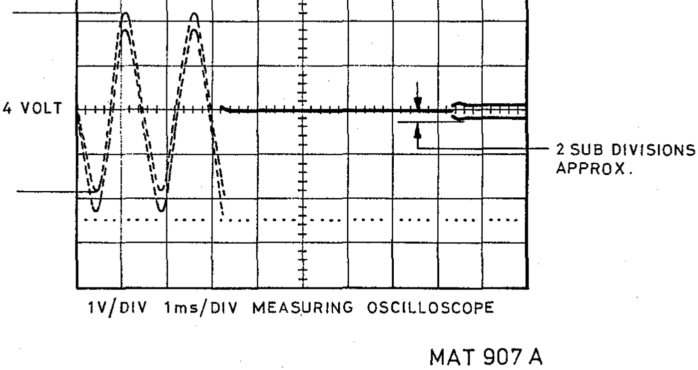


Fig. A.

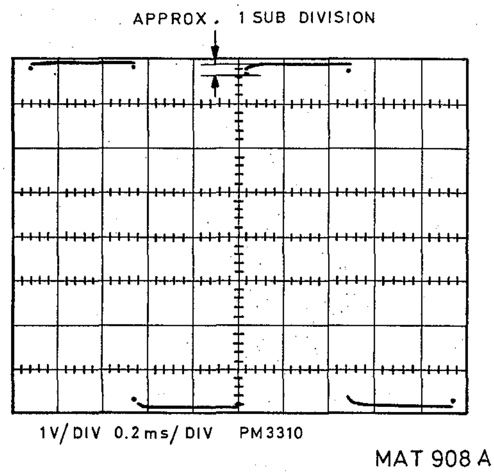


Fig. B.

8.3.4. Balance adjustments

The adjustments of the vertical channels A and B are identical.
The knobs, sockets and adjusting elements of channel B are shown in brackets after those of channel A.
These balance adjustments influence one another and must, therefore, be readjusted in the sequence in which they are described.

8.3.4.1. Vertical amplifier balances

0-DC balance

- Set channel A (B) AMPL/DIV switch S20 (S22) in position 50 mV/div.
- Check that the trace does not jump when pushbutton 0 S31 (S35) is operated.
  If necessary, readjust potentiometer **R2642 (R2526)** on unit A21 for minimum jump.
- Release the channel A (B) 0 pushbutton S31 (S35).

Attenuator balance

- Set the trace in the centre of the screen with the channel A (B) OFFSET control R10 (R12).
- Release pushbutton DOTS 16-C.
- Set TIME/DIV switch S23 to position 0.5 ms/div.
- Depress channel A (B) ON-OFF pushbutton S32 (S34) to ON.
- Check that the trace does not jump when the AMPL/DIV switch S20 (S22) is switched between 10 mV/div. 20 mV/div and 50 mV/div.
  If necessary readjust potentiometer **R2643 (R2527)** on unit A21 for minimum jump.

X1/X10 balance

- Check that the trace does not jump, when the channel A (B) AMPL/DIV switch S20 (S22) is switched between positions 50 mV/div and 0.1 V/div.
  If necessary, readjust potentiometer **R2657 (R2534)** on unit A21 for minimum jump.

Continue balance

- Set channel A (B) AMPL/DIV switch S20 (S22) in position 50 mV/div.
- Check that the trace does not move when the channel A (B) AMPL/DIV continuous control R7 (R8) is rotated between minimum and maximum.
  If necessary, readjust potentiometer **R2576 (R2416)** on unit A21 for minimum shift.
- Release the channel A (B) ON-OFF pushbutton S32 (S34) to OFF.

Follow the same procedure for channel B.

Normal/Invert balance (ONLY for channel B)

- Depress channel B ON-OFF pushbutton S34 to ON.
- Check that the trace does not jump when the channel B OFFSET control S28 is pulled and pushed.
  If necessary, readjust potentiometer **R2411** on unit A21 for minimum jump.
- Push channel B OFFSET control S28 to normal.

8.3.4.2. Trigger point symmetry

- Check that the voltage on testpoint X2707 is –1 V.
- If necessary, readjust potentiometer R2819 on the trigger-unit.

8.3.4.3. Trigger balances AC-DC

External

- Depress channel B ON-OFF pushbutton S34 to ON.
- Set TIME/DIV switch S23 to position 0.5 ms/div.
- Set the channel B AMPL/DIV switch S22 to position 1 V/div (0.2 V/div on the screen and in the alphanumeric display).
- Depress pushbutton EXT S39-C of the trigger source selector switch.
- Depress pushbutton AC S29-B of the trigger mode selector switch.
- Apply a sine-wave signal of 1.2 Vp-p – 2 kHz to the channel B input socket X4 as well as to the EXT input socket X6.
- Set the LEVEL control R9 for a stable display.

- Check that the trigger point does not shift when the trigger mode selector switch S29 is switched between AC and DC. If necessary, readjust potentiometer **R2753**, on unit A22 for minimum shift, in DC-mode.
- Remove the input signal from EXT input socket X6 and from channel B input socket X4.

A balance

- Depress channel A ON-OFF pushbutton S32 to ON.
- Release channel B ON-OFF pushbutton S34 to OFF.
- Set the channel A AMPL/DIV switch S20 to position 1 V/div (0.2 V/div on the screen and in the alphanumeric display).
- Depress pushbutton A S39-A of the trigger source selector switch.
- Depress pushbutton AC S29-B of the trigger mode selector switch.
- Apply a sine-wave signal of 1.2 Vp-p – 2 kHz to the channel A input socket X3.
- Set the LEVEL control R9 for a triggered display.
- Check that the trigger point does not move when the trigger mode selector switch S29 is switched between AC and DC.
  If necessary, readjust potentiometer **R2861** on unit A22, in DC-mode.
- Remove the input signal from channel A input socket A3.

B balance

- Depress channel B ON-OFF pushbutton S34 to ON.
- Release channel A ON-OFF pushbutton S32 to OFF.
- Set the channel B AMPL/DIV switch S22 to position 1 V/div (0.2 V/div on the screen and in the alphanumeric display).
- Depress pushbutton B S39-B of the trigger source selector switch.
- Depress pushbutton AC S29-B of the trigger mode selector switch.
- Apply a sine-wave signal of 1.2 Vp-p – 2 kHz to the channel B input socket X4.
- Set the LEVEL control R9 for a triggered display.
- Check that the trigger point does not shift when the trigger mode selector switch S29 is switched between AC and DC.
  If necessary, readjust potentiometer **R2859** on unit A22, in DC - mode.
- Release the channel B ON-OFF pushbutton S34 to OFF.
- Remove the input signal from channel B input socket X4.

LINE balance

- Depress pushbuttons EXT and EXT÷10 of the trigger source selector switch S39 simultaneously (LINE).
- Depress the channel A ON-OFF switch S32 to ON.
- Set TIME/DIV switch S23 to position 10 ms/div.
- Apply a mains voltage derived signal via a mains transformer with an amplitude of 6 divisions to the channel A input socket X3.
- Check that the trigger point does not move when the trigger mode selector switch S29 is switched between AC and DC.
  If necessary readjust potentiometer **R2857** on unit A22, in DC-mode.
- Remove the input signal from channel A input socket X3.

8.3.4.4. Trigger amplifier balance

- Set TIME/DIV switch S23 to position 0.5 ms/div.
- Set the LEVEL control R9 in its mid-position.
- Depress pushbutton A S39-A of the trigger source selector switch.
- Depress pushbutton AUTO S29-C of the trigger mode selector switch.
- Apply a sine-wave signal of 1.2 Vp-p – 2 kHz to the channel A input socket X3.
- Check that the trigger point is situated in the middle of the signal amplitude.
  If necessary, readjust potentiometer **R2867** on unit A22.

8.3.5. Final amplifier adjustments

Vertical trace height

- Depress the channel A ON-OFF switch S32 to ON.
- Depress pushbutton A of the trigger source selector switch S39.
- Depress pushbutton AUTO of the trigger mode selector switch S29.
- Depress pushbutton Yx5 S16-B.
- Depress pushbutton WRITE S12-A.
- Depress the ACCU DISPLAY pushbutton S1.
- Set the TIME/DIV switch S23 to position 0.5 ms/div.
- Depress pushbutton CLEAR S11 and shift the trace to −1 div simultaneously.
- Apply a signal to channel A input socket X3 with an amplitude so high that the display on the C.R.T. screen is blinking at the upper side.
- Adjust potentiometer **R2008** on unit A20 so that the display is blinking at + 4 divisions.
- Remove the input signal.

Display positions ACCU - STO1 - STO2 - STO3

- Depress the four ACCU - STO1 - STO2 and STO3 DISPLAY pushbuttons S1-S2-S3 and S4.
- Depress pushbutton CLEAR S11, keep it in the depressed position and depress then the three pushbuttons SAVE STO1 S8, SAVE STO2 S9 and SAVE STO3 S10.
- Depress pushbutton LOCK S12-B.
- Turn the ACCU - STO1 - STO2 and STO3 Y POSITION controls R1-R4-R5 and R6 such that the four traces cover each other in the centre of the screen.
- Depress pushbutton Yx1 S16-A.
- Adjust potentiometer **R2009** on unit A20 for a distance of two divisions between the traces.

Invert registers

- Set the channel A AMPL/DIV switch S20 to position 1 V/div
- Apply a sine-wave voltage of 1.2 Vp-p — 2 kHz to the channel A input socket X3.
- Depress pushbuttons SAVE STO1 S8, SAVE STO2 S9 and SAVE STO3 S10.
- Pull the invert switches S5, S6 and S7 and check that STO1, STO2 and STO3 are inverted.
- Push the switches S5, S6 and S7.
- Remove the input signal.

Horizontal trace length

- Clear STO1, STO2 and STO3.
- Adjust with potentiometer **R2011** on unit A20 the length of the horizontal lines on the screen for 10.1 divisions.

Dot joint adjustments

- Release pushbutton DOTS S17.
- Depress the channel A ON-OFF pushbutton S32 to ON.
- Release the channel B ON-OFF pushbutton S34 to OFF.
- Depress pushbutton WRITE S12-A.
- Depress pushbutton Yx5 S16-B.
- Apply a sine-wave signal with a trace height for 6 divisions display and a frequency of 2 kHz to the channel A input socket X3.
- Set TIME/DIV switch S23 to position 0.2 ms/div.
- Depress pushbutton SAVE STO1 S8.
- Depress DISPLAY pushbutton STO1 S2.
- Release the ACCU - STO2 and STO3 DISPLAY buttons S1 - S3 and S4.
- Check that the dot join faults in vertical direction are equal for the positive going edge and the negative going edge of the signal.
  If necessary equalize these faults with potentiometer **R2019** on unit A20.
- Eliminate the dot join faults by adjusting potentiometer **R2018** on unit A20.
- Adjust potentiometer **R2072** on unit A20 so that the dots on the screen are really connected with each other.
- Depress the channel B ON-OFF pushbutton S34 to ON.

- Depress pushbutton SAVE STO1 S8.
- Check that in double channel operation the dot join system still functions correctly.
- Adjust potentiometer **R2039** on unit A20 for minimum cross-talk between the two channels A and B.
- Remove the input signal.
- Release pushbutton STO1 DISPLAY S2.

CALibration voltage

- Check that the amplitude of the CAL voltage on CAL terminal X1 is 3V ± 0.7%.
  If necessary, readjust potentiometer **R2017** on unit A20.
- Check that the frequency of the CAL voltage is 2.5 kHz.

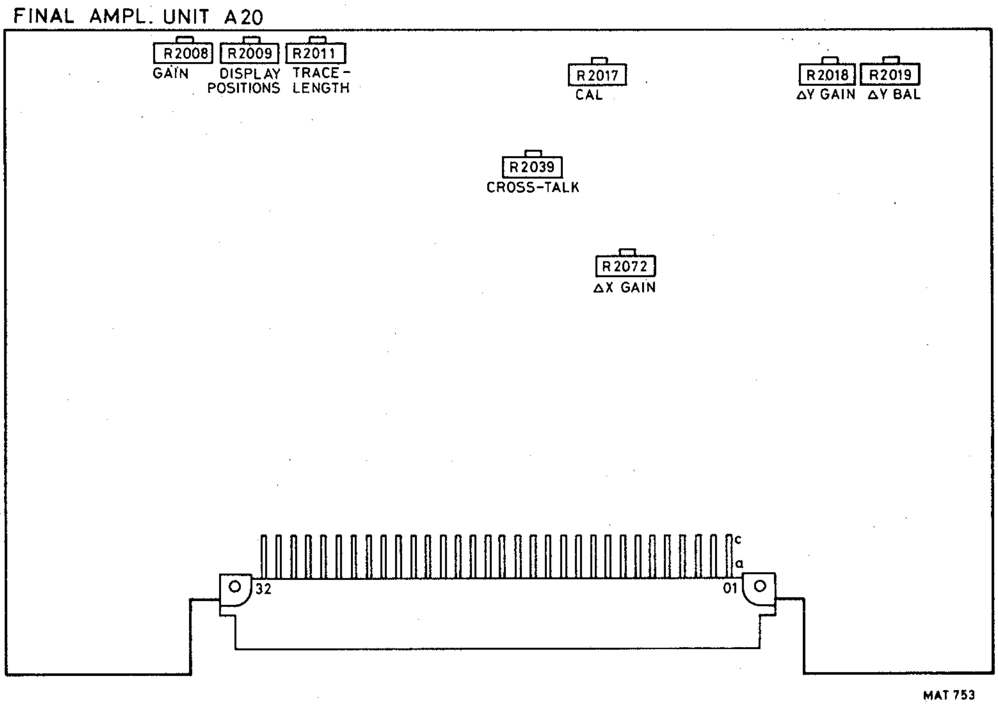


Fig. 8.3.7.

8.3.6. Vertical channels

The adjustments of the vertical channels A and B are identical.
The knobs, sockets and adjusting elements of channel B are shown in brackets after those of channel A.

8.3.6.1. Vertical amplifier sensitivity adjustments

Before checking the sensitivities, check the balances in accordance with section 8.3.4.

Channel B gain x1

- Depress the channel A and B ON-OFF pushbuttons S32 and S34 to ON.
- Release the channel A and B AC-DC switches S30 and S36 and the 0 switches S31 and S35.
- Set the channel A and B AMPL/DIV switches S20 and S22 to position 0.2 V/div (40 mV/div on the screen and in the alphanumeric display).
- Set the channel A and B AMPL/DIV continuous control R7 and R8 in the CAL position.
- Set the channel A and B OFFSET controls R10 and R12 so that the traces are shifted to the centre of the screen.
- Depress pushbutton RECURR S38-C.
- Set the TIME/DIV switch S23 to position 0.5 ms/div.
- Depress pushbutton AUTO of the trigger mode selector switch S29.
- Depress pushbutton B of the trigger source selector switch S39.
- Depress the ACCU DISPLAY pushbutton S1.
- Release the DISPLAY pushbuttons STO1 - STO2 and STO3, S2-S3 and S4.
- Depress pushbutton WRITE S12-A.
- Depress pushbutton X = t S15-A.
- Depress pushbutton Y x 5 S16-B.
- Set the XMAGN control R2 to its CAL position.
- Apply a square-wave signal of 240 mVp-p – 2 kHz to the channel B input socket X4.
- Adjust potentiometer **R3029** on unit A21 for a trace height of 6 divisions.

Channel A gain x1

- Depress pushbutton A of trigger source selector switch S39.
- Apply a square-wave signal of 240 mVp-p – 2 kHz to the channel A input socket X3.
- Adjust potentiometer **R2661** on unit A21 for a trace height of 6 divisions.

Channel A (B) gain x10

- Set channel A (B) AMPL/DIV switch S20 (S22) to position 20 mV/div (4 mV/div on the screen and in the alphanumeric display).
- Apply a square-wave signal of 24 mVp-p – 2 kHz to channel A (B) input X3 (X4).
- Adjust potentiometer **R2658 (R2536)** on unit A21 for a trace height of 6 divisions.

L.F. Correction

- Set channel A (B) AMPL/DIV switch S20 (S22) to position 0.2 V/div (40 mV/div on the screen and in the alphanumeric display).
- Apply a square-wave signal of 240 mVp-p – 100 Hz to channel A (B) input socket X3 (X4).
- Set TIME/DIV switch S23 to position 1 ms/div.
- Check that the pulse top is straight; if necessary, readjust potentiometer **R2611 (R2481)** on unit A21.

AC-DC channel A (B)

- Depress push-button AC-DC of channel A (B) - S30 (S36).
- Check that the pulse top difference is more than 0.5 div.

Sampling loop gain

- Set the TIME/DIV switch S23 to position 0.2 ms/div.
- Depress the channel A and B ON-OFF pushbuttons S32 and S34 to ON.
- Apply a square-wave signal of 240 mV – 2 kHz to channel A input socket X3.
- Set the channel B OFFSET control R12 so that the trace is set in the middle of the screen.
- Set the TIME/DIV switch S23 to position 0.5 ms/div.

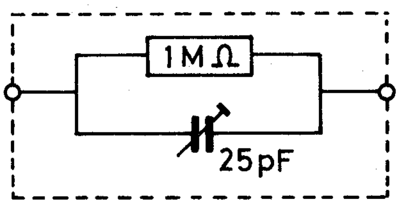
- Adjust potentiometer R3009 on unit A21 so that the pulse top is straight.
- Adjust potentiometer R3056 on unit A21 so that the pulse variation is symmetrical.
- Adjust potentiometer R3057 on unit A21 so that the channel B line is in the middle of the screen. If the range of R3057 is too small, change resistor R3054 (limits between 5K62 and 2K49).
- If necessary, repeat this procedure.

8.3.6.2. Input attenuators (square-wave response and input capacitance)

- Set TIME/DIV switch S23 to position 20 µs/div.
- Depress channel A (B) ON-OFF pushbutton S32 (S34) to ON.
- Release channel B (A) ON-OFF pushbutton S34 (S32) to OFF.
- Release the channel A (B) AC-DC pushbutton S30 (S36) to DC.
- Release the channel A (B) 0 pushbutton S31 (S35).
- Apply a square-wave voltage with a frequency as indicated in the table below, rise time ⩽ 100 ns to the channel A (B) input socket X3 (X4); peak to peak value as indicated in the table below.
- Check that the pulse top is straight, and pulse top errors does not exceed + or –5 %; if necessary readjust the relevant trimmers on unit A21.

2 : 1 DUMMY PROBE

1 MHz//25 pF



A (B) AMPL/DIV S20 (S22)	CHANNEL A (B) INPUT SIGNAL	ADJUSTER	TRACE HEIGHT
20 mV/div	2 kHz – 24 V	**C2503 (C2427)**	6 div +/–5 %
20 mV/div	10 kHz – 48 mV via dummy	C dummy	6 div +/–5 %
0.2 V/div	2 kHz – 240 mV	–	6 div +/–5 %
0.2 V/div	10 kHz – 480 mV via dummy	–	6 div +/–5 %
2 V/div	2 kHz – 2.4 V	**C2521 (C2444)**	6 div +/–5 %
2 V/div	10 kHz – 4.8 V via dummy	**C2518 (C2442)**	6 div +/–5 %
20 V/div	2 kHz – 24 V	**C2484 (C2416)**	6 div +/–5 %
20 V/div	10 kHz – 48 V via dummy	**C2477 (C2409)**	6 div +/–5 %

Note: The difference in input capacitance between channel A and channel B may not exceed 0.5 pF.

- Check that the range of the continuous control R7 (R8) is 1 : > 2.6.
- Remove the input signal.

8.3.6.3. Square-wave response vertical channel

Square-wave response channel A (B) x 1

- Set TIME/DIV switch S23 to position 20 ns/div.
- Depress channel A (B) ON-OFF switch S32 (S34) to ON.
- Release channel B (A) ON-OFF switch S34 (S32) to OFF.
- Set the channel A (B) AMPL/DIV switch S20 (S22) to position 0.2 V/div (40 mV/div on the screen and in the alphanumeric display).
- Apply a square wave voltage of 240 mV - 1 MHz, risetime ⩽ 1 ns to the channel A input socket X3.
- Check the square wave response of the final Y-amplifier. Pulse top errors may not exceed 1 subdivision; if necessary, readjust R3039 and C3017.
- Check the square wave response of channel A (B). Pulse top errors may not exceed 1 subdivision; if necessary, readjust C2424 and C2447 (C2496 and C2523).

Channel A square-wave response in ADD-mode

- Depress pushbutton ADD S33.
- Depress channel A ON-OFF pushbutton S32 to ON.
- Release channel B ON-OFF pushbutton S34 to OFF.
- Depress pushbutton A of the trigger source selector S39.
- Check that the square-wave response does not change when pushbutton ADD S33 is operated.

Channel B square-wave response in ADD-mode

- Release channel A ON-OFF pushbutton S32 to OFF.
- Depress channel B ON-OFF pushbutton S34 to ON.
- Depress pushbutton B of the trigger source selector S39.
- Check that the square-wave response does not change when pushbutton ADD S33 is operated.

Square-wave response channel B-INVERT

- Depress channel B ON-OFF pushbuttons S34 to ON.
- Check that the square-wave response does not change when the PULL FOR –B switch S28 is operated.
- Remove the input signal.

8.3.6.4. *Bandwidth*

- Depress channel A (B) ON-OFF pushbutton S32 (S34) to ON.
- Release channel B (A) ON-OFF pushbutton S34 (S32) to OFF.
- Set the channel A (B) AMPL/DIV switch S20 (S22) to position 10 mV/div (2 mV/div on the screen and in the alphanumeric display).
- Apply a sine-wave signal of 12 mVp-p and a frequency of 1 MHz to channel A (B) input socket X3 (X4).
- Set TIME/DIV switch S23 in such a position that about ten sine-waves are displayed on the screen (1 ms/div).
- Check that the trace height is 6 divisions.
- Increase the frequency of the input signal to 60 MHz (amplitude still 12 mVp-p).
- Set TIME/DIV switch S23 in such a position that about ten sine-waves are displayed on the screen (20 ns/div).
- Check that the trace height is at least 4,8 divisions.
- Remove the input signal.

If the trace height is less than 4,8 divisions, check the square-wave response again.

8.3.6.5. *OFFSET control range*

- Set TIME/DIV switch S23 to position 0.2 μs/div.
- Set channel A (B) AMPL/DIV switch S20 (S22) to position 0.2 V/div (40 mV/div on the screen and in the alphanumeric display).
- Apply a sine-wave signal of 1,2 Vp-p and a frequency of 2 MHz (= 30 div).
- Check that the display can be shifted more than 15 divisions on both sides by turning the channel A (B) OFFSET controls R10 (R12), the sine wave must be shifted out of the trace.
- Remove the input signal.

8.3.6.6. *Common mode rejection*

- Depress the channel A and B ON-OFF pushbuttons S32 and S34 to ON.
- Depress the channel A and B 0 pushbuttons S31 and S35.
- Set the channel A and channel B AMPL/DIV switches S20 and S22 to positions 0.2 V/div.
- Set the channel A and channel B AMPL/DIV continuous controls R7 and R8 to their CAL positions.
- Set the channel A and B OFFSET controls R10 and R12 so that the traces are situated in the centre of the screen.
- Release the channel A and B 0 pushbuttons S31 and S35.
- Depress pushbutton ADD S33.
- Pull PULL FOR –B switch S28.
- Apply a sine-wave signal with an amplitude of 960 mVp-p and a frequency of 2 MHz to the channel A as well as the channel B input sockets X3 and X4.
- Check that the rejection factor is better than 100. (Signal $<$ 0.25 divisions).

8.3.7. Time coefficient adjustments

8.3.7.1. Recurrent-mode

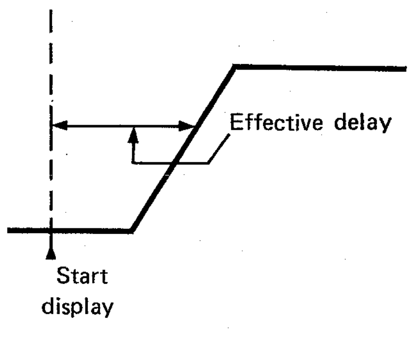
- Depress channel A ON-OFF pushbutton S32 to ON.
- Release channel B ON-OFF pushbutton S34 to OFF.
- Turn the XMAGN control R2 in the CAL position.
- Set channel A AMPL/DIV switch S20 to position 0.2 V/div (40 mV/div on the screen and in the alphanumeric display).
- Set the TIME/DIV switch S23 to position 20 ns/div.
- Apply a time marker signal of 160 mV and a pulse repetition rate of 20 ns to the channel A input socket X3.
- Check that the entre 8 cycles have a total width of 8 divisions.
  If necessary readjust potentiometer **R2958** on unit A22.
- Check that the range of the variable X-magn. R2 is 1 : > 2.5.
- Depress pushbutton DOTS S16-C.
- Turn potentiometer R2911 clockwise so that a horizontal trace appears at the left-hand side of the screen.
- Now adjust **R2911** on unit A22 so that the horizontal trace just disappears i.e. the first dot of the signal starts on the most left graticule line.
- Release pushbutton DOTS S16-C.
- Check all the TIME/DIV switch S23 positions in recurrent mode.
- Remove the input signal.

8.3.7.2. Roll-mode

- Depress pushbutton Y x 1 S16-A.
- Depress pushbutton ROLL S38-A.
- Apply a time marker signal with a repetition rate of 0.5 s to the channel A input socket X3.
- Depress pushbutton RUN-STOP S37.
- Check the ROLL-mode in TIME/DIV switch S23 position 0.5 s/div.
- Depress pushbutton CLEAR S11.
- Apply a voltage of +3 V to the external socket X6 and check that the ROLL-mode starts.
- Remove the voltage from X6.
- Depress pushbutton CLEAR S11.
- Apply a time marker signal with a repetition rate of 1 s to the channel A input socket X3.
- Depress pushbutton RUN-STOP S37.
- Check the ROLL-mode in TIME/DIV switch S23 position 1 s/div.
- Depress pushbutton CLEAR S11.
- Set the jumper S1201 on unit A12 in the left position.
- Depress pushbutton RUN-STOP S37.
- Check the ROLL-mode in TIME/DIV switch S23 position 60 min/div.
- Set the jumper S1201 on unit A12 in the right position.
- Remove the input signal.

8.3.7.3. Effective delay

- Depress pushbutton RECURR S38-C.
- Depress pushbutton Yx5 S16-B.
- Set the TIME/DIV switch S23 to position 10 ns/div.
- Set channel A AMPL/DIV switch S20 to position 2 V/div (0.4mV/div. on the screen and in the alphanumeric display).
- Apply a square-wave voltage of about 2.4 Vp-p – 100 kHz and a rise time ⩽ 3 ns to the A input socket X3.
- Depress pushbutton DC of the trigger mode selector switch S29.
- Set LEVEL control R9 for a triggered display.
- Check that the effective delay is more than 1 division.



8.3.7.4. Single shot

- Depress pushbutton DISPLAY ACCU S1.
- Depress pushbuttons DISPLAY STO1, STO2 and STO3 (S2, S3 and S4).
- Depress pushbutton Yx1 S16-A.
- Set TIME/DIV switch S23 to position 2 ms/div.
- Depress pushbutton AC of the trigger mode selector switch S29.
- Apply a square wave voltage of 1.2 Vp-p, frequency 1 kHz to the channel A input socket X3.
- Set LEVEL control R9 for a triggered display.
- Remove the input signal.
- Depress pushbutton SINGLE S38-B and check that the pilot lamp NOT TRIG'D B23 lights up (depress RESET S37).
- Apply the square wave voltage to the channel A input socket X3 again.
- Check that the ACCU is refreshed and that the pilot lamp NOT TRIG'D B23 is extinguished.

8.3.7.5. Multiple

- Depress pushbutton RECURR S38-C.
- Remove the input signal.
- Depress pushbuttons ROLL and SINGLE (= MULTIPLE) S38-A and S38-B and check that the pilot lamp NOT TRIG'D B23 lights up (depress pushbutton RESET S37).
- Apply the square wave voltage to the channel A input socket X3 again.
- Check that all 4 registers are refreshed and that the pilot lamp NOT TRIG'D B23 is extinguished.
- Release pushbuttons S2, S3 and S4.
- Remove the input signal.

8.3.8. Triggering

Trigger sensitivity

- Depress pushbutton Yx5 S16-B.
- Depress channel A ON-OFF pushbutton S32 to ON.
- Depress pushbutton AUTO of the trigger mode selector switch S29.
- Depress pushbutton RECURR S38-C.
- Set channel A AMPL/DIV switch S20 to position 0.2 V/div (40 mV/div on the screen and in the alpha-numeric display).
- Set TIME/DIV switch S23 to position 0.5 ms/div.
- Depress pushbutton A of the trigger source selector switch S39.
- Set LEVEL control R9 in its mid-position.
- Apply a sine-wave signal of 20 mVp-p –2 kHz to the channel A input socket X3.
- Adjust potentiometer **R2867** on unit A22 so that a triggered display is obtained.
- Remove the input signal.

Trigger slope and level

- Push SLOPE switch S27 to "+".
- Apply a sine-wave signal of 240 mVp-p – 2 kHz to the channel A input socket X3.
- Check that the display is triggered on the positive going edge of the signal and that the trigger point moves upwards when the LEVEL control R9 is turned clockwise.
- Pull SLOPE switch S27 to "–".
- Check that the display is triggered on the negative going edge of the input signal.
- Push SLOPE switch S27 again to "+".
- Depress pushbutton AC of the trigger mode selector switch S29.
- Rotate the LEVEL control R9 fully clockwise and anti-clockwise and check that in both extreme positions the trace is not triggered.
- Increase the signal amplitude of the input signal to 960 mVp-p.
- Rotate the LEVEL control R9 fully clockwise and anti-clockwise and check that in both extreme positions the trace remains triggered.
- Remove the input signal.

Trigger level AUTO

- Depress pushbutton AUTO of the trigger mode selector switch S29.
- Apply a sine-wave signal of 240 mVp-p – 100 Hz to channel A input socket X3.
- Rotate LEVEL control R9 and check that the trigger point can be shifted over 4 divisions.
- Remove the input signal.

Trigger level EXT

- Depress pushbutton AC of the trigger mode selector switch S29.
- Depress pushbutton EXT of the trigger source selector switch S39.
- Apply a sine-wave signal of 240 mVp-p – 100 Hz to channel A input socket X3.
- Apply a sine-wave signal of 3.2 Vp-p – 2 kHz to EXT input socket X6.
- Rotate LEVEL control R9 and check that the trigger point can be shifted over the total signal amplitude.

Trigger level EXT÷10

- Depress pushbutton EXT÷10 of the trigger source selector switch S39.
- Apply a sine-wave signal of 32 Vp-p – 2 kHz to EXT input socket X6.
- Rotate LEVEL control R9 and check that the trigger point can be shifted over the total signal amplitude.
- Remove the input signal.

Trigger sensitivities

- Depress pushbutton A of the trigger source selector switch S39.
- Apply a sine-wave signal to the channel A input socket X3 according to the table below.
- Set the TIME/DIV switch S23 to such a position that about ten sine-waves are displayed on the screen.
- Set the LEVEL control R9 for a stationary display.

– Check the trigger sensitivity in accordance with the table below.

TRIGGER MODE	INPUT FREQUENCY	AMPLITUDE
AUTO	100 Hz	0.75 div
	60 MHz	1.5 div
AC	20 Hz	0.75 div
	60 MHz	1.5 div
DC	10 Hz	0.75 div
	60 MHz	1.5 div

– Check the trigger sensitivity for EXT and EXT÷10 for l.f. and h.f. signals.
– Remove the input signal.
– Depress channel B ON-OFF pushbutton S34 to ON.
– Release channel A ON-OFF pushbutton S32 to OFF.
– Set channel B AMPL/DIV switch S22 to 0.2 V/div. (40 mV/div on the screen and in the alphanumeric display).
– Depress pushbutton B of the trigger source selector switch S39.
– Apply a sine-wave signal with an amplitude of 1,5 division – 60 MHz to the channel B input socket X4.
– Check that a triggered display is obtained.
– Remove the input signal.

Triggering at mains frequency

– Depress channel A ON-OFF pushbutton S32 to ON.
– Release channel B ON-OFF pushbutton S34 to OFF.
– Depress pushbutton AC of the trigger mode selector switch S29.
– Set TIME/DIV switch S23 to position 2 ms/div.
– Depress pushbuttons EXT and EXT÷10 of trigger source selector switch S39 simultaneously (LINE).
– Apply a mains voltage derived signal of 200 mVp-p via a transformer to the channel A input socket X3.
– Check that independent on the position of LEVEL control R9 a triggered display can be obtained.
– Remove the input signal.

T.V. triggering

– Depress pushbutton A of the trigger source selector switch S39.
– Depress pushbutton TVF of trigger mode selector switch S29.
– Apply a TV signal (CCIR norm - 625 lines - positive video - amplitude 0.5 division sync. pulse) to channel A input socket X3.
– Set TIME/DIV switch S23 to position 0.1 ms/div.
– Check that a triggered display is obtained with a frame pulse and an equalization pulse on the screen.
– Remove the TV signal.

Trigger delay adjustment

– Depress pushbutton AUTO of the trigger mode selector switch S29.
– Set TIME/DIV switch S23 to 10 ns/div.
– Set the TRIGGER DELAY alphanumeric display B21 to zero by pressing both pushbuttons UP and DIGIT S24 and S25 simultaneously (RESET).
– Apply a square-wave signal of 2 MHz, rise time ⩽ 1 ns to channel A input socket X3.
– Check that the leading edge of the signal is visible on the screen.
– Set the number 100 in the alphanumeric display B21 with pushbuttons DIGIT and UP S25 and S24.
– Adjust potentiometer **R2910** on unit A22 so that the leading edge of the signal is again visible on the screen.
– Set the number 0 in the display B21 by pressing both pushbuttons UP and DIGIT S24 and S25 simultaneously.
– Remove the input signal.

Trigger delay

- Set TIME/DIV switch S23 to position 0.2 ms/div.
- Depress pushbutton DC of the trigger mode selector switch S29.
- Set the number 0002 in the alphanumeric display B21 with pushbuttons DIGIT and UP S25 and S24 and set pushbutton DIGIT S25 to the least significant DIGIT (= 2).
- Apply a square-wave voltage of 2 kHz to the channel A input socket X3.
- Set LEVEL control R9 for a triggered display.
- Switch TIME/DIV switch S23 to position 0.5 μs/div and check that the beginning of the signal can be magnified on the screen; if necessary, use pushbutton UP S24.
- Set the TIME/DIV switch S23 to position 0.2 μs/div and check that the number in the alphanumeric display B21 is 100 (max. value in sampling mode).

8.3.9. X-Y mode

- Depress the channel A and B ON-OFF pushbuttons S32 and S34 to ON.
- Depress the channel A and B pushbuttons "0" S31 and S35.
- Set the channel A and B AMPL/DIV switch S20 and S22 to 0.2 V/div.
- Set TIME/DIV switch S23 to position 0.5 μs/div.
- Set the channel A and B OFFSET controls R10 and R12 so that the spot is shifted to the centre of the screen.
- Release the channel A and B pushbuttons "0" S31 and S35.
- Depress pushbutton X = A/Y = B S15-B.
- Apply a sinewave signal of 240 mVp-p – 2 MHz to the channel A as well as the channel B input sockets X3 and X4.
- Check that a straight line is displayed with a angle of 45° with the positive horizontal axis.
- Check the same with TIME/DIV switch S23 in position 0.2 μs/div.
- Depress the channel A "0" pushbutton S31.
- Check that a vertical line is displayed.
- Remove the input signals.

8.3.10. Range indication

- Depress pushbutton X = t S15-A.
- Depress channel A (B) ON-OFF pushbutton S32 (S34) to ON.
- Release channel B (A) ON-OFF pushbutton S34 (S32) to OFF.
- Read the A (B) V/div. alphanumeric display B10 (B11) contents.
- Connect a probe with range indication to the channel A (B) input socket X3 (X4).
- Check that the indication in the A (B) V/div. alphanumeric display B10 (B11) is changed by a factor of 10.

8.3.11. Plotter outputs

- Store a square-wave signal of 1 div. in memory STO1.
- Select memory STO1 with SELECT pushbutton S14.
- Connect voltmeters to the plotter output sockets on the rear side of the instrument.
- Depress pushbutton PLOT S18 and check the following:
  1. X-OUT and Y-OUT are 0 Volt
  2. PENLIFT goes to 0 Volt
  3. X-OUT and Y-OUT are generating output signals
- Check that during plotting an intensified dot is visible on the screen.
- Depress pushbutton PLOT S18 again and check that the PLOT action is stopped.
- Remove the input signal.

8.3.12. Periodic and random deviations

These must be checked only with the cabinet plates fitted:

- Depress pushbutton RECURR S38-C.
- Set TIME/DIV switch S23 to position 1 ms/div.
- Depress channel A (B) ON-OFF pushbutton S32 (S34) to ON.
- Depress channel B (A) ON-OFF pushbutton S34 (S32) to OFF.
- Release the channel A and B pushbuttons "0" S31 and S35.
- Depress pushbuttons AC/DC of the input coupling controls S30 and S36 to AC.
- Set both AMPL/DIV switches S20 and S22 to positions 10 mV/div and the AMPL/DIV continuous controls R7 and R8 to their CAL positions.
- Depress pushbutton AUTO of the trigger mode switch S29.
- Check that ripple-noise-instability of the trace and microfony does not exceed 4 mm.

8.3.13. Effect of mains voltage variations

- Depress channel A ON-OFF pushbutton S32 to ON.
- Depress channel B ON-OFF pushbutton S34 to ON.
- Set channel A AMPL/DIV switch S20 to position 1 V/div.
- Set channel B AMPL/DIV switch S22 to position 1 V/div.
- Connect the CAL terminal x1 output signal with the channel A as well as the channel B input sockets X3 and X4.
- Vary the mains voltage by + and –10 %.
- Check that neither trace height nor trace width changes and that the brilliance remains the same.

8.4. ADJUSTMENT INTERACTIONS

Adjustment \ Interaction	Power supply	C.R.T. circuit	Balance adjustment vertical amplifier	Trigger balance AC-DC	Trigger amplifier balance	Trigger point symmetry	Final amplifier adjustments	Vertical amplifier sensitivities	P^2CCD adjustments	Input attenuators	Square-wave response vertical channel	Time coefficients	Trigger sensitivity	Trigger delay
Power supply	□	□	□	□	□	□	□	□	□	□	□	□	□	□
C.R.T. circuit		□					□	□						
Balance adjustments vertical amplifier			□											
Trigger balance AC-DC				□										
Trigger amplifier balance					□	□								
Trigger point symmetry					□	□								
Final amplifier adjustments							□							
Vertical amplifier sensitivities							□	□	□					
P^2CCD adjustments								□	□					
Input attenuators										□				
Square-wave response vertical channel											□			
Time coefficients							□					□		□
Trigger sensitivity													□	
Trigger delay														□

9. CORRECTIVE MAINTENANCE

9.1. REPLACEMENTS

WARNING: The opening of covers or removal of parts, except those to which access can be gained by hand, is likely to expose live parts, and also accessible terminals may be live.
The instrument shall be disconnected from all voltage sources before any adjustment, replacement or maintenance and repair during which the instrument will be opened.
If afterwards any adjustment, maintenance or repair of the opened instrument under voltage is inevitable, it shall be carried out only by a skilled person who is aware of the hazard involved.
Bear in mind that capacitors inside the instrument may still be charged even if the instrument has been separated from all voltage sources.

Standard parts

Electrical and mechanical replacement parts can be obtained through your local Philips organisation or representative. However, many of the standard electronic components can be obtained from other local suppliers.
Before purchasing or ordering replacement parts, check the parts list for value tolerance, rating and description.

Note: Physical size and shape of a component may affect instrument performance, particularly at high frequencies. Always use direct-replacement components, unless it is known that a substitute will not degrade instrument performance.

Special parts

In addition to the standard electronic components, some special components are used.
These components are manufactured or selected by Philips to meet specific performance requirements.

Transistors and integrated circuits

Transistors and I.C.'s (integrated circuits) should not be replaced unless they are actually defective. If removed from their sockets during routine maintenance return them to their original sockets. Unnecessary replacement or switching of semiconductor devices may affect the calibration of the instrument. When a transistor is replaced, check the operation of the part of the instrument that may be affected. (see interaction table 8.4.)

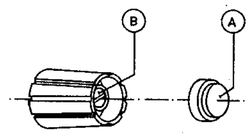
WARNING: Handle silicone grease with care. Avoid getting silicone grease in the eyes. Wash hands thoroughly after use.

Any replacement component should be of the original type or a direct replacement. Bend the leads to fit the socket and cut the leads to the same length as on the component being replaced.

9.1.1. Replacing single knobs

- Prise off cap A.
- Slacken screw (or nut) B.
- Pull the knob from the spindle.

When fitting a knob or cap, ensure that the spindle is in a position which allows reference lines to be coincident with the markings on the text plate of the oscilloscope.

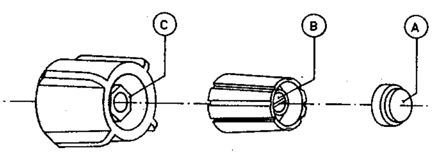


MAT 163

9.1.2. Replacing double knobs

- Prise off cap A and slacken screw B.
- Pull the inner knob from the spindle.
- Slacken nut C and pull the outer knob from the spindle.

When fitting a knob or cap, ensure that the spindle is in a position which allows reference lines to be coincident with the markings on the text plate of the oscilloscope.



MAT 163

9.1.3. Replacing carrying handle

1. Remove both the upper and lower cabinet plates after slackening the four quick-release fasteners at the corners of each plate. To prevent the fasteners coming apart, do not slacken more than two turns.
2. Remove the plastic strip which is snapped on to the grip.
3. Remove the four screws which secure the grip to the brackets (these screws have been locked with a sealing varnisch).
4. Depress the push-buttons in the brackets and turn the carrying handle as far as possible to the upper side of the oscilloscope.
5. Keep the push-button of the right-hand bracket depressed and pull the bracket from its bearing 1).
6. Remove the grip from the remaining bracket.
7. Depress the push-button of the left-hand bracket and turn the latter as far as possible to the lower side of the instrument.
8. Keep the push-button depressed and pull the bracket from its bearing.

If it is impossible to remove the left-hand bracket in this way, remove also its bearing in a similar way as described in footnote 1).

1) With some instruments it may be impossible to remove the handle in the described way. This is due to an extra securing plate in the right-hand bearing. In that case, DO NOT USE FORCE, but work in accordance with the following procedure which replaces points 3, 4 and 5.

3. Remove the two screws which secure the grip to the right-hand bracket.
4. Remove the two hexagonal bolts which secure the right-hand bearing to the side strip.
5. Depress the push-button of the right-hand bracket and take the bearing from the bracket.

9.1.4. Removing the cabinet plates and the screen bezel

Both upper and lower cabinet plate can be removed after slackening one or two turns the four quick release fasteners at the corners of each plate. Do not slacken the fasteners more than two turns, otherwise they may come apart.

The screen bezel can be detached by pressing the longer edges and pulling out.

Fig. 9.1.1.

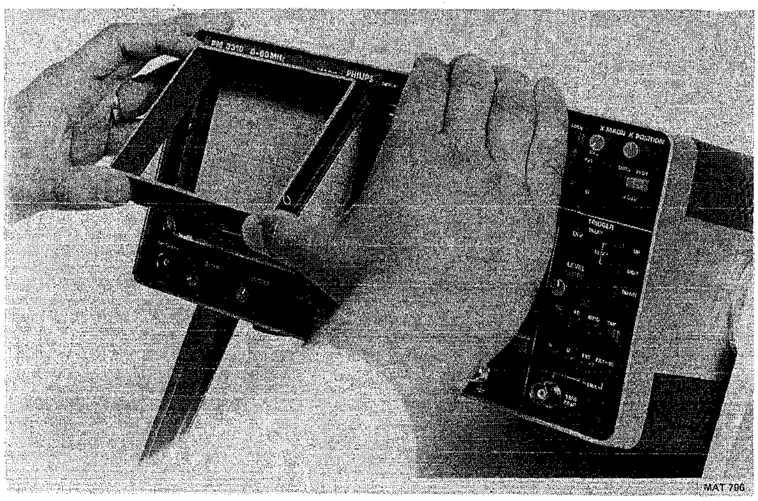


Fig. 9.1.2.

9.1.5. Replacing the plug-in units

The plug-in units are:

A4 – microprocessor unit
A6 – RAM unit
A7 – buffer unit
A8 – conversion unit
A9 – ACL unit
A10 – CCD logic unit
A12 – time-base unit
A13 – delay trigger unit
A14 – IEC bus interface (if available)
A20 – final amplifier unit

These circuit boards can be easily removed after disconnecting the various cables.
Unit A10 can only be removed after slackening the screw at the upper right side of the unit which secures the heatsinks to the metal spport.

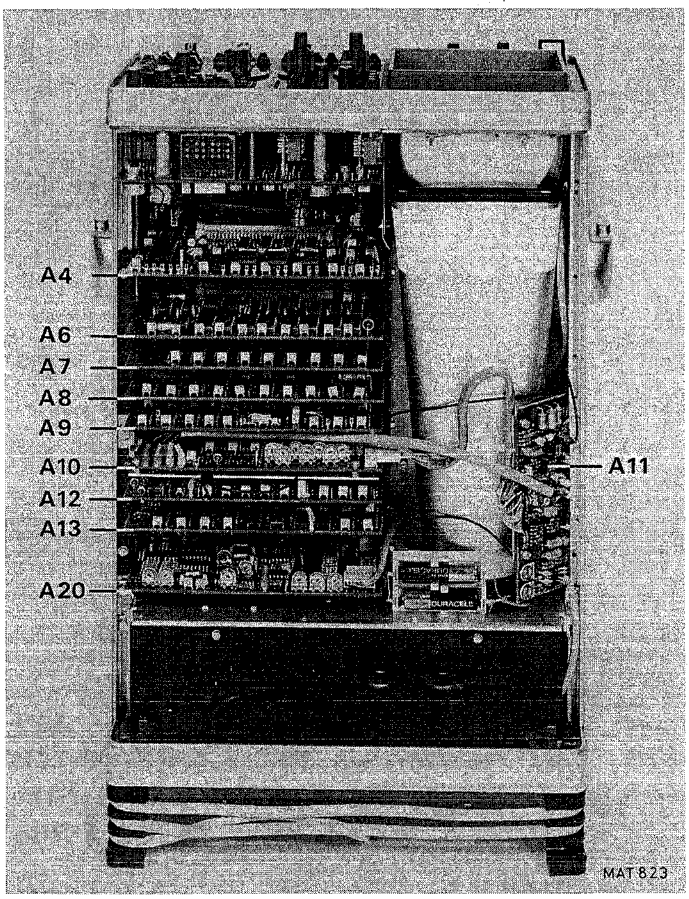


Fig. 9.1.3.

9.1.6. Replacing the P2CCD unit A11

This unit A11 is located at the upper left side of the instrument above the C.R.T.

- Remove the four miniature coaxial plugs from unit A10.
- Remove the multipole connector from unit A10.
- Remove the two miniature coaxial plugs from unit A11.
- The unit can be removed after unscrewing the two screws which secure the unit to the side frame.

ATTENTION: The P2CCD is a highly sensitive MOS circuit. Upon delivery of a spare unit the miniature coaxial plugs are interconnected so that no static charge can influence the circuit.
Moreover the multipole connector is short circuited by a conductive plastic foam material.
When mounting a new unit, first secure the unit mechanically to the side frame.
After having taken the precautions as described in chapter 9.3. remove the conductive plastic foam of the multipole connector and plug it in the CCD logic unit.
After that, the miniature coaxial connectors may be disconnected and connected to the right connectors one by one.

9.1.7. Replacing the front unit A2

- Remove the screen bezel and the contrast plate.
- Remove all the knobs except the pushbutton knobs.
- Remove the textplate with the two screws underneath the channel A AMPL/DIV switch and the TIME/DIV switch.
- Remove the four screws as indicated in the figure.

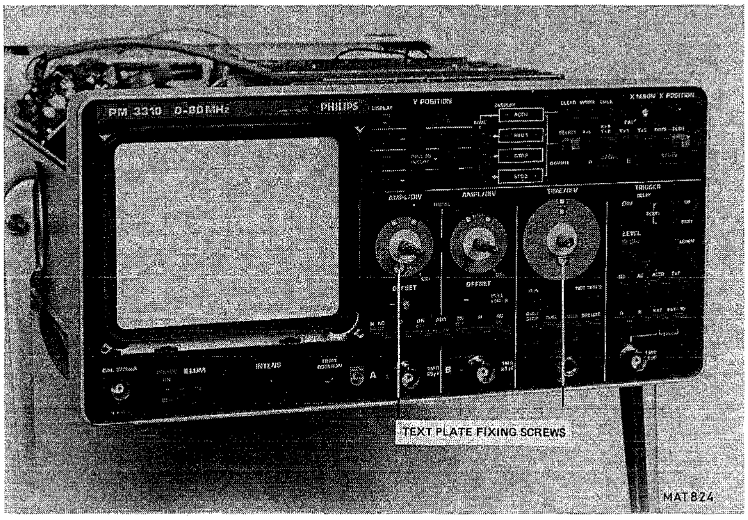


Fig. 9.1.4.

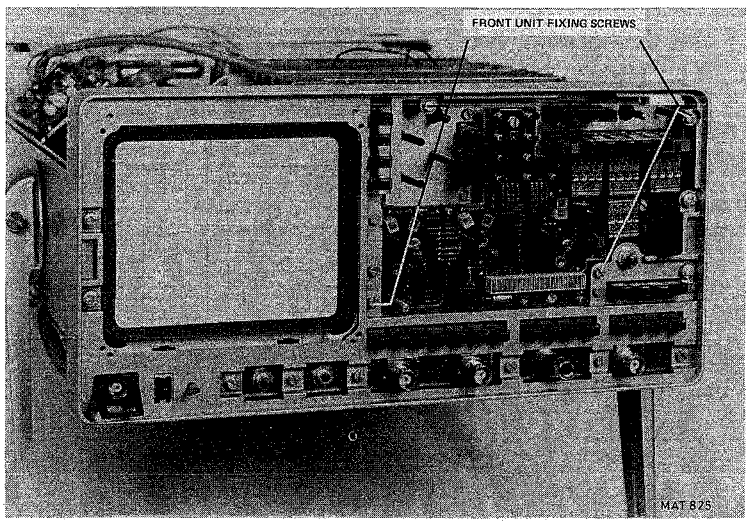


Fig. 9.1.5.

- Remove plug in unit A4.
- Disconnect the two multipole connectors on the motherboard unit A3 which are situated behind the front unit.
- Press the front unit to the rear by pushing the connector which is mounted underneath the TIME/DIV switch.
- Carefully remove the unit out of the instrument.
- When mounting again, carefully insert the front unit into the instrument.
- Be sure that the bottom of the unit is completely outlined with the connector on the motherboard.
- Carefully press the front unit into the connector.
- Fix the unit, the textplate and the knobs again in the reversed sequence.
- Plug in the microprocessor unit A4.
- Plug in the two multipole connectors.

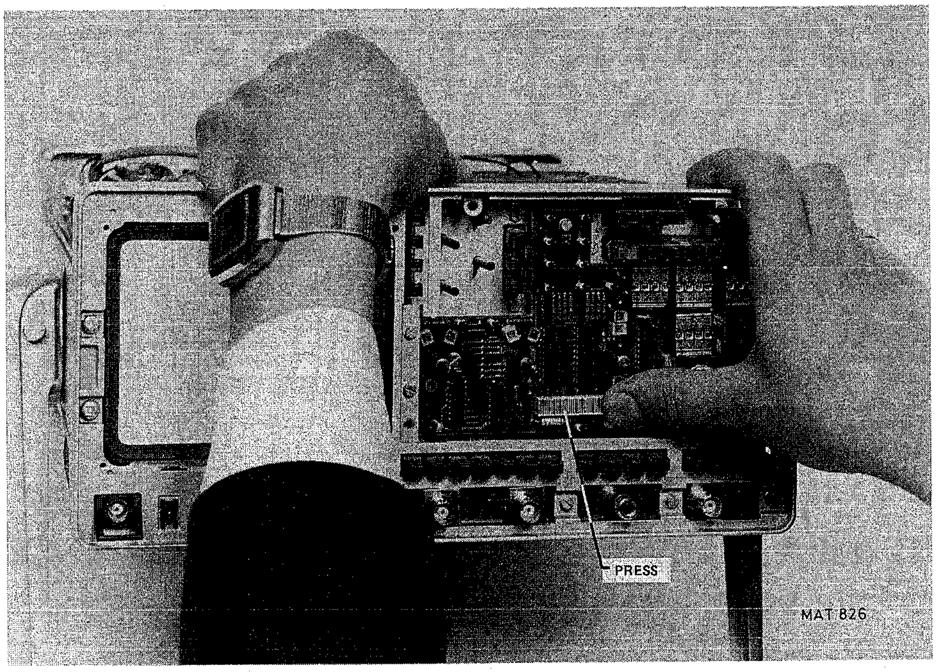


Fig. 9.1.6.

9.1.8. Replacing the LEVEL control

- Remove the front unit A2.
- Unsolder the wires on the potentiometer.
- Unscrew the potentiometer.

9.1.9. Replacing the trigger mode selector switch

- Remove the front unit A2.
- Unsolder the interconnection wire between the LEVEL potentiometer and the switch.
- Remove the two slot headed screws on the front that fixes the switch.

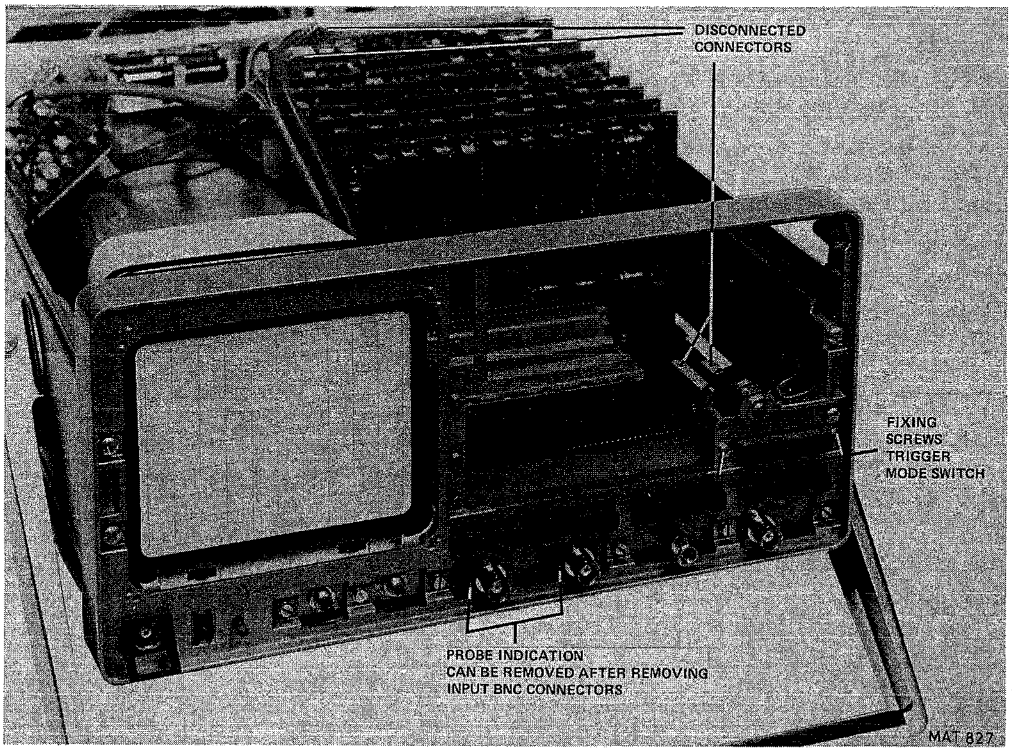


Fig. 9.1.7.

9.1.10. Replacing the C.R.T.

WARNING: Handle the C.R.T. carefully. Rough handling or scratching can cause the C.R.T. to implode.

- Remove the upper and lower instrument cabinet plate.
- Remove the bezel and the contrast plate.
- Remove the two screws that secure the upper scale illumination lamps support to the front panel and remove this support.
- Disconnect the two connectors on the C.R.T. socket from the power supply unit (A15) and the final amplifier unit (A20).
- Unsolder the red and yellow TRACE ROTATION wire from the support in the front underneath the C.R.T.
- Loosen the screw of the clamping bracket around the C.R.T. neck (accessible via the hole in the C.R.T. screen).
- Carefully withdraw the C.R.T. partly through the front panel of the instrument.
- Disconnect the EHT cable from the C.R.T. and discharge the cable and the C.R.T.
- Remove the C.R.T. and take care of the C.R.T. socket wiring.
- Remount the new C.R.T. in the reversed sequence.
- If the rubber sleeve around the neck of the C.R.T. must be slid over the neck of a replacement tube, the use of industrial talcum powder is strongly recommended, to prevent the rubber sleeve from sticking on the C.R.T. neck.

9.1.11. Replacing the DELAY LINE UNIT A18

The delay line can be removed after removing the C.R.T. (see section 9.1.10.).

- Remove the C.R.T.
- Disconnect the delay line connections from the vertical amplifier unit (A21) by removing two screws and pulling four miniature plugs.
- The delay line unit itself can be removed by removing the screw of its support bracket which is visible after the C.R.T. is removed.

9.1.12. Removing the rear plate together with the AC POWER UNIT A16

- Remove the six slot headed screws which secure the rear panel.
- Pull out the rear panel.
- Disconnect the three cables and the miniature coaxial plug.
- Unscrew the six screws that secure the unit to the rear panel.

9.1.13. Removing the DC POWER UNIT A15

- Remove the rear panel.
- Remove the internal upper and lower black metal screening plates (2 screws each).
- Disconnect all the seven multipole connectors.
- Unsolder the EHT unit cable and discharge the cable.
- Remove the unit after unscrewing the seven screws that secure the unit to the chassis.

9.1.14. Removing the mains filter

- Remove the rear panel.
- Remove the internal lower black metal screening plate (2 screws).
- Remove the screw that secures the mains filter to the chassis.

9.1.15. Removing the EHT unit A23

- Remove the rear panel.
- Unsolder the EHT unit cable.
- Remove the C.R.T. partly and disconnect and discharge the EHT cable.
- Remove the EHT unit after unscrewing the two ALLEN-screws that fix the unit to the chassis.

9.1.16. Removing the vertical amplifier unit A21

- Remove the three multipole connectors.
- Remove the screening plate from the unit.
- Remove the eight miniature coaxial sockets.
- Remove the delay line connections (see 9.1.11).
- Unsolder the two groups of connections to the trigger unit A22.
- Disconnect the wires which connect the unit to the input sockets A and B and unscrew the screws that secure the unit to these sockets.
- Remove the front panel POWER ON/OFF knob and the plastic axis which is connected to the switch and potentiometer at the rear of the instrument.
- Remove the textplate
- Remove the complete unit after unscrewing twelve screws.

9.1.17. Removing trigger unit A22

- Disconnect all the three multipole connectors from the unit.
- Disconnect the five miniature coaxial plugs from the unit.
- Unsolder the wires that connect the front panel input socket EXT to the unit.
- Unsolder the two groups of connections between this trigger unit and amplifier unit A20.
- Remove the textplate
- The unit can be removed now after unscrewing five screws.

9.2. SOLDERING TECHNIQUES

Working method:

- Carefully unsolder one after the other the soldering tags of the semi-conductor.
- Remove all superfluous soldering material. Use a sucking iron or sucking copper litze wire.
- Check that the tags of the replacement part are clean and pre-tinned on the soldering places.
- Locate the replacement semi-conductor exactly on its place, and solder each tag to the relevant printed conductor on the circuit board.

Note: Bear in mind that the maximum permissible soldering time is 10 seconds during which the temperature of the tags must not exceed 250 deg C. The use of a solder with a low melting point is therefore recommended.

Take care not damage the plastic encapsulation of the semi-conductor.

ATTENTION: When you are soldering inside the instrument it is essential to use a low-voltage soldering iron, the tip of which must be earthed to the mass of the oscilloscope.

Suitable soldering irons are:

- ORYX micro-miniature soldering instrument, type 6A, voltage 6 V, in combination with PLATO pin-point tip type 0-569.
- ERSA miniature soldering iron, type minor 040 B, voltage 6 V.
- Low Voltage Mini Soldering Iron, Type 800/12 W - 6 V, power 12 W, voltage 6 V, order no. 4822 395 10004, in combination with 1 mm-pin-point tip, order no. 4822 395 10012.

Ordinary 60/40 solder and 35- to 40-watt pencil-type soldering iron can be used to accomplish the majority of the soldering. If a higher wattage-rating soldering iron is used on the etched circuit boards, excessive heat can cause the etched circuit wiring to separate from the board base material.

9.3. HANDLING MOS DEVICES

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

Caution

Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or special IC carrier that either short-circuits all leads or insulates them from external contact.

Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord or chain. Connect all testing and handling equipment to the same surface.
Signals should not be applied to the inputs while the device power supply is off. All unused input leads should be connected to either the supply voltage or ground.

Mounting

Mount MOS integrated circuits on printed circuit boards *after* all other components have been mounted.
Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board the person mounting the circuits should touch the board before bringing MOS circuits into contact with it.

Soldering

Soldering iron tips, including those of low-voltage irons, or soldering baths should also be kept at the same potential as the MOS circuits and the board.

Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the MOS circuits have been mounted on the board proper handling precautions should still be observed.
Until the sub-assemblies are inserted into a complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the devices mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape be put on the circuit board terminals.

Transient voltages

To prevent permanent damage due to transient voltages, do not insert or remove MOS devices, or printed-circuit boards with MOS devices, from test sockets or systems with power on.

Voltage surges

Beware of voltage surges due to switching electrical equipment on or off, relays and d.c. lines.

9.4. SPECIAL TOOLS

Special tool for the slotted nut of the ACCU POSITION and XMAGN potentiometers, ordering number 5322 395 54024.

For those who want to make such a tool, we give a sketch with the dimensions in mm.
The material is silversteel N094, tempered 40-45 RC.

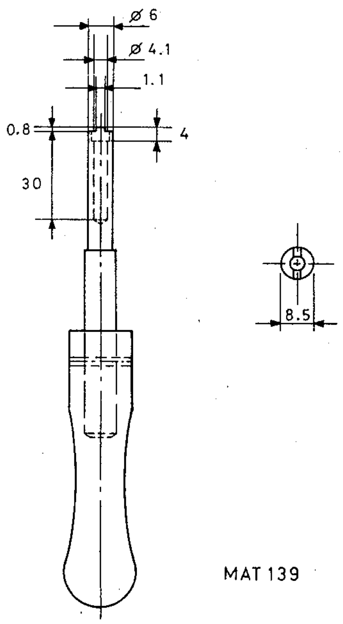


Fig. 9.4.1.

Extension card for plug-in units

To measure plug-in units of this oscilloscope an extension card is necessary.
Most components can be reached by the use of one extension card.
Complete access to all parts is possible by the use of two extension cards, but the wiring of some of the units is not long enough than.
Ordering number 5322 263 74144.

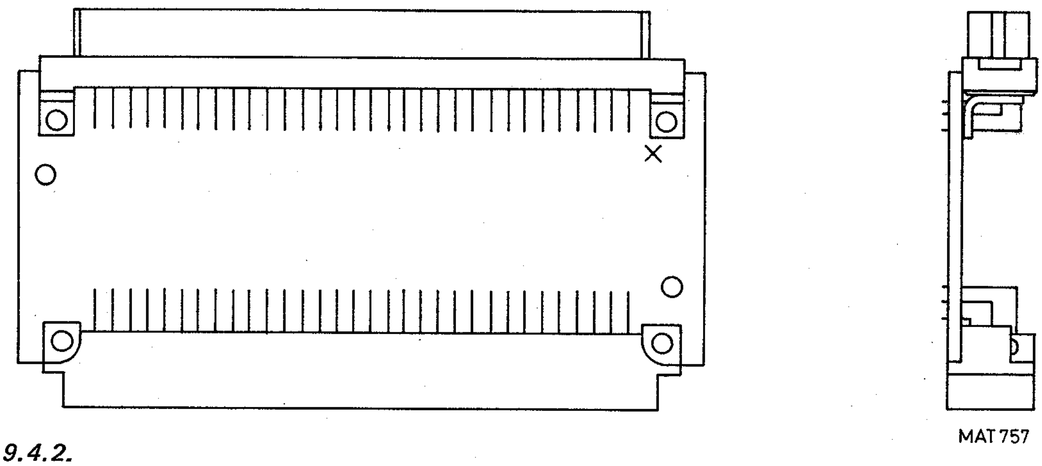


Fig. 9.4.2.

9.5. RECALIBRATION AFTER REPAIR

After any electrical component has been replaced the calibration of that particular circuit should be checked, as well as the calibration of other closely related circuits.
Since the power supply affects all circuits, calibration of the entire instrument should be checked if work has been done in the power supply or if the transformer has been replaced (see interaction table 8.4).

9.6. INSTRUMENT REPACKAGING

If the instrument is to be shipped to a Service Centre for service or repair, attach a tag showing owner (with address) and the name of an individual at your firm that can be contacted. The Service Centre needs the complete instrument serial number and a fault description.

Save and re-use the packing in which your instrument was shipped. If the original packing is unfit for use or not available, repack the instrument in such a way that no damage during transport occurs.

9.7. TROUBLE SHOOTING

9.7.1. Introduction

The following information is provided to facilitate trouble shooting. Information contained in other sections of this manual should be used along with the following information to aid in locating the defective component. An understanding of the circuit operation is helpful in locating faults, particularly where integrated circuits are used. See chapter 6 for this information.

9.7.2. Power-up routine

When switching-on the instrument, note that the built-in microprocessor initiates an automatic test of a number of internal circuits including:

- Start test
- PROM test
- LED display test
- RAM test

The sequence and explanation of this power-up routine is as follows:

a) Start test

- Check that about 2 seconds after switching on, pilot lamps REMOTE, RUN, and NOT TRIG'D are ON
- Check that all other pilot lamps and scale lamps are OFF.

This is a visual check only. After this, the next test starts directly.

b) PROM test

This is a check-sum test of all the internal PROM circuits. PROMs 1 to 4 are checked in turn starting with PROM 1.

PROM 1

DISPLAY		SELECT
●	ACCU	●
○	STO1	○
○	STO2	○
○	STO3	○

- Check that the ACCU display and select lamps switch ON.

If a fault is found the test sequence stops and no other test is made.
When no fault is found, the next test starts

PROM 2

DISPLAY		SELECT
●	ACCU	●
●	STO 1	●
○	STO 2	○
○	STO 3	○

- Check that the STO1 display and select lamps also switch ON.

If a fault is found the test sequence stops and no other test is made.
Following a valid test result, the next test starts.

PROM 3

DISPLAY		SELECT
●	ACCU	●
●	STO 1	●
●	STO 2	●
○	STO 3	○

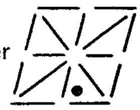
- Check that the STO2 display and select lamps also switch ON.

If a fault is found the test sequence stops and no other test is made.
Following a valid test result, the last PROM test starts.

PROM 4	DISPLAY		SELECT
	●	ACCU	●
	●	STO1	●
	●	STO2	●
	●	STO3	●

– Check that the STO3 display and select lamps also switch ON.

If a fault is found the test sequence stops and no other test is made.
Following a valid test result, the RAM test will start.

c) LED-display test
Each segment of all the LED-display sections will be switched ON, so that the character  will be shown in every section.

All the pilot lamps and scale lamps on the front panel will be switched ON. In this way, the LED-displays and the indicator lamps can be visually checked.
After about 3 seconds the next test is executed.

d) RAM test
This test checks only the micro-processor RAM and not the RAM memories ACCU, STO1, STO2 and STO3.
The RAM part, of which the contents may be destroyed, is now checked by writing and reading a particular pattern.
If a fault is found, the system will stop. If no fault is detected, this RAM part will be cleared.
The RAM part, in which the settings of the channel A and channel B AMPL/DIV switches, the TIME/DIV switch and the trigger delay and their check-sums are stored, may not be destroyed when using the battery back-up facility.
This RAM part will be check-sum tested (in the same way as the PROMS), and cleared when a fault is found (NOP will then be displayed in the alpha-numeric display).

Summary: If the tested circuits are working correctly, all tests will run through in an uninterrupted sequence and after the last test the instrument is ready for use.
In the event of a fault, the test sequence will stop at the point of fault detection.
The test sequence will still continue if a failure occur in one of the pilot lamps or in the alpha-numeric displays.

9.7.3. Trouble shooting aids

Print lay-out and circuit diagrams

The instrument contains a number of functional units. For each of these units a complete detailed circuit diagram and a complete detailed print lay-out drawing is given.

Printed-circuit board lay-out drawings are printed on foldout pages on the left and circuit diagrams are printed on foldout pages on the right, next to each other.
These drawings are located behind the detailed circuit description of the relevant unit.

Electrical values or types of the used components or the component item numbers are shown on the circuit diagram. For the used types of integrated circuits a table is provided.

Each component which is shown on the circuit diagram is marked on the print lay-out drawing by its item number.

Red symbols ▽ on the circuit diagrams are indicating the testpoints which are available on the circuit boards.

Red symbols ○ on the circuit diagrams are indicating all the adjusting elements.

Red symbols □ on the circuit diagrams are giving additional information.

For each integrated circuit and for all the connectors and transformers the pin configuration is given on the circuit diagram.

On the left side of the circuit diagram a part of the print connector is drawn which is giving the connector pin numbers of the incoming signals.
The part of the connector with the outgoing signals and their connector numbers is drawn on the right side of the circuit diagram.

Circuit description

Circuit descriptions (section 6) can be found in the manual in unit number sequence.
Each circuit description gives not only the explanation of the working principle of the unit but also a list of signal denominations and origines and destinations. Furthermore a number of timing diagrams are available.

Locations of adjusting elements

Drawings in section 8 "CHECKING AND ADJUSTING" show the locations of the different adjusting elements to locate these elements rapidly.

I/O addresses

The address codes for the input ports and the output ports are written in the circuit diagrams in hexadecimal notation. They can be found near to the I/O port circuitries.

9.7.4. Service faultfinding software routines

To facilitate fault finding the PM 3310 is provided with two internal service jumpers. These jumpers can select 3 service routines:

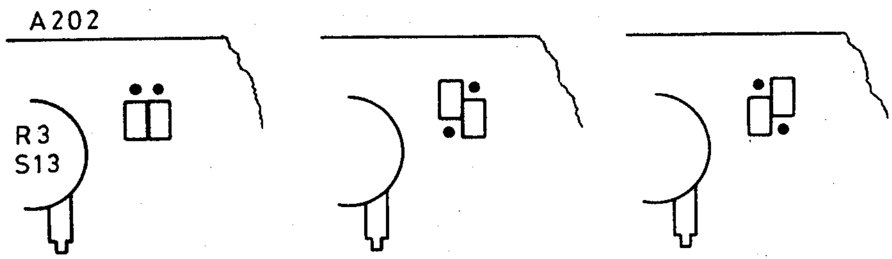
9.7.4.1. Interface test

9.7.4.2. Data-and address-bus test

9.7.4.3. Amplifier and time base setting test

The position of the jumpers, located at the component side of the switch board, is as follows:

Service routine 1 Service routine 2 Service routine 3



Rear view

Note 1: *A service routine can be called only after switching off-and-on the instrument.*

Note 2: *Both jumpers in upper position means normal operation*

Note 3: *Always set the INTENS control fully counter clockwise*

9.7.4.1. Interface test

This test is provided to check the interface functions of microprocessor unit A4. To make this test usefull, the user should know the principles of a microprocessor controlled system and the principles of the PM3310. To start this test, the jumpers at the rear side of the switch board must be set as indicated in the figure at chapter 9-7-4, and afterwards switch-on the instrument again.
The following listing indicates the test sequence, which is executed approximately every 325 μs.

- All alpha-numeric displays are filled with "1"
- To trigger the measuring oscilloscope the SOD pulse at X418 of unit A4 gets active once per cycle
- The pattern AA_H ($1010\ 1010_2$) is written into the output ports:

	D2424, D2426, D2427	(unit A21)
	D1326	(unit A13)
	D414	(unit A4)
and into the counters	D1308 and D1309, D1311 and D1312	(unit A13)
and into the DAC	D1327	(unit A13)

- The pattern $3F_H$ ($0011\ 1111_2$) is written into the first address of the ACCU-RAM D601 and D602 (unit A6)
- The TBS pulse is set to 25 kHz by setting $A1_H$ ($1010\ 0001_2$) into output port D1221
- The pattern $3F_H$ ($0011\ 1111_2$) is read out of the ACCU D601 and D602 (unit 6) and written into output port D201.
  This results in lighting of the following scale-and pilot lamps: UNCAL A and B; NOT TRIGD'D RUN and the six scale lamps of the A and B AMPL/DIV switches and the TIME/DIV switch.
- The position of the pushbutton switches DISPLAY are copied to the corresponding SELECT pilot lamps.
- The position of the push-pull-switches INVERT are copied to the corresponding DISPLAY pilot lamps.

NOTE: *The ACCU DISPLAY pilot lamp can be tested by the AUTO or DC/AC triggering switches.*
DC or AC: ACCU DISPLAY pilot lamp ON.
AUTO : ACCU DISPLAY pilot lamp OFF.

9.7.4.2. Address and data bus test

This test is provided to check the data-and address bus. To start this test the jumpers at the rear side of the switch board must be set as indicated in the figure at chapter 9.7.4., and afterwards switch-on the instument again.
The following listing indicates the test sequence, which is repeated every 3.8 ms.

- All alpha numeric displays shows "2"
- The patterns

01_H	($0000\ 0001_2$)
02_H	($0000\ 0010_2$)
04_H	($0000\ 0100_2$)
08_H	($0000\ 1000_2$)
10_H	($0001\ 0000_2$)
20_H	($0010\ 0000_2$)
40_H	($0100\ 0000_2$)
80_H	($10000\ 000_2$)

  are written sequential into the data-ram D601 and D602.
- The above patterns are read out of the data-ram. If the data bus is incorrect the NOT TRIG'D pilot lamp will light. If the data bus is correct the next step is carried out.
- The data Ø Ø H upto and included FFH are written in the data ram on the addresses C Ø Ø Ø H upto and included C Ø FFH.
- The above data are read out of the data ram.
  If the address bus is incorrect the REMOTE pilot lamp will light. If the address bus is correct the test will start again.

9.7.4.3. Front panel switch setting test

This test is provided to copy the settings of the front panel switches (except for the trigger mode and trigger source switches) to the output ports contineously.
Now easy checking of switches, interconnections and output ports is possible.
To start this test, the jumpers at the rear side of the switch board must be set as indicated in the figure of chapter 9.7.4. and afterwards switch-on the instrument again.
The following listing indicates the test sequence:

- All alpha numeric displays are filled with "3"
- The front panel settings are compared and copied into the output ports:

  D2424
  D2426
  D2427
  D1221

- The test repetition time is about 1 ms

9.7.5. Trouble-shooting hints

If a fault appears, the following test sequence can be used to find the defective circuit part:

- Check if the settings of the controls of the oscilloscope are correct. Consult the operating instructions in this manual.
- Check the equipment to which the oscilloscope is connected and the interconnection cables.
- Check if the oscilloscope is well-calibrated. If not refer to section 8 (checking and adjusting).
- Visually check the part of the oscilloscope in which the fault is suspected. In this way, it is possible to find faults such as bad soldering connections, bad interconnection plugs and wires, damaged components or transistors and IC's that are not correctly plugged into their sockets.
- Location of the circuit part in which the fault is suspected: the symptom often indicates this part of the circuit. If the power supply is defective the symptom will appear in several circuit parts.

After having carried out the previous steps, individual components in the suspected circuit parts must be examined:

- Transistors and diodes. Check the voltage between base and emitter (0,7 Volt approx. in conductive state) and the voltage between collector and emitter (0.2 Volt approx. in saturation) with a voltmeter or oscilloscope. When removed from the p.c.b. it is possible to test the transistor with an ohmmeter since the base/emitter and base/collector junctions can be regarded as diodes. Like a normal diode, the resistance is very high in one direction and low in the other direction. When measuring take care that the current from the ohmmeter does not damage the component under test.
  Replace the suspected component by a new one if you are sure that the circuit is not in such a condition that the new one will be damaged.
- Integrated circuits. In circuit testing can be done with an oscilloscope or voltmeter. A good knowledge of the circuit part under test is essential. Therefore first read the circuit description in section 6.
- Capacitors. Leakage can be traced with an ohmmeter adjusted to the highest resistance range. When testing take care of polarity and maximum allowed voltage. An open capacitor can be checked if the response for AC signals is observed. Also a capacitance meter can be used: compare the measured value with value and tolerance indicated in the parts list.
- Resistors. Can be checked with an ohmmeter after having unsoldered one side of the resistor from the p.c.b. Compare the measured value with value and tolerance indicated in the parts list.
- Coils and transformers. An ohmmeter can be used for tracing an open circuit. Shorted or partially shorted windings can be found by checking the wave-form response when HF signals are passed through the circuit. Also an inductance meter can be used.
- Data latches. To measure on inputs and outputs of data latches a measuring oscilloscope can be triggered by the clock signal which is connected to the clock input of the data latch.
  Check the input data lines one by one during the active edge of the clock signal.
  This measurement can only be done in this way when there is an acceptable repetition time of the clock signal. A too low clockpulse repetition time results in a low intensity of the trace on the C.R.T. screen of the measuring oscilloscope.
  The outputs can easily be checked for correct data by an oscilloscope or voltmeter

Oscilloscope checking of micro-processor bus signals

The 8085 micro-processor (D408) is provided with the following busses:
- Address bus
- Data bus
- Control bus

In general, if signals on these bus lines are checked with an oscilloscope, a very unstable display will be the result.
This is due to the fact that these signals vary with time in a rather unpredictable way.
If anyhow a stable display of signals from one of these busses is obtained, this may be an indication that the micro-processor runs in a small program loop.

Note: *Note:*

If a component must be replaced always use a direct-replacement. If not available use an equivalent after carefully checking that it does not degrade the instrument's performance. See also section 9.1. (replacement).
After replacement of a component the calibration of the instrument may be affected due to component tolerances. If necessary do the required adjustments.

Most of the test measurements can be carried out with a 2-channel oscilloscope and a voltmeter.
Use of a 4-channel oscilloscope with delayed time-base (e.g. PM 3244 or PM 3264) is recommended.
A number of measurements can also be done with a correct triggered logic analyzer.
Probes must be earthed near to the measuring points.

9.7.6. Overall view of provisions and service methods especially for fault location in various digital circuitries of the instrument.

FRONT BOARD A201

The data to be displayed in the alphanumeric displays and the pilot lamps can be measured in the following way:

Pilot lamps

Trigger an oscilloscope with the clock signal on point 11 of the relevant latch D201 or D202 and check the data lines D0 ... D7 one by one during the positive going edge of the clock signal.
The data outputs can easily be checked for correct data by an oscilloscope or voltmeter.

Alphanumeric displays

Trigger the main time-base of an oscilloscope externally with the "DELAY LOOP TRIGGER" which is available on test point X412 of unit A4.
Connect the signal $\overline{\text{IOA}}$ on point C21 of connector X424 on unit A4, with channel A of the oscilloscope and set the TIME/DIV switch to 0.2 ms/div.
A group of 16 negative going $\overline{\text{IOA}}$ pulses is displayed now.
Select this group of 16 pulses with the aid of the delayed time-base in such a way that a triggered display of 16 pulses divided over the whole ten divisions of the screen is obtained.
The first $\overline{\text{IOA}}$ pulse belongs to address 80A0H and the last $\overline{\text{IOA}}$ pulse belongs to address 80AFH.
By connecting the data lines D0 ... D7 one by one to the B channel of the oscilloscope the data can be checked.

Set the oscilloscope for this check in ALT-mode and use the TBMAGN and XPOSITION controls.

SWITCH BOARD A202

For measuring on the switch board the instrument has to be set in the SERVICE ROUTINE NUMBER 3 (page 9-16) with the jumpers on unit A202.

Switches

The output signals of the front panel switches can be measured with a normal voltmeter on the CIS connectors or the input of the multiplexer's D241-D242-D243-D247-D248 and D249.
Signals can be checked while operating the relevant switches.

Multiplexers

Trigger the MAIN TIME-BASE of a dual channel oscilloscope with one of the signals $\overline{\text{RDF0}}$ - $\overline{\text{RDF2}}$ or $\overline{\text{RDF4}}$ connected to the channel A input.
RDF0 is available on testpoint X246 on unit A202
RDF2 is available on testpoint X244 on unit A202
RDF4 is available on testpoint X243 on unit A202
Set the measuring oscilloscope in 5 μs/div. - DC - TRIG - SLOPE "–" and correct LEVEL.

Connect the data lines D0 ... D7 one by one to the channel B input and check the data during the positive going edges of the trigger signal on channel A when operating the relevant front panel switches.

MICROPROCESSOR UNIT A4

Every ≈ 20 ms a number of trigger pulses are generated by the software for test purposes.
- Trigger pulse "START MAINLOOP" is available at X407.
- Trigger pulse "START DISPLAY LOOP" is available at X409.
- Trigger pulse "START DELAY LOOP" is available at X412.

Latches and bidirectional buffer D413 - D414 - D416 and D417 are placed in sockets and can be easily removed from the unit for test purposes.
- Removing D413 results in disconnecting the internal address bus from the internal address/data bus.
- Removing D414 results in disconnecting the output port from the system.

– Removing D416 results in disconnecting the system address bus from the internal address/data bus.
– Removing D417 results in disconnecting the system data bus from the internal address/data bus.

This can for example be used to separate and locate the fault in case of a short-circuit in one of the busses.

The unit contains a number of soldering spots with the following functions:

– Signal RST 7.5 can be connected to the +5 V for test purposes.
  This is not of interest for servicing in standard instruments.
– PROM address line A11* can be disconnected from the +5 V and connected to address line A11 from the microprocessor.
  This is necessary in case the IEC option PM 3325 is used because of the use of a PROM circuit D407 of 4096 x 8 bits.
– For test purposes the $\overline{\text{RESIN}}$ input circuit (watchdog circuit) can be replaced by a simple reset circuit with C411.
– The TRAP input circuitry can be made inactive for service purposes.

To measure the signals ZEN - INV and CLDT, the measuring oscilloscope must be triggered with the signal on X407 (START MAINLOOP).

– ZEN can be checked by operating the front panel display select switches.
– INV can be checked by operating the front panel invert switches for STO1-2 and 3.

The input data lines for the latch D414 can be measured with the method described in section 9.7.5.

Fault finding method

– Check supply voltages.
– Check whether the "START MAIN LOOP" trigger is present once every 20 msec at testpoint X407 on unit A4 or not.
– Check if the μP is switched in the HOLD-state. $\overline{\text{RD}}$ and $\overline{\text{WR}}$ are then switched to about 1.5 V (can be done via input TRAP for example).

– Disconnect TRAP input (solder spot).
– Disconnect the WATCHDOG circuit and connect C411 to $\overline{\text{RESIN}}$ (solder spot).
– Replace eventually the μP itself.
– Replace eventually the PROM circuits.
– Check the busses for short circuits or interrupts. For this, latches and bidirectional buffers can be removed from their sockets.

After the repair everything must be brought in the normal position again.

RAM UNIT A6

Tri-state buffer D617 can be removed from its socket so that no data can be placed on the system data bus by the RAM unit.

BUFFER UNIT A7

A solder spot is available in the CLKSH circuitry for test purposes. So a CLKSH can be derived from signal C4 which is generated during the time that the ADC output is placed on the ADC bus. The ADC output contents can then directly be placed in the shift register without correction.

Using this facility in combination with the interruption of signal line DAC M-1, results in the switching off of the total correction circuitry.

After the repair everything must be brought in the normal position again.

TIME-BASE UNIT A12

For test purposes in ROLL-mode, the ROLL-mode action can be done 5000 times faster by placing jumper S1201 in the left position.

Check for correct time-base setting

Select service test routine number 3.
The TIME/DIV switch position is now read by the microprocessor and this processor in turn will set the belonging code (according to the table on page 6-136) on the data lines D0 ... D7 so that it can be latched by latch D1221 on unit A12.

These codes can be measured on the inputs of latch D1221 by triggering a monitor oscilloscope with the clock signal on D1221-pt. 11. Now the data lines can be observed one by one during the active edge of the clock signal. Codes on the outputs of the latch can be measured with a voltmeter or an oscilloscope.

In this way the correct functioning of the TIME/DIV switch, the microprocessor and the latch D1221 can be checked for RECURR-mode as well as for ROLL-mode. (In ROLL-mode D5 will steady be "0") and different TIME/DIV switch positions.
Now all the dividers and multiplexers can be checked for all the TIME/DIV switch positions in a simple way.

ROLL-mode check 0.5 s/div ... 60 min/div

- Depress pushbutton ROLL.
- Set jumper S1201 in the left position.
- Measure the TBS signal on D1219 - point 7 with an oscilloscope and check the signal repetition time in accordance with the table below.

TIME/DIV switch setting	Signal repetition time
60 min/div	28,80 ms
30 min/div	14,40 ms
15 min/div	7.20 ms
6 min/div	2.88 ms
2 min/div	0.96 ms
1 min/div	0.48 ms
0.5 min/div	0.24 ms
20 s/div	160 µs
10 s/div	80 µs
5 s/div	40 µs
2 s/div	16 µs
1 s/div	8 µs
0.5 s/div	4 µs

- Set the jumper S1201 again in the right position.

RECURR-mode check 0.2 s/div ... 0.5 ms/div

- Depress pushbutton RECURR.
- Measure the TBS signal on D1219 - point 7 with an oscilloscope and check the signal repetition time in accordance with the table below.

TIME/DIV switch setting	Signal repetition time
0.2 s/div	8 ms
0.1 s/div	4 ms
50 ms/div	2 ms
20 ms/div	800 µs
10 ms/div	400 µs
5 ms/div	200 µs
2 ms/div	80 µs
1 ms/div	40 µs
0.5 ms/div	20 µs

RECURR-mode check 0.2 ms/div ... 0.5 μs/div

- Depress pushbutton RECURR.
- Measure the TBF signal on X1206 in accordance with the table below.

TIME/DIV switch position	Signal repetition time
0.2 ms/div	8 μs
0.1 ms/div	4 μs
50 μs/div	2 μs
20 μs/div	0.8 μs
10 μs/div	0.4 μs
5 μs/div	0.2 μs
2 μs/div	0.08 μs
1 μs/div	0.04 μs
0.5 μs/div	0.02 μs

DELAY TRIGGER UNIT A13

There are two solder spots available on the unit. One to invert the PENLIFT output signal and a solder spot to connect the input trigger TRIST directly with the output signal line DELTRG.
In this way the whole delayed trigger circuit is switched off, and the trigger point is at the right-hand side of the CRT screen.

Check for correct latch, delay counter and DAC delay setting

The input data lines for the latch D1326, the counters D1308 - D1309 - D1311 and D1312 and the DAC DELAY D1327 can be measured with the method described in section 9.7.5.

Trigger signals

D1324 - pt. 8	for data latch D1326
D1324 - pt. 6	for MSB of delay counter
D1324 - pt. 12	for LSB of delay counter and for DAC DELAY

The delay counter (used in D- and P-mode) is set according to the formula:

$$\text{Counter setting} = \{(10+N) * 5+8\}$$

In this formula N is the number of divisions set by the user ($-9 \leqslant N \leqslant 9999$).
Note that the four least significant bits the inverted information is placed on the data bus.

The DAC DELAY (used in S-mode) is set in the following way:

$$\text{DAC DELAY setting} = 2 * N$$

N is the number of divisions set by the user ($0 \leqslant N \leqslant 100$)

DC POWER SUPPLY A15

Dummy load for PM 3310 power supply

Voltage	Load resistance	
– 12 V	15.6 Ω	(3 x 47 Ω //)
+ 12 V	15.6 Ω	(3 x 47 Ω //)
– 6 V	40 Ω	(47 Ω // 220 Ω)
+ 6 V	40 Ω	(47 Ω // 220 Ω)
– 5.2 V	5 Ω	(2 x 10 Ω //)
+ 5 V	2.5 Ω	(4 x 10 Ω //)
+ 40 V	300 Ω	
–125 V	10 kΩ	
+125 V	10 kΩ	

INPUT AMPLIFIER UNIT A21

Check for correct latch setting

The input data lines for the latches D2424 - D2426 and D2427 can be measured with the method described in section 9.7.5.

Multiplexer check

Trigger the MAIN-TIME-BASE of a dual channel oscilloscope with the external trigger signal "MAIN LOOP TRIGGER" which is available on testpoint X407 on unit A4.
Connect the signal on point 6 of D2423 on unit 21 with the channel A of the oscilloscope and set the TIME/DIV switch to 20 μs/div.
Two negative going pulses are displayed now.
Select these two pulses with the aid of the delayed time-base in such a way that a triggered display of these two pulses is obtained.
During the first pulse multiplexers D2418 and D2419 are set to the "T" position and during the second pulse they are set to the "1" position.
By connecting the data lines D0 ... D7 one by one to the B channel of the oscilloscope the data can be checked.

10. INTRODUCTION TO MICROPROCESSORS

10.1. A BRIEF ENCOUNTER

Microcomputers, like people, do not reveal all their secrets at a brief encounter. If this is your first introduction to a microcomputer, you will need a little time to familiarise yourself with its characteristics – what it can do, how it does it and how its facilities are best used to advantage.

As its name implies, a microcomputer is an extremely small device.
Extremely small because it is based on a silicon-chip microprocessor.

The great future predicted for the microprocessor lies in its *enormous work capacity* for processing signals, available within *negligible physical capacity.*

The human brain has the ability to determine by calculation in a more sophisticated way, but our microcomputer, with its built-in 'one-track' mind, is capable of much faster calculation speeds. Also the computer facilities extend beyond the confines of the brain and memory to perform some of the functions we allocate to other parts – the eyes, ears, arms and legs.

Besides the ability to store and manipulate information, the microprocessor circuits are capable of recognising visual, aural and physical conditions, evaluating them and presenting them in a form required by an instrument or operator. A practical application of this could be the monitoring of strain-gauges or thermometers in an industrial process at regular intervals and the recording of the values, together with any alarm conditions, on a print-out. In contrast to this data logging function, the microcomputer could be an integral part of a laboratory measuring instrument; e.g. a digital oscilloscope, for control, storage and read-out purposes.
Microcomputers are designed with built-in flexibility to enable them to be used for a wide variety of applications. This versatility is obtained in the signal conditioning circuits that present the data to the computer central processing unit in a form that it can readily understand. In electronics, the simplest and most reliably defined condition is when a circuit is either switched on or switched off. This two-state notation of defining the numerical terms of a problem is universally used in computers and is known as the binary system.

10.2. COMING TO TERMS

After a general picture of the microcomputer field, it is useful to look a little closer at the practical aspects and to discuss some of the terms that are in everyday use.

Microcomputer	A miniature electronic system that performs arithmetic and logic operations on data according to a programmed sequence of instructions stored in a memory. As a calculating system, the microcomputer consists not only of the physical components (the hardware) but also of program instructions (the software).
Hardware	The mechanical, electronic and electromechanical components of the computer system.
Software	The programmer's language for communicating with the computer. This includes sets of programs translated into binary form to enable the computer to perform specific functions as required by the system user.

Microprocessor CPU	The heart of the microcomputer, the central processing unit (CPU) that performs all the functions as arithmetic and logic operations that are written in the system software program. In addition to the Arithmetic and Logic Unit (ALU) it also contains a Control Block and Register Array.
Memory	A high-speed electronic device in which data and instructions are stored for subsequent processing.
Input/Output	Devices that provide communication between the microcomputer system and the outside world. For example, interfacing input data and instructions via a keyboard and outputting results via a display unit or printer.
Instruction set	A set of characters that define an operation with generally one or more addresses, which are given via the input device and can be stored in the memory. When a program is running, data-words are processed in a sequence and manner as specified by the instructions, the results being stored and/or outputted via an output device.
Data word	A word, or group of binary digits (bits) used to encode data, as distinct from an instruction word. A byte is a word of 8 bits.
Binary notation	A system of numbering used in computers that uses 2 as a base in contrast with the normally used decimal system that has 10 as a base. Only two symbols are required in the binary system, 0 and 1, which can be conveniently represented in electronic circuits as two voltage levels in a signal. The binary equivalents of the decimal numbers 0 to 10 are as follows:

DECIMAL		BINARY
0	=	0000
1	=	0001
2	=	0010
3	=	0011
4	=	0100
5	=	0101
6	=	0110
7	=	0111
8	=	1000
9	=	1001
10	=	1010

Addition:

DECIMAL	BINARY
5	0101
+9	+1001
14	1110

To add binary numbers, proceed as in decimal but remember that the radix is 2. i.e. carry 1 when 2 is reached.

Hexadecimal notation

Using 16 as a base this system provides a short-band method of writing 4-bit binary numbers with alphanumeric symbols. This is useful for a data-word grouped as a 4-bit field, where there are 16 combinations.

COMBINATION	BINARY CODE	HEXADECIMAL CODE
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F

Analog-to-Digital Converter

Enables physical or electrical input signals that are in analog form to be converted to digital form for processing in the computer.

Register

Consists of a group of two-state flip-flops, which by means of a clock-pulse command can store the data-word present on its input lines.
The output lines remain stable until a new data-word is clocked into the register. A group of registers forms a memory.

Data-bus

Enables several circuits to communicate with each other without the need for separate data paths. This databus is common to all circuits and a timing and control circuit organises which circuits use the databus at any particular time, in conjunction with an ADDRESS-BUS and a CONTROL-BUS.

Address-bus

Enables memory locations to be addressed by their unique device numbers.

Control-bus

Controls the exact timing of the communication on the data-bus and also the direction of data flow.

10.3. SYSTEM FEATURES

With a basic understanding of the language and hardware component parts of a microcomputer it is interesting to discover how these can be integrated to form an organised system. The following illustrations show the basic system features which, for greater comprehension, should be studied with reference to the computer terms that have been previously defined.

Basic features

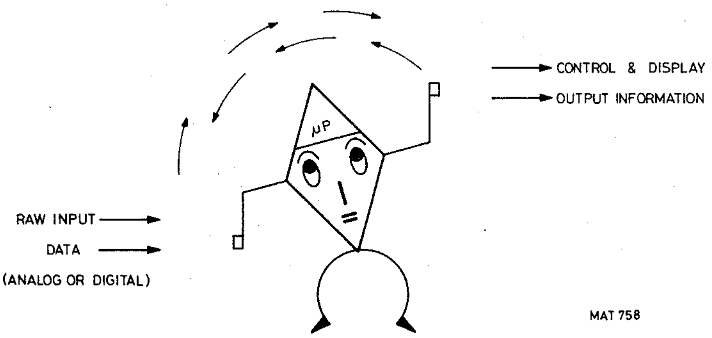


Fig. 10.3.1.

In simple terms, our Master Microcomputer takes data with one hand, juggles with it, and hands it out with the other. Being highly intelligent, its right hand definitely knows what its left hand is doing!

Input features

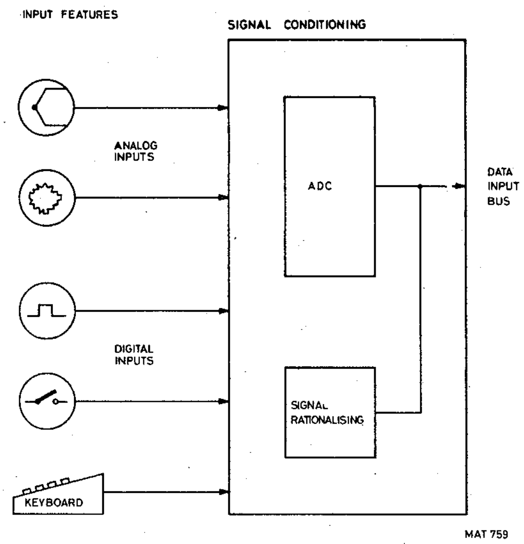


Fig. 10.3.2.

The raw inputs from analog sources such as thermocouples, strain-gauges voltage and current devices, etc., must first be converted to the digital form required by an ADC in the signal conditioning part of the microcomputer.
Digital inputs from switch contacts, logic levels from sold-state devices or from counters, etc., must be converted to the correct logic levels within the signal conditioning part.

Output features

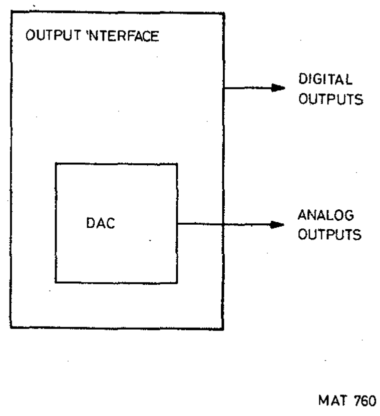


Fig. 10.3.3.

The output interface circuits are designed to present the output data in a form suitable for the various system requirements, e.g. digital displays, print-outs, parallel and serial interfaces, alarms, etc. When analog output signals are required, digital-to-analog conversion (DAC) is performed in the computer output interface circuits.

Memory features

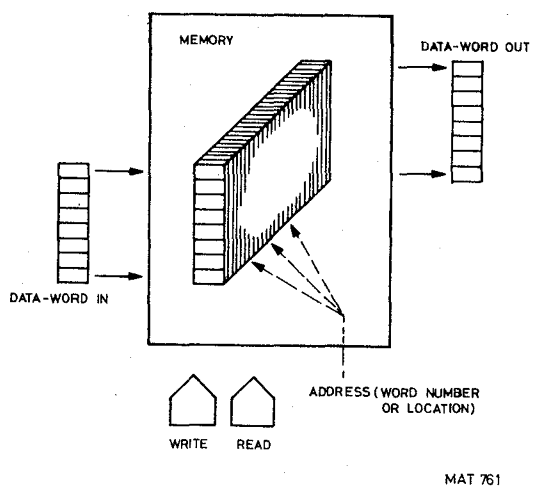


Fig. 10.3.4.

A memory is simply a group of registers used for storing data-words, for future retrieval when required. With a WRITE pulse, a data-word can be stored; a READ pulse enables a data-word to be read out of a location.
An ADDRESS must be provided with the READ and WRITE pulses to locate the specified data-word.
Memories can be used for storing signal data or for programming instructions. Instruction sets for microcomputers are usually stored in read-only memories, ROMs or PROMs (Program Read Only Memories).

The memory contains not only the information to tell the microprocessor what to do, but also the instructions on how to do it.
Variable data are usually stored in random-access memories, RAMs.

Microprocessor features

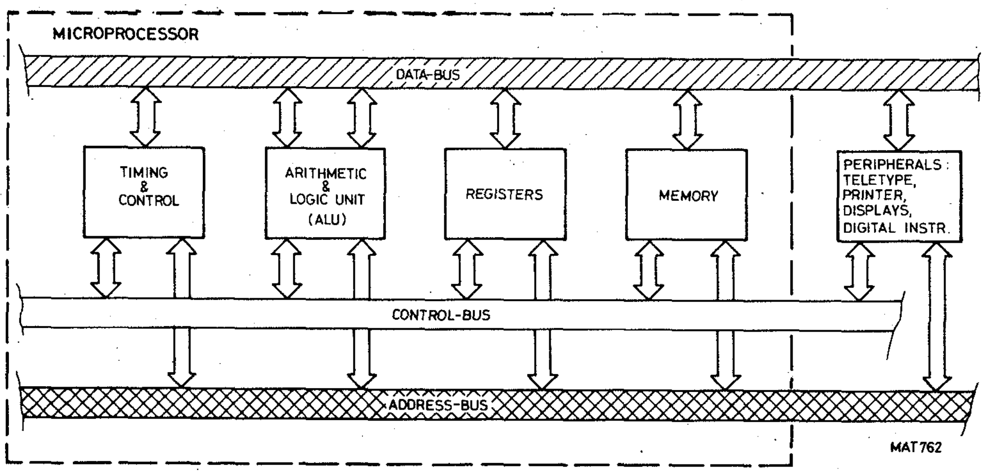


Fig. 10.3.5.

The elementary circuits of a microcomputer comprise:
- registers
- a memory (ROM + RAM)
- a data-bus, control-bus and address-bus
- a data-bus, timer and controller circuit
- an arithmetic and logic unit (ALU)

If the integrated circuit contains no memory, or only a limited memory, we refer to this as a microprocessor. The microcomputer, together with its memory and the peripheral equipment constitute the hardware of the system.

Programming features

In order to perform meaningful operations with the hardware of a computer system, we need to specify precisely:
- what OPERATIONS are required upon a defined DATA-WORD
- in what SEQUENCE these will occur
- to which LOCATION the results of the operation have to be deposited.

This process of prescribing the necessary actions within a computer system is called PROGRAMMING the computer software.
Programming consists of the sequential execution of the instructions stored in the memory, under the control of the TIMING and CONTROL part. Its circuits decode the instruction and initiate the necessary data-word transports and operations.
A basic flow-chart cycle for each instruction is as follows:

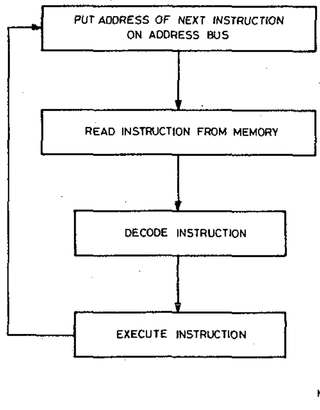


Fig. 10.3.6.

A PROGRAM COUNTER is a special register equipped to increment the address of sequential instructions to enable new instructions to be FETCHED from the memory. As the program counter is connected to the data-bus, the contents can be replaced by other values to permit a JUMP to an instruction elsewhere in the memory.

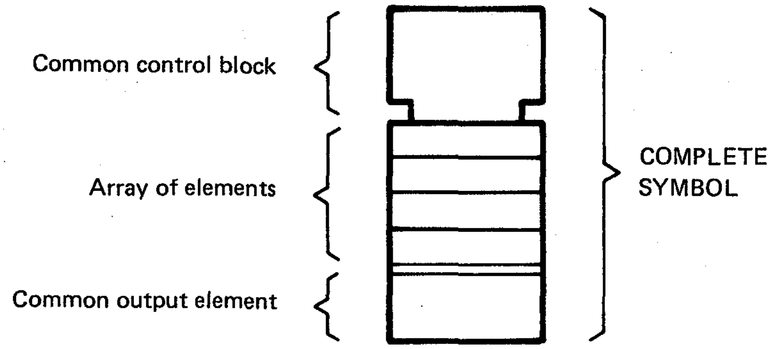
As the execution of an instruction consists of a number of sub-steps, it is useful to be able to store an instruction temporarily in a register if the next operation needs to use this result. The two operations are combined in a single register, called the ACCUMULATOR for ease of presentation to the ALU in the next instruction.
Apart from the memory, microcomputers usually have some general-purpose registers to store intermediate results on a temporary basis.

Note: *For more information refer to:*
"INTRODUCTION TO MICROPROCESSORS AND THEIR USE IN T&M INSTRUMENTS".
Ordering number: 9499 990 00711.

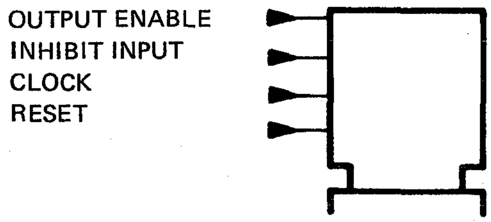
11. EXPLANATION OF USED SYMBOLS

I NTRODUCTION

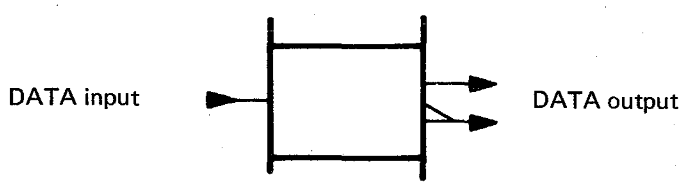
Common control block
The use of binary logic integrated circuits (M.S.I.'s) necessitated an abbreviated notation for the interdependency of various functions, as well as simplified symbols for complex functions.
The most important information is: which signals appear at the input and how the outputs behave with respect to the function of the IC.



Common control block
On the common control block, all **common** input lines are connected. These lines must have funtional relation to the other elements of the symbol. Examples: general reset, output enable, inhibit input, clock signal etc.

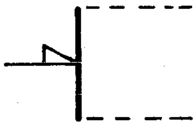
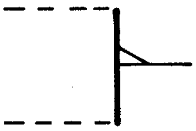
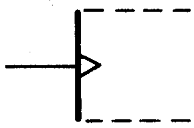
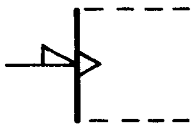
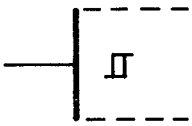
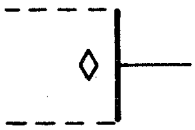
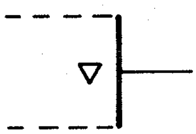
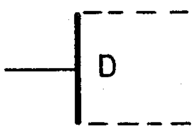
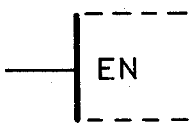


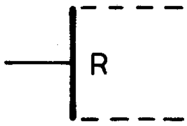
Array of elements
Each element of the array has its own in-and outputs. Example: it can be a D-flip-flop with one data input and two outputs (one inverted and the other not inverted).



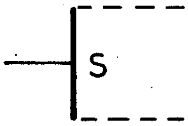
LIST OF CHARACTERS AND SYMBOLS

In the common control blocks, characters and symbols are used to indicate the function of the in-and outputs.

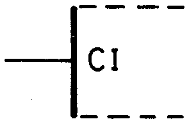
SYMBOL	DESCRIPTION
	Polarity indicator at input
	Polarity indicator at output
	Dynamic input
	Dynamic input with polarity indicator
	Schmitt - trigger input
	Open collector output
	Tri-state output
	D - input
	Enable input



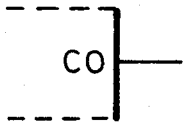
Forcing reset input



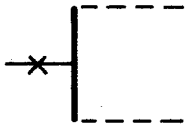
Forcing set input



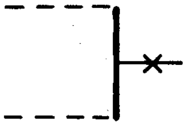
Carry input of an arithmetical element



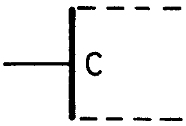
Carry output of an arithmetical element



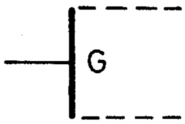
Line carrying no logic information (input)



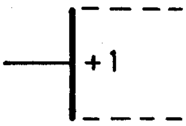
Line carrying no logic information (output)



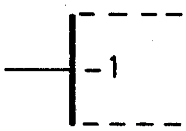
Clock input



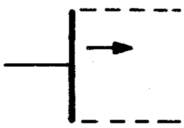
G – input implying an AND– relationship



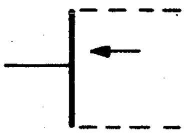
Count up command for counters



Count down command for counters

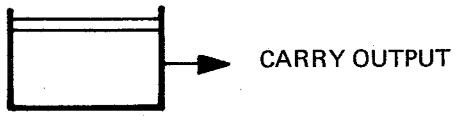


Shift right (down) command for shift register

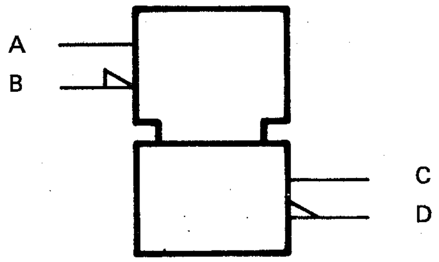


Shift left (up) command for shift register

Common output element
On the common output element the common or resulting outputs of the elements are drawn.
Example: it can be a carry or a borrow signal for a counter.

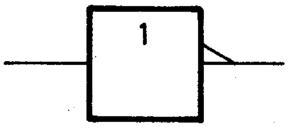


Input and output lines
Input lines are drawn at the left side of a symbol, output lines at the right side. In-and output lines can be drawn with and without as shown.

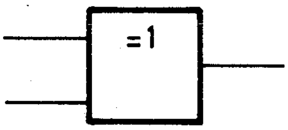


Meaning of the above-drawn lines A, B, C and D:
- Line A is active for the block when it is high ("1") and inactive when it is low ("0") .
- Line B is active for the block when it is low ("0") and inactive when it is high ("1").
- Line C is low ("0") in the rest state of the element or when output is inhibited. This output is then inactive.
- Line D is high ("1") in the rest state of the element or when output is inhibited. This output is then inactive.
- When line C is "high", this output is active.
- When line D is "low", this output is active.

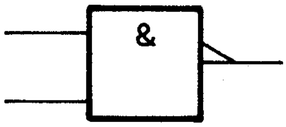
BASIC SYMBOLS



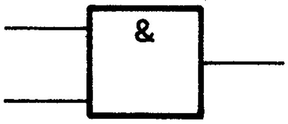
Inverter



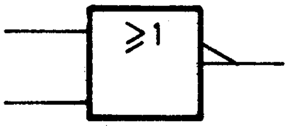
Exclusive – OR



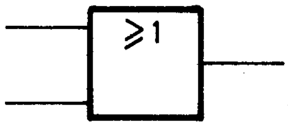
NAND (inverting AND)



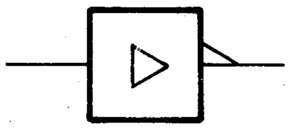
AND



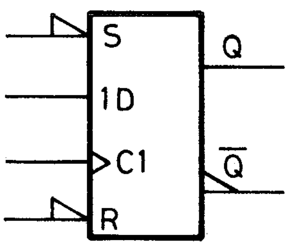
NOR (inverting OR)



OR



Inverting emitter – follower



D – type flip flop

DEPENDENCY NOTATION

1. Introduction

Dependency notation is a means of denoting the relationship between inputs, outputs and between inputs and outputs, without actually showing all the element and interconnections involved.

Apart from its use in complex element, dependency notation should not be used to replace the symbols for combinative elements.

The information provided by dependency notation **supplements** that provided by the qualifying symbol for an element's function.

In the convention for the dependency notation, use is made of the terms "affecting" and "affected". In the case where it is not evident which inputs must be considered as being the affecting or the effected ones (e.g. if they stand in an AND-relation), the choice may be made in any convenient way.

Ten different kinds of dependency have been defined.
They are:

A	ADDRESS	– dependency
C	CONTROL	– dependency
EN	ENABLE	– dependency
G	AND	– dependency
M	MODE	– dependency
N	NEGATE	– dependency
R	RESET	– dependency
S	SET	– dependency
V	OR	– dependency
Z	INTERCONNECTION	– dependency

Each dependency is represented by a capital letter or letter combination, as shown above.

AND–, OR– and NEGATE–dependencies are used to denote Boolean relationships between inputs and/or outputs. INTERCONNECTION-dependency is used to indicate that an input or output is connected to one or more inputs and/or outputs.

CONTROL–dependency is used to identify a timing-input or a clock-input of a sequential element and to indicate which inputs are controlled by it.
SET– and RESET–dependencies are used to specify the internal logic states of an RS bistable element in the case that the R– and S–inputs both stand at their internal 1–states.
ENABLE–dependency is used to identify an ENABLE–input and to indicate which inputs and/or outputs are controlled by it (e.g. which outputs take on their high impedance state).
MODE–dependency is used to identify an input which selects the mode of operation of an element and to indicate the inputs and or outputs depending on that mode.
ADDRESS–dependency is used to identify the ADDRESS inputs of a memory.

The table below lists the various dependencies and summarizes their effects. In this table the word "action" implies:

– that affected inputs will have their normally defined effect on the function of the element;

– that affected outputs will take on the internal logic states as determined by the function of the element.

2. Convention

a. Dependency notation usually defines relationships between internal logic states. However in the case of 3–state outputs and open circuit outputs, ENABLE–dependency defines relationship between the internal logic states of affecting inputs and the external states of affected outputs.

b. Application of dependency notation is accomplished by:
– labelling the affecting input or output with the relevant letter followed by an identifying number;
– labelling each input or output affected by that affecting input or output with that same number;
– labelling each input or output affected by the **negated** internal logic state of the affecting input or output with that same number with a bar over it.

c. If the affected input or output already has a label, denoting its function, this label must be prefixed by the identifying number of the affecting input.

d. If an input is affected by more than one affecting input or output, the identifying number of each of the affecting inputs or outputs shall appear in the label of the affected one, separated by commas. The normal reading order of these identifying numbers is the same as the sequence of the affecting ralationship.

e. Two affecting inputs labelled with different letters, must not have the same identifying number, unless when one of the letters is A.

f. If two affecting inputs or outputs have the same letter and the same identifying number, they stand in an OR–relation to each other.

g. If an affected input or output already has a label which would form an ambiguous combination with the identifying number, the latter must then be replaced by a different character (e.g. Greek letter) to avoid ambiguity.

h. An affecting input or output affects only the corresponding affected input or outputs of the element.

Type of dependency	Letter(s)	Effect on affected input or output if the affecting input stands at its internal 1–state	0–state
ADDRESS	A	permits action (address selected)	prevents action (address not selected)
CONTROL	C	permits action	prevents action
ENABLE	EN	permits action	– prevents action of affected inputs – imposes external high-impedance state on open-circuit and 3-state outputs (internal state of 3-state outputs unaffected) – imposes 0-state on other outputs
AND	G	permits action	imposes 0-state
MODE	M	permits action (mode selected)	prevents action (mode not selected)
NEGATE	N	complements state	no effect
RESET	R	affected output reacts as it would to S=0, R=1	no effect
SET	S	affected output reacts as it would to S=1, R=0	no effect
OR	V	imposes 1-state	permits action
INTERCONNECTION	Z	imposes 1-state	imposes 0-state

2.1. MECHANICAL PARTS

Item	Qty	Order number	Description	
1	1	5322 460 64042	Side profile left	
2	1	5322 447 94625	Side profile right	
3	2	5322 462 34199	Print support	
4	2	5322 528 34113	Arret for handle	
5	2	5322 447 94638	Cover top and bottom	
6	1	5322 815 22804	Cil bolt M4X6	
7	1	4822 505 10488	Square nut M4	
8	1	5322 532 14593	Washer 4. 3X12	
9	1	4822 530 80077	Spring washer 5,2	
10	1	5322 815 28054	Cil bolt M3X8	
11	1	4822 532 10332	Washer 3. 2X7	
12	1	4822 530 80173	Spring washer	
13	1	5322 462 54154	CRT shielding	
14	1	5322 492 64767	Clamping strip	
15	1	4822 502 10051	Cil bolt M4X20	
16	1	4822 505 10488	Square nut M4	
17	1	5322 466 64213	Plastic profile 30cm	
18	1	5322 256 64014	Battery holder	
19	1	5322 535 94978	Shaft assy	
20	1	5322 532 24398	Coupling	
21	2	4822 502 10668	Screw for coupling	
22	1	5322 455 84091	Textplate	
23	3	5322 414 34134	Knob dia 10	
24	3	5322 492 64337	Clamping spring knob	
25	9	5322 414 34091	Knob dia 10 shaft 6	
26	2	5322 414 34249	Attenuator knob assy	
27	1	5322 414 34261	Time/div knob assy	
28	3	5322 532 54478	Distance washer	Range indication instrument parts.
29	2	5322 462 44458	Housing	
30	2	5322 462 44459	Cover	
31	2	5322 492 54338	Compression spring	
32	2	5322 268 14157	Contact pin	
33	1	5322 466 85887	Cover for IEC conn.	
	1	5322 480 34074	Contrast filter acc.	
37	1	5322 466 74059	Bezel	
38	1	5322 480 34046	Contrast filter	
39	1	5322 447 94169	Front cover	
40	1	5322 447 94626	Top cover	
41	1	5322 466 64214	Adhesive strip	
42	1	5322 447 94627	Bottom cover	
43	1	5322 455 84092	Text strip	
44	1	5322 498 54042	Aluminium profile	
45	1	5322 498 54045	Plastic profile	
46	2	5322 535 74401	Locking pin	
47	2	5322 492 54155	Compression spring	
48	1	5322 498 54044	Bracket left	
49	1	5322 498 54043	Bracket right	
50	5	5322 414 74029	Knob cover blue + line	
51	7	5322 414 74015	Knob cover grey + line	
52	1	5322 414 74019	Knob cover grey	
53	2	5322 380 24089	Light reflector assy	
54	1	5322 290 64085	Soldering support	
55	1	5322 255 44088	Led holder	
56	1	5322 505 14184	Nut for cal terminal	

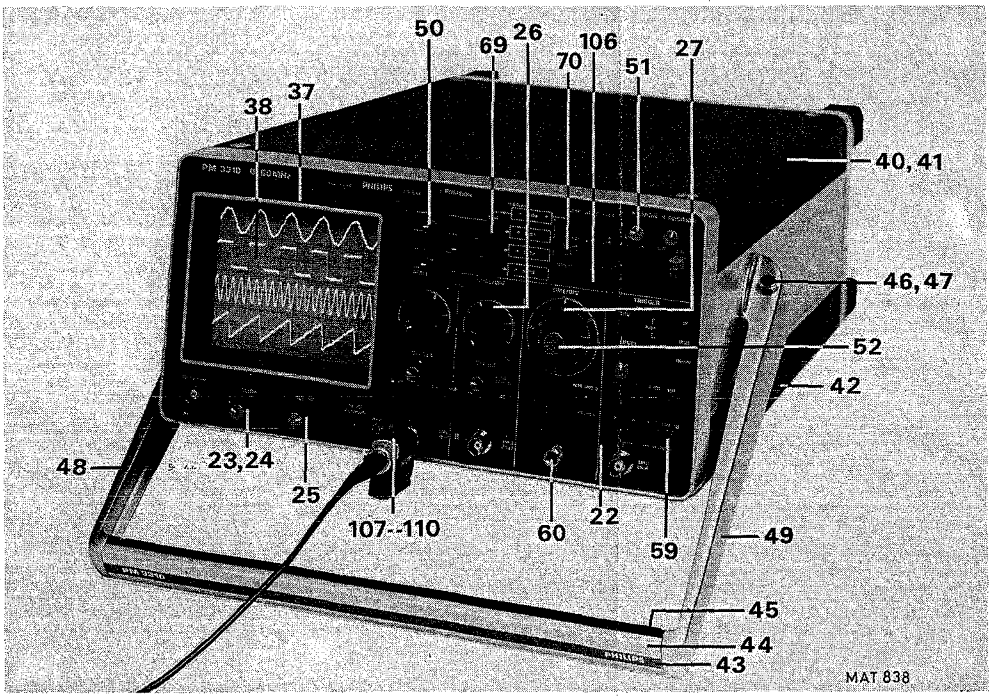


Fig. 12.1.3.

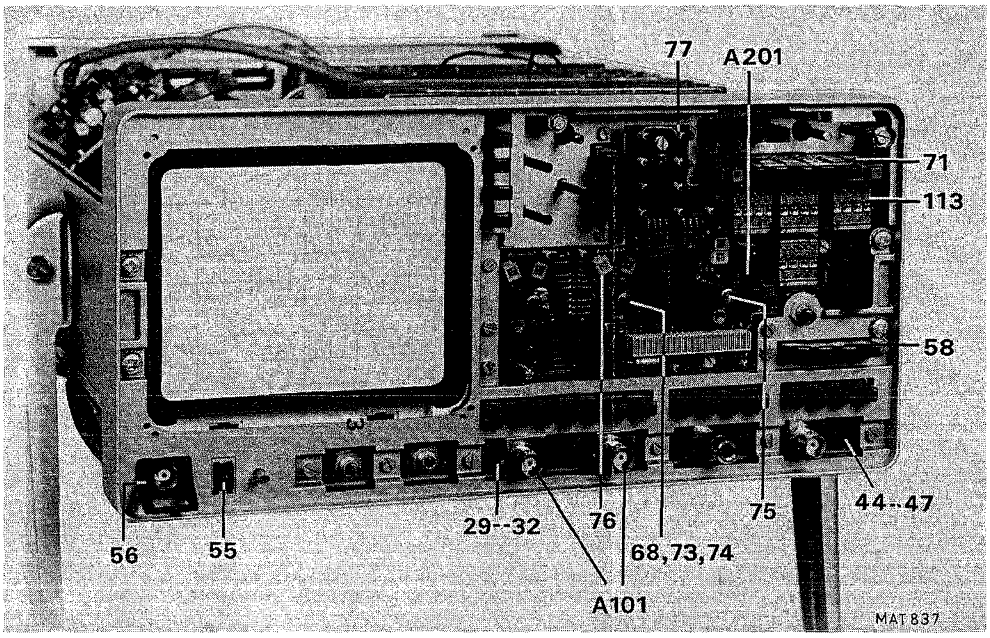


Fig. 12.1.4.

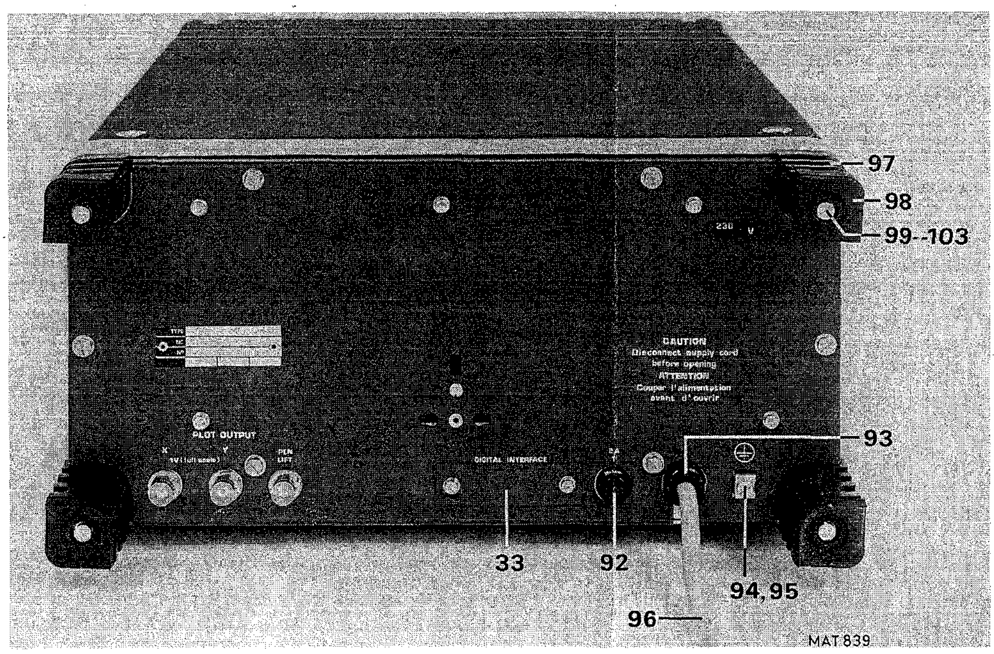


Fig. 12.1.5.

2.2.1. *Capacitors*

Type: FOIL 1 % 630 V

Item number	Ordering number	Value
C2923	5322 121 54228	390 pF
C2014	5322 121 54229	511 pF
C2027		
C2028		
C2041		
C2043		
C827	5322 121 54231	825 pF
C1317	4822 121 50591	1 nF
C1327		
C2007		

Type: FOIL 5 % 1500 V

Item	Ordering number	Value
C1602	5322 121 44333	12 nF
C1603		

Type: FOIL 10 % A = 100 V
B = 250 V
C = 400 V
D = 630 V
E = 1600 V

Item	Ordering number	Value	Type
C1541	5322 121 44201	10 nF	D
C1012	5322 121 44232	22 nF	C
C1013			
C1613			
C1614			
C2719			
C2414	4822 121 40407	22 nF	D
C2476			
C1543	5322 121 44025	33 nF	C
C1501	5322 121 44138	47 nF	B
C1538	5322 121 44137	68 nF	B
C1548			
C1618			
C2033			
C2039			
C1517	4822 121 40279	68 nF	D
C1519			
C1601			
C724	5322 121 40323	100 nF	A
C916			
C1328			
C1532			
C1546			
C1616			
C2467			
C2947			

Item	Qty	Order number	Description	
57	2	5322 255 24015	Lamp holder	
58	4	5322 535 84447	Extension part (01 version)	
58	4	5322 462 50215	Extension part (02 and up)	S29
59	4	5322 414 25613	Push button + green (01 version)	
59	4		Push button + green (02 and up)	
60	1	5322 505 14178	Knurled nut	
61	1	5322 466 85888	Locking plate	
62	1	5322 532 24579	Bush	
63	1	5322 532 14697	Washer	
64	1	5322 290 34022	Soldering tag	
65	1	5322 506 14001	Nut	
66	2	5322 505 14186	Nut	
67	2	5322 532 34124	Spacer	
68	2	5322 532 24374	Coupling R7-R8	
69	8	5322 414 14011	Push button grey (01 version)	
69	8		Push button grey (02 and up)	
70	2	5322 414 26019	Push button L. grey (01 version)	
70	2	5322 414 20002	Push button L. grey (02 and up)	
71	35	5322 535 84447	Extension part switch (01 version)	
71	35	5322 462 50215	Extension part switch (02 and up)	
72	6	5322 532 54492	Paper washer 2.2X5	
73	2	5322 278 74008	Arret for switch	
74	2	5322 535 94966	Inner shaft	
75	1	5322 278 74009	Arret for switch	
76	6	5322 255 34122	Lamp holder	
77	10	5322 532 60487	Ceramic spacer	
78	6	5322 255 44218	IC-FOOT 16 - P DIL	
	1	5322 255 44217	IC-FOOT 40 - P DIL	
	4	5322 255 44259	IC-FOOT 20 - P DIL	
	4	5322 255 44109	IC-FOOT 24 - P DIL	
	2	5322 255 44284	IC-FOOT 22 - P DIL	
79	2	4822 502 10692	CIL BOLT M3X30X19	
80	2	4822 532 10582	Washer 3.2X9	
81	2	4822 532 60711	Insulation bush	
82	2	5322 532 50488	Washer 4.3X9	
83	2	4822 532 10582	Washer 3.2X9	
84	2	4822 505 10325	Nut M3	
85	2	4822 532 10582	Washer	
86	2	4822 530 80173	Spring washer	
87	2	4822 505 10325	Nut M3	
88	1	5322 532 24578	Bushing	
89	1	4822 530 80173	Spring washer	
90	1	4822 502 11064	CIL bolt M3X6	
91	2	5322 255 40029	Transistor socket	
92	1	5322 256 40017	Fuse holder	
93	1	5322 325 64061	Cable grommet	
94	1	5322 405 94046	Bracket	
95	1	4822 502 10693	CIL bolt M4X8	
96	1	5322 321 14066	Mains cord assy	
97	4	5322 462 44457	Foot	
98	4	5322 529 14067	Rubber puffer	
99	4	4822 502 10056	CIL bolt M4X55	
100	4	5322 532 14593	Washer 4.3X12	

Item	Qty	Order number	Description	
101	4	4822 530 80163	Spring washer 4.1	
102	4	5322 532 24591	Distance bushing 6X5	
103	8	5322 532 24592	Distance bushing 6X20	
104	1	5322 447 94639	Inner rear plate (01 version)	
104	1	5322 466 80791	Inner rear plate (02 and up)	
105	6	5322 532 24577	Threaded spacer	
106	4	5322 381 14286	Window red	
107	2	5322 532 64277	Holder	RANGE INDICATION PROBE PARTS FIG. 1.11.
108	4	5322 532 64278	Ring	
109	2	5322 532 14696	Contact ring	
110	2	5322 492 64765	Contact spring	
111	1	5322 447 94652	Cast. al. front panel	
112	1	5322 447 94653	Cast. al. rear panel	
113	4	5322 466 90998	Spacer for alphanumeric display	
114	25	5322 414 25613	Push button + green (01 version)	
114	25		Push button + green (02 and up)	

Item	Ordering number	Value	Type
C1547	4822 121 40231	150 nF	A
C1554			
C1523	5322 121 40307	150 nF	C
C1524			
C1529			
C1531			
C1612	4822 121 40232	220 nF	A
C2038			
C2711			
C2734			
C3009	5322 121 40175	470 nF	A
C2737	5322 121 40233	680 nF	A
C2743			
C1537	5322 121 40197	1 μF	A
C1542			

Type: FOIL 10 % 1600 V

Item	Ordering number	Value
C1502	4822 121 40123	15 nF
C1503		

Type: FOIL 10 % 250 V

Item	Ordering number	Value
C1701	4822 121 41161	100 nF
C1702		

Type: FEEDTHROUGH 10 % 300 V

Item	Ordering number	Value
C2443	5322 123 34001	30 pF
C2519		
C2413	5322 123 10168	300 pF
C2483		

Type: TRIMMER

Item	Ordering number	Value
C2416	5322 125 54026	3 pF
C2444		
C2484		
C2521		
C2409	5322 125 54027	5.5 pF
C2427		
C2442		
C2477		
C2503		
C2518		

Item	Ordering number	Value
C2424	5322 125 50051	18 pF
C2447		
C2496		
C2523		
C3017		

Type: PAPER 10 % 250 V

C1608	5322 121 44142	220 nF

Type: HT 10 % 2000 V

C1607	5322 122 54024	270 pF
C1504	5322 122 54019	470 pF
C1518		
C1521		
C1522		
C1620		
C1625		

Type: HT 20% 4000 V

C1506	5322 122 54004	470 pF

Type: ELEC. TANTAL 20 % 16 V

C412	4822 124 10204	2.2 μF
C432	5322 124 14069	6.8 μF
C433		
C3022		
C1039	4822 124 20977	15 μF
C1048		
C1133		

Type: ELEC. TANTAL 20 % 35 V

C434	5322 124 14039	680 nF

Type: ELEC. TANTAL 40 % 16 V

C2568	4822 124 20947	3.3 μF
C3015		
C3020		

ALUMINIUM ELECTROLYTIC

Tolerance: –10 +50 %

Value (F)	Voltage (V)	Ordering number
4.7 µ	63	5322 124 24211
10 µ	63	4822 124 20728
15 µ	40	4822 124 20709
22 µ	25	4822 124 20698
33 µ	16	4822 124 20688
33 µ	40	4822 124 20712
47 µ	10	4822 124 20678
47 µ	63	4822 124 20733
68 µ	16	4822 124 20689
100 µ	10	4822 124 20679
220 µ	10	4822 124 20589
220 µ	16	4822 124 20693
220 µ	350	5322 124 44007
330 µ	10	4822 124 20684
680 µ	16	4822 124 20776
1000 µ	25	4822 124 20786
2200 µ	10	4822 124 20771

MINIATURE CERAMIC PLATE

Voltage : 100 V
Tolerance : Type A – 0.25 pF
Type B – 2 %
Type C – 10 %
Type D – –20 +50 %

Value (F)	Type	Ordering number
1 p	A	4822 122 30104
1.5 p	A	4822 122 30105
2.2 p	A	4822 122 31036
3.9 p	A	5322 122 34107
4.7 p	A	4822 122 31045
5.6 p	A	4822 122 31047
6.8 p	A	4822 122 31049
8.2 p	A	4822 122 31052
10 p	B	4822 122 31054
12 p	B	4822 122 31056
15 p	B	4822 122 31058
22 p	B	4822 122 31063
27 p	B	4822 122 30045
33 p	B	4822 122 31067
39 p	B	4822 122 31069
47 p	B	4822 122 31072
56 p	B	4822 122 31074
68 p	B	4822 122 31349
82 p	B	4822 122 31243
100 p	B	4822 122 31504
100 p	B	4822 122 31316
180 p	B	5322 122 34144
180 p	C	4822 122 30113
220 p	B	4822 122 31173

Value (F)	Type	Ordering number
220 p	B	4822 122 31222
270 p	B	4822 122 31335
470 p	C	4822 122 30034
560 p	C	4822 122 30126
1 n	C	4822 122 30027
1.8 n	C	4822 122 30048
2.2 n	C	4822 122 30114
4.7 n	C	4822 122 30128
10 n	D	4822 122 31414

MINIATURE CERAMIC PLATE

Voltage : 500 V
Tolerance : Type A – 0.25 pF
Type B – 2 %
Type C – 10 %

Value (F)	Type	Ordering number
2.2 p	A	4822 122 31186
3.9 p	A	4822 122 31217
6.8 p	A	4822 122 31192
8.2 p	A	4822 122 31194
12 p	B	4822 122 31196
68 p	B	4822 122 31207
100 p	B	4822 122 31081
560 p	C	4822 122 31166

1.2.2.2. Potentiometers

CARBON CONTROL POTENTIOMETER

Type : CP16
P at 40 °C : 0.1 W
Tolerance : 20 %

Item	Value (Ω)	Ordering number	Remarks
R1	47 k	5322 101 24185	Carbon potm. lin.
R2/S13	10 k	5322 101 44069	Carbon potm. lin. + switch
R3	10 k	5322 101 24184	Carbon potm. lin.
R4/S5	47 k	5322 101 64031	Carbon potm. lin. + switch
R5/S6	47 k	5322 101 64031	Carbon potm. lin. + switch
R6/S7	47 k	5322 101 64031	Carbon potm. lin. + switch
R7/S19	4.7 k	5322 101 44051	Carbon potm. lin. + switch
R8/S21	4.7 k	5322 101 44051	Carbon potm. lin. + switch
R9/S27	47 k	5322 101 64032	Carbon potm. lin. + switch
R10/R11	10 k	5322 102 34025	Carbon tandem potm.
R12/R13/S28	10 k	5322 102 44008	Carbon tandem potm. + switch
R15	47 k	5322 101 24203	Carbon potm. lin.
R16	4.7 k	5322 101 24186	Carbon potm. lin.

BOURNS CARBON POTENTIOMETER

Type : 3011 P-I-504
P : 0.25 W
Tolerance : 20 %

Item	Value (Ω)	Ordering number	Remarks
R14/S20	100 k	5322 101 44037	Carbon potm. lin. + switch

CERAMIC POTENTIOMETERS

Type : Cermet Preset
P at 70 °C : 0.5 W
Tolerance : 20 %

Type A : Horizontal mounting
Type B : Vertical mounting

Value (Ω)	Type	Ordering number
220	A	5322 101 14009
470	A	5322 101 14047
470	B	5322 101 14049
1 k	A	5322 100 10112
1 k	B	5322 101 10294
2.2 k	A	5322 101 14008
2.2 k	B	5322 100 10117
4.7 k	B	5322 101 14292
10 k	A	5322 100 10113
10 k	B	5322 101 14066

Value (Ω)	Type	Ordering number
22 k	A	5322 101 14069
22 k	B	5322 100 10118
47 k	B	5322 101 14293
100 k	A	5322 101 14071
100 k	B	5322 100 10116
1 M	B	5322 101 14068

1.2.2.3. Resistors

METALFILMRESISTORS

Series MR25 1 % Service code 5322 116 .....

4,99	5322 116 50568	16,5	5322 116 54109	54,9	5322 116 54445
5,11	5322 116 54192	16,9	5322 116 50627	56,2	5322 116 54446
5,23	5322 116 54113	17,4	5322 116 54432	57,6	5322 116 54447
5,36	5322 116 54239	17,8	5322 116 50418	59	5322 116 54448
5,49	5322 116 54102	18,2	5322 116 54083	60,4	5322 116 54449
5,62	5322 116 54128	18,7	5322 116 50895	61,9	5322 116 54451
5,76	5322 116 54413	19,1	5322 116 54104	63,4	5322 116 54375
5,90	5322 116 51064	19,6	5322 116 50473	64,9	5322 116 54453
6,04	5322 116 54114	20	5322 116 51048	66,5	5322 116 54454
6,19	5322 116 51049	20,5	5322 116 50678	68,1	5322 116 54455
6,34	5322 116 50862	21	5322 116 54433	69,8	5322 116 54456
6,49	5322 116 54112	21,5	5322 116 50677	71,5	5322 116 54457
6,65	5322 116 54414	22,1	5322 116 50983	73,2	5322 116 54458
6,81	5322 116 54013	22,6	5322 116 50491	75	5322 116 54459
6,98	5322 116 54103	23,2	5322 116 54434	76,8	5322 116 50494
7,15	5322 116 54415	23,7	5322 116 54014	78,7	5322 116 50578
7,32	5322 116 54416	24,3	5322 116 54435	80,6	5322 116 54461
7,50	5322 116 54417	24,9	5322 116 50903	82,5	5322 116 54462
7,68	5322 116 54418	25,5	5322 116 54436	84,5	5322 116 54463
7,87	5322 116 54046	26,1	5322 116 50876	86,6	5322 116 54464
8,06	5322 116 54419	26,7	5322 116 54067	88,7	5322 116 54465
8,25	5322 116 54099	27,4	5322 116 50493	90,9	5322 116 54466
8,45	5322 116 54421	28	5322 116 50623	93,1	5322 116 54467
8,66	5322 116 51051	28,7	5322 116 54068	95,3	5322 116 50569
8,87	5322 116 54101	29,4	5322 116 54084	97,6	5322 116 54468
9,09	5322 116 50863	30,1	5322 116 50904	100	5322 116 54469
9,31	5322 116 54422	30,9	5322 116 54437	102	5322 116 54471
9,53	5322 116 54258	31,6	5322 116 54034	105	5322 116 54472
9,76	5322 116 54423	32,4	5322 116 54105	107	5322 116 54473
10	5322 116 50452	33,2	5322 116 50527	110	5322 116 54474
10,2	5322 116 54111	34	5322 116 54433	113	5322 116 54475
10,5	5322 116 54071	34,8	5322 116 54027	115	5322 116 54476
10,7	5322 116 54424	35,7	5322 116 54439	118	5322 116 54477
11	5322 116 54059	36,5	5322 116 50409	121	5322 116 54426
11,3	5322 116 54425	37,4	5322 116 54158	124	5322 116 54478
11,5	5322 116 50838	38,3	5322 116 50954	127	5322 116 54479
11,8	5322 116 50738	39,2	5322 116 54087	130	5322 116 54481
12,1	5322 116 54069	40,2	5322 116 50926	133	5322 116 54482
12,4	5322 116 54427	41,2	5322 116 54108	137	5322 116 54483
12,7	5322 116 54261	42,2	5322 116 51052	140	5322 116 54484
13	5322 116 54082	43,2	5322 116 50519	143	5322 116 54485
13,3	5322 116 51047	44,2	5322 116 50818	147	5322 116 50766
13,7	5322 116 54428	45,3	5322 116 50795	150	5322 116 54486
14	5322 116 50839	46,4	5322 116 50492	154	5322 116 50506
14,3	5322 116 54429	47,5	5322 116 50952	158	5322 116 54487
14,7	5322 116 50412	48,7	5322 116 50511	162	5322 116 50417
15	5322 116 50902	49,9	5322 116 54441	165	5322 116 54488
15,4	5322 116 50925	51,1	5322 116 54442	169	5322 116 54489
15,8	5322 116 50861	52,3	5322 116 54443	174	5322 116 54491
16,2	5322 116 54431	53,6	5322 116 54444	178	5322 116 54492

182	5322 116 54493	604	5322 116 54528	2k	5322 116 54572
187	5322 116 54494	619	5322 116 54529	2k05	5322 116 50664
191	5322 116 54495	634	5322 116 54531	2k1	5322 116 54573
196	5322 116 50676	649	5322 116 54532	2k15	5322 116 50767
200	5322 116 54496	665	5322 116 54533	2k21	5322 116 54574
205	5322 116 50669	681	5322 116 54534	2k26	5322 116 50675
210	5322 116 54036	698	5322 116 54037	2k32	5322 116 54575
215	5322 116 50457	715	5322 116 50571	2k37	5322 116 54576
221	5322 116 54002	732	5322 116 54535	2k43	5322 116 54004
226	5322 116 54497	750	5322 116 54536	2k49	5322 116 50581
232	5322 116 54498	768	5322 116 54537	2k55	5322 116 54577
237	5322 116 50679	787	5322 116 54538	2k61	5322 116 50671
243	5322 116 50437	806	5322 116 54539	2k67	5322 116 54578
249	5322 116 54499	825	5322 116 54541	2k74	5322 116 50636
255	5322 116 54501	845	5322 116 54542	2k8	5322 116 54579
261	5322 116 54502	866	5322 116 54543	2k87	5322 116 50414
267	5322 116 54503	887	5322 116 54544	2k94	5322 116 54581
274	5322 116 54504	909	5322 116 54545	3k01	5322 116 50524
280	5322 116 54505	931	5322 116 54546	3k09	5322 116 54582
287	5322 116 54506	953	5322 116 54547	3k16	5322 116 50579
294	5322 116 54507	976	5322 116 54548	3k24	5322 116 54583
301	5322 116 54508	1k	5322 116 54549	3k32	5322 116 54005
309	5322 116 54509	1k02	5322 116 54551	3k4	5322 116 54584
316	5322 116 54511	1k05	5322 116 54552	3k48	5322 116 54585
324	5322 116 54512	1k07	5322 116 54553	3k57	5322 116 54586
332	5322 116 54513	1k1	5322 116 54554	3k65	5322 116 54587
340	5322 116 54514	1k13	5322 116 54555	3k74	5322 116 54588
348	5322 116 54515	1k15	5322 116 50415	3k83	5322 116 54589
357	5322 116 50603	1k18	5322 116 54556	3k92	5322 116 54591
365	5322 116 54516	1k21	5322 116 54557	4k02	5322 116 54592
374	5322 116 54517	1k24	5322 116 54559	4k12	5322 116 54593
383	5322 116 54518	1k27	5322 116 50555	4k22	5322 116 50729
392	5322 116 54006	1k3	5322 116 50526	4k32	5322 116 54594
402	5322 116 54519	1k33	5322 116 54561	4k42	5322 116 50556
412	5322 116 54521	1k37	5322 116 50628	4k53	5322 116 50631
422	5322 116 50459	1k4	5322 116 54562	4k64	5322 116 50484
432	5322 116 54522	1k43	5322 116 54563	4k75	5322 116 54008
442	5322 116 50592	1k47	5322 116 50635	4k87	5322 116 50509
453	5322 116 54523	1k5	5322 116 54564	4k99	5322 116 50523
464	5322 116 50536	1k54	5322 116 50586	5k11	5322 116 54595
475	5322 116 54007	1k58	5322 116 50622	5k23	5322 116 54596
487	5322 116 50508	1k62	5322 116 54565	5k36	5322 116 54597
499	5322 116 54524	1k65	5322 116 54566	5k49	5322 116 54598
511	5322 116 54525	1k69	5322 116 54567	5k62	5322 116 54011
523	5322 116 54526	1k74	5322 116 50629	5k76	5322 116 54599
536	5322 116 50621	1k78	5322 116 50515	5k9	5322 116 50583
549	5322 116 50732	1k82	5322 116 54568	6k04	5322 116 54601
562	5322 116 54009	1k87	5322 116 50728	6k19	5322 116 50608
576	5322 116 54527	1k91	5322 116 54569	6k34	5322 116 54602
590	5322 116 50561	1k96	5322 116 54571	6k49	5322 116 54603

6k65	5322 116 54604
6k81	5322 116 54012
6k98	5322 116 54605
7k15	5322 116 54606
7k32	5322 116 54607
7k5	5322 116 54608
7k68	5322 116 54609
7k87	5322 116 50458
8k06	5322 116 54611
8k25	5322 116 54558
8k45	5322 116 54612
8k66	5322 116 54613
8k87	5322 116 54614
9k09	5322 116 54615
9k31	5322 116 54616
9k53	5322 116 54617
9k76	5322 116 54618
10k	5322 116 54619
10k2	5322 116 54621
10k5	5322 116 50731
10k7	5322 116 54622
11k	5322 116 54623
11k3	5322 116 50668
11k5	5322 116 54624
11k8	5322 116 54625
12k1	5322 116 50572
12k4	5322 116 54626
12k7	5322 116 50443
13k	5322 116 50522
13k3	5322 116 54627
13k7	5322 116 54628
14k	5322 116 54629
14k3	5322 116 54631
14k7	5322 116 54632
15k	5322 116 54007
15k4	5322 116 50479
15k8	5322 116 54633
16k2	5322 116 50593
16k5	5322 116 54634
16k9	5322 116 54635
17k4	5322 116 54636
17k8	5322 116 54637
18k2	5322 116 54638
18k7	5322 116 50558
19k1	5322 116 54639
19k6	5322 116 54641
20k	5322 116 54642
20k5	5322 116 54643
21k	5322 116 54644
21k5	5322 116 50451
22k1	5322 116 54003
22k6	5322 116 50481
23k2	5322 116 54645
23k7	5322 116 54646
24k3	5322 116 54647
24k9	5322 116 54648
25k5	5322 116 54649
26k1	5322 116 54651
26k7	5322 116 54652
27k4	5322 116 50559
28k	5322 116 50667
28k7	5322 116 54653
29k4	5322 116 54654
30k1	5322 116 54655
30k9	5322 116 54656
31k6	5322 116 54657
32k4	5322 116 54658
33k2	5322 116 50482
34k	5322 116 54659
34k8	5322 116 54661
35k7	5322 116 54662
36k5	5322 116 50726
37k4	5322 116 54663
38k3	5322 116 50483
39k2	5322 116 54664
40k2	5322 116 54665
41k2	5322 116 54666
42k2	5322 116 50474
43k2	5322 116 54667
44k2	5322 116 54668
45k3	5322 116 54669
46k4	5322 116 50557
47k5	5322 116 54671
48k7	5322 116 50442
49k9	5322 116 50674
51k1	5322 116 50672
52k3	5322 116 54673
53k6	5322 116 54674
54k9	5322 116 54675
56k2	5322 116 54676
57k6	5322 116 54677
59k	5322 116 54678
60k4	5322 116 54679
61k9	5322 116 50872
63k4	5322 166 54681
64k9	5322 116 50514
66k5	5322 116 54682
68k1	5322 116 54683
69k8	5322 116 54684
71k5	5322 116 54685
73k2	5322 116 50666
75k	5322 116 54686
76k8	5322 116 54687
78k7	5322 116 50533
80k6	5322 116 54688
82k5	5322 116 54689
84k5	5322 116 54691
86k6	5322 116 54692
88k7	5322 116 54693
90k9	5322 116 54694
93k1	5322 116 54297
95k3	5322 116 50567
97k6	5322 116 54695
100k	5322 116 54696
102k	5322 116 54697
105k	5322 116 54698
107k	5322 116 54699
110k	5322 116 54701
113k	5322 116 54702
115k	5322 116 54279
118k	5322 116 54703
121k	5322 116 54704
124k	5322 116 54705
127k	5322 116 54706
130k	5322 116 54707
133k	5322 116 54708
137k	5322 116 54709
140k	5322 116 54259
143k	5322 116 54711
147k	5322 116 54712
150k	5322 116 54713
154k	5322 116 54714
158k	5322 116 54715
162k	5322 116 54716
165k	5322 116 54717
169k	5322 116 54718
174k	5322 116 54719
178k	5322 116 54721
182k	5322 116 54722
187k	5322 116 54723
191k	5322 116 54724
196k	5322 116 54725
200k	5322 116 54726
205k	5322 116 54727
210k	5322 116 54208
215k	5322 116 54728
221k	5322 116 54038
226k	5322 116 54729
232k	5322 116 54731
237k	5322 116 54732
243k	5322 116 54733
249k	5322 116 54734
255k	5322 116 54735
261k	5322 116 54736
267k	5322 116 54737
274k	5322 116 54738
280k	5322 116 54739
287k	5322 116 54741
294k	5322 116 54742
301k	5322 116 54743

Series MR30 1 %

301k	5322 116 54216	619k	5322 116 54326
316k	5322 116 54154	640k	5322 116 50768
332k	5322 116 54185	681k	5322 116 54263
348k	5322 116 54325	723k	5322 116 54095
365k	5322 116 54762	750k	5322 116 54235
383k	5322 116 54761	787k	5322 116 51018
402k	5322 116 54744	825k	5322 116 54195
422k	5322 116 50196	866k	5322 116 54757
445k	5322 116 50019	909k	5322 116 54408
464k	5322 116 54759	953k	5322 116 50397
490k	5322 116 50575	1M	5322 116 54188
511k	5322 116 54123		
536k	5322 116 54758		
562k	5322 116 54266		
584k	5322 116 50252		

LACQUERED METAL FILM

Type : MR 16
P at 70 ^{o}C : 0.25 W
Tolerance : 1 %

Item	Value (Ω)	Ordering number
R3050-3055	127	5322 116 55396
R2475-2602-2605	1 k	5322 116 55393

LACQUERED METAL FILM

Type : MR spec.
P at 70 ^{o}C : 0.25 W
Tolerance : 1 %

R2413-2546	992 k	5322 116 55153

POWER METAL FILM

Type : PR52
P at 70 ^{o}C : 1.6 W
Tolerance : 5 %

R1604	20	5322 116 54351
R1603	2 k	5322 116 55205
R1619-1621	27 k	5322 116 54983

CARBON FILM

Type : CR 16
P at 70 ^{o}C : 0.2 W
Tolerance : 5 %

R2423-2559	10	4822 111 30347
R2472-2599	15	5322 111 44153
R2459-2586	22	5322 111 30396
R2463-2591	27	4822 111 30348
R2436-2464-2568-2592	33	4822 111 30067
R2422-2471-2544-2598	560	4822 111 30309

CARBON FILM

P at 70 ^{o}C : 0.125 W
Tolerance : 5 %

R2426-2562-2704	100 M	5322 111 30376

Item	Value (Ω)	Ordering number

HIGH-VOLTAGE

Type : VR 25
P at 70 °C : 0.25 W
Tolerance : 5 %

R2410	1.5 M	4822 110 72192
R2415	3.3 M	4822 110 72201
R2400	5.6 M	4822 110 72207

HIGH-VOLTAGE

Type : VR 37
P at 70 °C : 0.5 W
Tolerance : 5 % or 1 %

R1617	1 M	4822 110 42187
R1509	2.2 M	4822 110 42196
R1502	6.8 M	4822 110 42209
R1522	10 M	4822 110 42214 (1 %)
	31.6 M	5322 116 64103 (1 %)

CEMENTED WIREWOUND

Type : WR 0617
P at 70 °C : 4 W
Tolerance : 5 %

R1616	3.3 k	4822 112 21121

RESISTOR CIRCUIT

P at 70 °C : 9 x 0.2 W
Tolerance : 2 %

R801	3.3 k	5322 111 94255

PTC THERMISTOR DISC

P at 55°C : 0.5 W
Tolerance : 25 %

R1631	1.5 k	5322 116 34051

PTC THERMISTOR DISC

R1507	30-50	4822 116 40031

NTC THERMISTOR DISC

P at 55 °C : 0.5 W
Tolerance : 10 %

R1120-1130	6.8 k	5322 116 34058

1.2.2.4. Transistors

Type	Ordering number
BC264A	5322 130 44476
BC547B	4822 130 40959
BC549C	4822 130 44246
BC556	4822 130 40989
BC558	4822 130 40941
BC558B	4822 130 44197
BC559B	4822 130 44358
BD237	4822 130 44235
BD435	4822 130 40982
BD436	4822 130 44421
BF199	4822 130 44154
BF324	4822 130 41448
BF422	4822 130 41544
BF423	4822 130 41543
BF450	4822 130 44237
BFQ24	
BFW30	5322 130 40379
BFY90	4822 130 40493
BRY39	5322 130 40482
BSS38	4822 130 40968
BSX20	5322 130 40417
BUX86	5322 130 44718

1.2.2.5. Diodes

Type	Ordering number
BAX12A	5322 130 34605
BAV21	4822 130 30842
BAV45	5322 130 34037
BAW62	4822 130 30613
BSV80	5322 130 34044
BT151-500R	5322 130 24081
BU208A	4822 130 31171
BY208-800	4822 130 31348
BY208-1000	4822 130 31051
BY224-600	5322 130 34761
BY409A	5322 130 34594
BYW29-150	5322 130 34711
BYX55-600	4822 130 30817
BZV10	5322 130 34439
BZV13	5322 130 34301
BZX75-C1V4	4822 130 34047
BZX75-C2V1	4822 130 34049
BZX75-C2V8	4822 130 34048
BZX79-C4V7	4822 130 34174
BZX79-C5V1	4822 130 34233
BZX79-C5V6	4822 130 34173
BZX79-C6V2	4822 130 31111
BZX79-B6V2	4822 130 34167
BZX79-B6V8	4822 130 34278
BZX79-C9V1	4822 130 30862
BZX79-C10	4822 130 34297
BZX79-C12	4822 130 34197
BZX79-C30	4822 130 34328
BZX79-C47	4822 130 34383
BZY88-C3V3	5322 130 30392
FH1100	5322 130 34062
1N823	5322 130 34405

1.2.2.6. Integrated circuits

Type	Ordering number
ADC80-AGZ-10	5322 209 86447
CA3086	5322 209 84111
GXB10102P	5322 209 85955
GXB10116P	5322 209 86441
GXB10124P	5322 209 86341
GXB10125P	5322 209 86119
GXB10137P	5322 209 86265
GXB10174P	5322 209 86442
GXB10231P	5322 209 86003
HEF4001BP	5322 209 14045
HEF4008BP	5322 209 14214
HEF4013BP	5322 209 10002
HEF4049BP	5322 209 14049
HEF4051BP	5322 209 14212
HEF4052BP	5322 209 14233
HEF4053BP	5322 209 14121
HEF4070BP	5322 209 14073
HEF4073BP	5322 209 14066
HEF4081BP	5322 209 14054
HEF4093BP	5322 209 14186
HEF4508BP	5322 209 14559
HEF4518BP	5322 209 14064
HEF4520BP	5322 209 14189
HEF4526BP	5322 209 14858
HEF4528BP	5322 209 14191
HEF4539BP	5322 209 14442
HEF4731VP	5322 209 14859
HEF40097BP	5322 209 14433
LF356N	5322 209 86451
LM308AN	5322 209 86056
LM308N	4822 209 80293
LM324N	5322 209 85899
LM339AN	4822 209 80631
LM358N	4822 209 80484
LM7805CT	5322 209 86445
MCM51L01P45	5322 209 10155
NE521N	5322 209 14441
NE5018N	5322 209 86421
NE5537H	5322 209 86444
OQ0012	5322 209 85484
OQ0017	5322 209 85627
OQ0043	5322 209 86488
P8085A	5322 209 86035
DRIVER (D1001)	5322 209 86489
SD5000N	5322 209 85748
N74LS00N	5322 209 84823
N74S00N	5322 209 84167
N74LS02N	5322 209 85312
N7404N	5322 209 86326
N74LS04N	5322 209 85486
N7406N	5322 209 84073
N74LS08N	5322 209 84995
N74LS10N	5322 209 84996
N74LS11N	5322 209 85604

Type	Ordering number
SN74LS27N-00	5322 209 86076
N74LS30N	5322 209 84985
N74LS32	5322 209 85311
N74LS42N	5322 209 85562
N74LS74AN	5322 209 84986
SN74S74N-00	5322 209 84183
N74LS86N	5322 209 84997
N74LS90N	5322 209 85255
N74LS107N	5322 209 85816
SN74LS123N-00	5322 209 85266
N74LS132N	5322 209 85201
N74LS138N	5322 209 85647
N74LS139N	5322 209 85839
SN74LS151N-00	5322 209 86452
N74LS153N	5322 209 85688
N74LS153N	5322 209 85488
N74LS163AN	5322 209 85863
N74LS191N	5322 209 84989
N74LS193N	5322 209 85405
SN74S196N-00	5322 209 85411
SN74S197N-00	5322 209 86448
SN74LS373N-00	5322 209 86062
S74LS244N-00	5322 209 86017
SN74LS245N-00	5322 209 86225
SN74LS257N-00	5322 209 80859
N74LS266N	5322 209 86163
TL082CP	5322 209 86064
TDA1060	5322 209 85662
TDA3081	5322 209 85767
µA741CN	5322 209 85254
11C58PC	5322 209 86446
7905CU	5322 130 44843
SL3145E	5322 130 34854
T&H GATE (D3001)	5322 209 86491

OPTOCOUPLER

H11A550	5322 130 94015

1.2.2.7. Miscellaneous

Item	Ordering number	Type/Description
B1	5322 130 34875	Led red cqy 54 – 111
B2	5322 130 34875	Led red cqy 54 – 111
B3	5322 130 34875	Led red cqy 54 – 111
B4	5322 130 34875	Led red cqy 54 – 111
B5	5322 130 34875	Led red cqy 54 – 111
B6	5322 130 34875	Led red cqy 54 – 111
B7	5322 130 34875	Led red cqy 54 – 111
B8	5322 130 34875	Led red cqy 54 – 111
B9	5322 130 34875	Led red cqy 54 – 111
B10	5322 130 34971	DL1414D Display
B11	5322 130 34971	DL1414D Display
B12	5322 130 34971	DL1414D Display
B13	4822 134 40167	Lamp 5 V 60 mA
B14	4822 134 40167	Lamp 5 V 60 mA
B15	5322 130 34875	Led red cay 54 – 111
B16	5322 130 34875	Led red cqy 54 – 111
B17	4822 134 40167	Lamp 5 V 60 mA
B18	4822 134 40167	Lamp 5 V 60 mA
B19	4822 134 40167	Lamp 5 V 60 mA
B20	4822 134 40167	Lamp 5 V 60 mA
B21	5322 130 34971	DL1414D Display
B22	5322 130 34875	Led red cqy 54 – 111
B23	5322 130 34875	Led red cqy 54 – 111
B24	4822 130 31144	Led red cqy 24B
B401	5322 242 74397	CRYSTAL 5MC
E1	5322 134 44177	Lamp 28 V - 80 mA
E2	5322 134 44177	Lamp 28 V - 80 mA
F1701	4822 253 30025	Fuse
K2401...K2418	5322 280 24126	Reed contact
K2401...K2418	5322 156 14076	Reed coil
K2701	5322 280 24103	Reed relay assy
L1101	5322 158 10283	Microchoke 150 μH
L1102	5322 156 14101	Coil
L1103	5322 156 14101	Coil
L1104	5322 156 14101	Coil
L1106	5322 156 14101	Coil
L1501 L1502 L1503 L1504	4822 152 20486	Choke AT 4043-15
L1506	5322 152 24095	Choke TFU-15
L1508 L1509	5322 152 24094	Choke TFU-15
L1601	5322 281 64154	Coil
L1602	5322 152 24062	Choke
L1603	5322 156 14076	Coil
L1604	5322 156 14076	Coil
L2401 L2402 L2403 L2404	5322 156 14076	Coil

Item	Ordering number	Type/Description
L2406 L2407 L2408 L2409 L2411 L2412	5322 158 14283	Coil assy.
S1	5322 276 44099	Pushbutton switch
S8	5322 276 34063	Pushbutton switch
S11	5322 276 34064	Pushbutton switch
S14	5322 276 74026	Pushbutton switch
S20	5322 278 64015	Rotary switch
S22	5322 278 64015	Rotary switch
S23	5322 278 64015	Rotary switch
S29	5322 276 44084	Pushbutton switch
S30	5322 276 74037	Pushbutton switch
S37	5322 276 44085	Pushbutton switch
S39	5322 276 44086	Pushbutton switch
S45	5322 277 24071	Mains voltage adaptor
S201	5322 263 64007	Plug (jumper)
S1201	5322 263 64007	Plug (jumper)
S1801	4822 277 10348	Switch assy.
T1501	5322 142 64104	Transformer
T1601	5322 148 84041	Transformer
T1602	5322 146 34126	Transformer
T1603	5322 142 44026	Transformer
V1	5322 131 24086	C.R.T. D14-292GH/39
X1	5322 267 14014	CAL socket
X2	5322 405 94073	CAL current loop
X3	5322 267 10004	HF-CON BNC Female
X4	5322 267 14037	Connector
X5	5322 535 84446	Threaded end
X6	5322 267 10004	HF-CON BNC Female
X7	5322 268 14157	Contact
X8	5322 268 14157	Contact
X259	5322 267 74111	Plug female
X1606	4822 266 30071	Plug
Z1701	5322 121 44261	Mains filter

1.2.2.8. Connectors

Ordering number	Description
5322 265 64082	64-pole connector male } PLUG-IN UNITS
5322 267 74092	64-pole connector female } PLUG-IN UNITS
5322 267 64007	CIS connectors male
5322 267 64031	CIS connectors bottom entry
5322 265 54006	CIS connectors top entry
5322 290 34123	Soldering pin for measuring points
4822 267 50268	CIS connector male
5322 268 24116	Coaxial socket, vertically mounted on pc boards
4822 265 30121	3-pole socket (stocko MKS 823-1-0-303)
5322 268 24133	Delay line connectors

1.2.2.8. IEC 625-1 bus interface unit A14 (PM3325).

Item	Ordering number	Description			
		CAPACITORS			
C 1401	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1402	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1403	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1404	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1406	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1407	4822 122 31173	CAPACITOR,CERAM	220PF	10%	500V
C 1408	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1409	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1411	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1412	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1413	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1414	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1416	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1417	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1418	4822 122 31054	CAPACITOR,CERAM	10PF	2%	100V
C 1419	4822 122 31054	CAPACITOR,CERAM	10PF	2%	100V
C 1421	4822 122 31054	CAPACITOR,CERAM	10PF	2%	100V
C 1422	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1423	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1424	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1426	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1427	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1428	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1429	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1431	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1432	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1433	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1434	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1436	4822 122 31173	CAPACITOR,CERAM	220PF	10%	500V
C 1437	4822 124 20699	CAP,ELECTROLYT	47UF	50%	25V
		RESISTORS			
R 1401	5322 116 50608	RESISTOR,M.FILM	6K19	1%	0,4W
R 1402	5322 116 50608	RESISTOR,M.FILM	6K19	1%	0,4W
R 1403	5322 116 50608	RESISTOR,M.FILM	6K19	1%	0,4W
R 1404	5322 116 50608	RESISTOR,M.FILM	6K19	1%	0,4W

Item	Ordering number	Description
	INTEGRATED CIRCUITS	
D 1401	5322 209 84823	INTEGR.CIRCUIT N74LS00N
D 1402	5322 209 84996	INTEGR.CIRCUIT SN74LS10N
D 1403	5322 209 85311	INTEGR.CIRCUIT N74LS32A
D 1404	5322 209 84995	INTEGR.CIRCUIT SN74LS08N
D 1406	5322 209 85464	INTEGR.CIRCUIT MC3441P
D 1407	5322 209 85464	INTEGR.CIRCUIT MC3441P
D 1408	5322 209 14509	INTEGR.CIRCUIT HEF4738VP
D 1409	5322 209 85266	INTEGR.CIRCUIT SN74LS123N
D 1411	5322 209 85312	INTEGR.CIRCUIT N74LS02A
D 1412	5322 209 85266	INTEGR.CIRCUIT SN74LS123N
D 1413	5322 209 85562	INTEGR.CIRCUIT
D 1414	5322 209 85752	INTEGR.CIRCUIT N74LS155N
D 1416	5322 209 85464	INTEGR.CIRCUIT MC3441P
D 1417	5322 209 85464	INTEGR.CIRCUIT MC3441P
D 1418	5322 209 84997	INTEGR.CIRCUIT SN74LS86N
D 1419	5322 209 85346	INTEGR.CIRCUIT SN74LS279N
D 1421	5322 209 84823	INTEGR.CIRCUIT N74LS00N
D 1422	5322 209 84823	INTEGR.CIRCUIT N74LS00N
D 1423	5322 209 86017	INTEGR.CIRCUIT SN74LS244N
D 1424	5322 209 86062	INTEGR.CIRCUIT
D 1426	5322 209 86062	INTEGR.CIRCUIT
D 1427	5322 209 86062	INTEGR.CIRCUIT
D 1428	5322 209 86017	INTEGR.CIRCUIT SN74LS244N
D 1429	5322 209 14219	INTEGR.CIRCUIT HEF4014BP
D 1431	5322 209 14219	INTEGR.CIRCUIT HEF4014BP
		MISCELLANEOUS
S 1401	5322 277 24045	SWITCH
S 1402	5322 277 24045	SWITCH
S 1403	5322 277 24045	SWITCH
S 1404	5322 277 24045	SWITCH
S 1405	5322 277 24045	SWITCH
S 1406	5322 277 24045	SWITCH
S 1407	5322 277 24053	SWITCH,SLIDE
X 1401	5322 265 64082	SOCKET,MALE
A80	5322 321 20474	CABLE,CONNECT.
D407	5322 209 10151	INTEGR.CIRCUIT
	5322 500 10265	NUT

13. ADDITIONAL DIAGRAMS

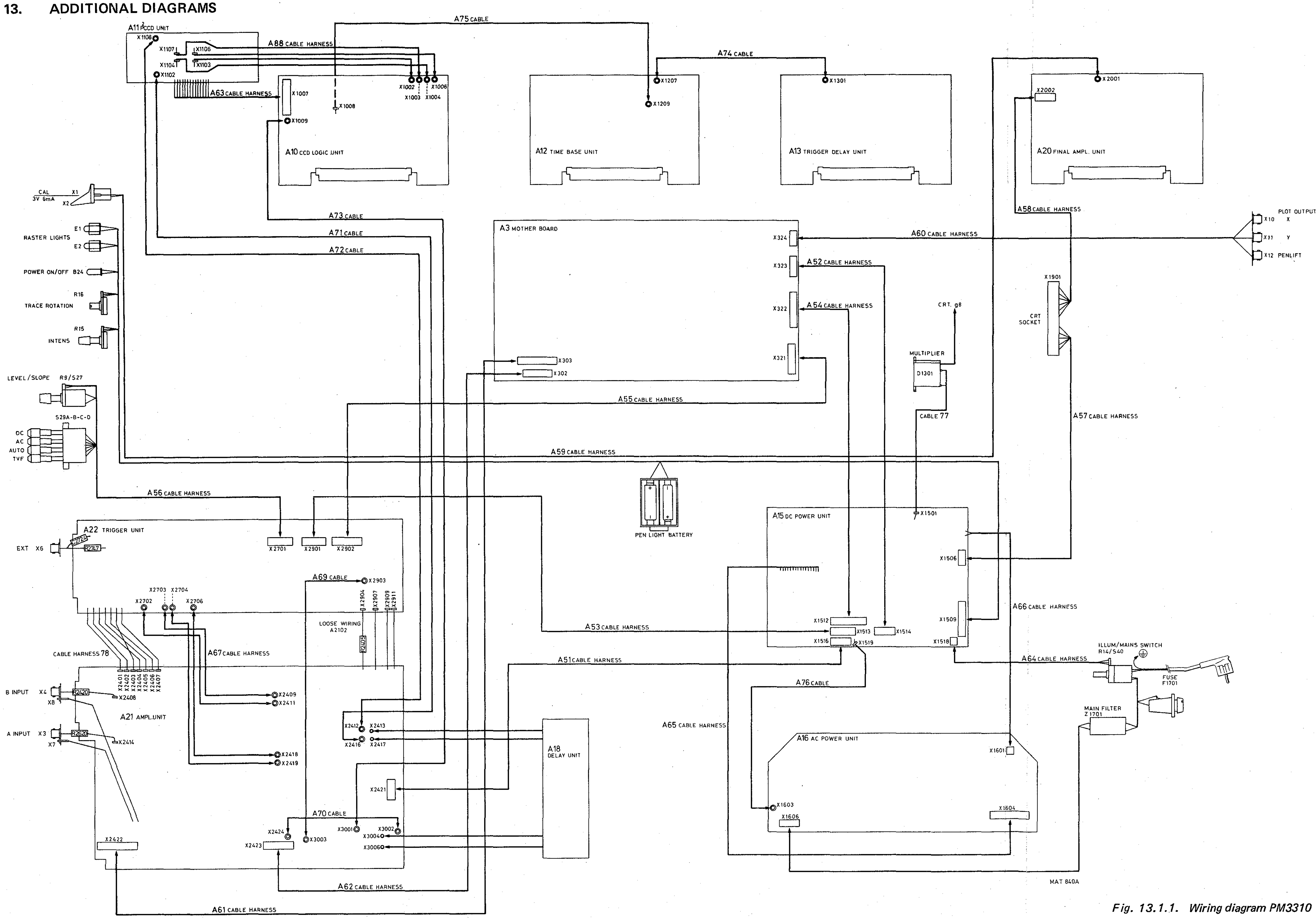


Fig. 13.1.1. Wiring diagram PM3310

CODING SYSTEM OF FAILURE REPORTING FOR QUALITY ASSESSMENT OF T & M INSTRUMENTS
(excl. potentiometric recorders)

The information contents of the coded failure description is necessary for our computerized processing of quality data.

Since the reporting of repair and maintenance routines must be complete and exact, we give you an example of a correctly filled-out PHILIPS SERVICE Job sheet.

① Country	② Day Month Year	③ Typenumber /Version	④ Factory/Serial no.
3 2	1 5 0 4 7 5	0 P M 3 2 6 0 0 2	D 0 0 0 7 8 3

CODED FAILURE DESCRIPTION ⑥

⑤ Nature of call	Location	Component/sequence no.	Category
☐ Installation		T S 0 6 0 7	5
☐ Pre sale repair		R 0 0 6 3 1	2
☐ Preventive maintenance	0 0 2 1	9 9 0 0 0 1	4
☒ Corrective maintenance			
☐ Other			

⑦ *Job completed* ☒

Working time ⑧ ☐☐ 1 2 Hrs

Detailed description of the information to be entered in the various boxes:

①Country: 3 2 = Switzerland

②Day Month Year 1 5 0 4 7 5 = 15 April 1975

③Type number/Version 0 P M 3 2 6 0 0 2 = Oscilloscope PM 3260, version 02 (in later oscilloscopes this number is placed in front of the serial no)

④Factory/Serial number D 0 0 0 7 8 3 = DO 783 These data are mentioned on the type plate of the instrument

⑤ Nature of call: Enter a cross in the relevant box

⑥ Coded failure description

Location

☐☐☐☐

These four boxes are used to isolate the problem area. Write the code of the part in which the fault occurs, e.g. unit no or mechanical item no of this part (refer to 'PARTS LISTS' in the manual).

Example: 0001 for Unit 1
000A for Unit A
0075 for item 75

If units are not numbered, do not fill in the four boxes; see Example Job sheet.

Component/sequence no.

☐☐☐☐☐☐

These six boxes are intended to pinpoint the faulty component.

A. Enter the component designation as used in the circuit diagram. If the designation is alfa-numeric,the letters must be written (starting from the left) in the two left-hand boxes and the figures must be written (in such a way that the last digit occupies the right-most box) in the four right-hand boxes.

B. Parts not identified in the circuit diagram:

- 990000 Unknown/Not applicable
- 990001 Cabinet or rack (text plate, emblem, grip, rail, graticule, etc.)
- 990002 Knob (incl. dial knob, cap, etc.)
- 990003 Probe (only if attached to instrument)
- 990004 Leads and associated plugs
- 990005 Holder (valve,transistor, fuse, board, etc.)
- 990006 Complete unit (p.w. board, h.t. unit, etc.)
- 990007 Accessory (only those without type number)
- 990008 Documentation (manual, supplement, etc.)
- 990009 Foreign object
- 990099 Miscellaneous

Category

☐

- 0 Unknown, not applicable (fault not present, intermittent or disappeared)
- 1 Software error
- 2 Readjustment
- 3 Electrical repair (wiring, solder joint, etc.)
- 4 Mechanical repair (polishing, filing, remachining, etc.)
- 5 Replacement (of transistor, resistor, etc.)
- 6 Cleaning and/or lubrication
- 7 Operator error
- 8 Missing items (on pre-sale test)
- 9 Environmental requirements are not met

⑦ Job completed: Enter a cross when the job has been completed.

⑧ Working time: Enter the total number of working hours spent in connection with the job (excluding travelling, waiting time, etc.), using the last box for tenths of hours.

☐☐ 1 2 = 1,2 working hours (1 h 12 min.)

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Costa Rica: Philips de Costa Rica Ltda. Apartado Postal 4325, San José; tel. 210111

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Eire: Philips Electrical (Ireland) Ltd., Newstead, Clonskeagh, Dublin 14; tel. 693355

El Salvador: Philips de El Salvador S.A., Apartado Postal 865, San Salvador; tel. 217441/229066

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Finland: See Suomi

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New Zealand: Philips Electrical Industries of N.Z. Ltd., Scientific and Industrial Equipment Division; Wakefield Street 181-195, P.O.B. 2097, Wellington C1; tel. 859 859

Nigeria: Associated Electronic Products (Nigeria) Ltd., 6 Ijora Causeway, P.O.B. 1921, Lagos; tel. 845414/7

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